



Package Style: Hermetic 2-Pin Flanged Ceramic

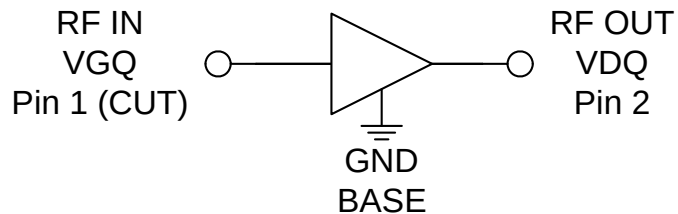


## Features

- Broadband Operation DC to 3.5GHz
- Advanced GaN HEMT Technology
- Advanced Heat-Sink Technology
- Gain = 15dB at 2GHz
- 48V Operation Typical Performance at 900MHz
  - Output Power 50W
  - Drain Efficiency 65%
  - -40 °C to 85 °C Operation

## Applications

- Commercial Wireless Infrastructure
- Cellular and WiMAX Infrastructure
- Civilian and Military Radar
- General Purpose Broadband Amplifiers
- Public Mobile Radios
- Industrial, Scientific and Medical



Functional Block Diagram

## Product Description

The RF3931 is a 48V 30W high power discrete amplifier designed for commercial wireless infrastructure, cellular and WiMAX infrastructure, industrial/scientific/medical, and general purpose broadband amplifier applications. Using an advanced high power density Gallium Nitride (GaN) semiconductor process, these high-performance amplifiers achieve high efficiency and flat gain over a broad frequency range in a single amplifier design. The RF3931 is an unmatched GaN transistor packaged in a hermetic, flanged ceramic package. This package provides excellent thermal stability through the use of advanced heat sink and power dissipation technologies. Ease of integration is accomplished through the incorporation of simple, optimized matching networks external to the package that provide wide-band gain and power performance in a single amplifier.

## Ordering Information

|               |                                                             |
|---------------|-------------------------------------------------------------|
| RF3931S2      | 2-Piece sample bag                                          |
| RF3931SB      | 5-Piece bag                                                 |
| RF3931SQ      | 25-Piece bag                                                |
| RF3931SR      | 100 Pieces on 7" short reel                                 |
| RF3931TR7     | 750 Pieces on 7" reel                                       |
| RF3931PCK-411 | Fully assembled evaluation board optimized for 2.14GHz; 48V |

## Optimum Technology Matching® Applied

|                                      |                                      |                                     |                                              |
|--------------------------------------|--------------------------------------|-------------------------------------|----------------------------------------------|
| <input type="checkbox"/> GaAs HBT    | <input type="checkbox"/> SiGe BiCMOS | <input type="checkbox"/> GaAs pHEMT | <input checked="" type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET | <input type="checkbox"/> Si BiCMOS   | <input type="checkbox"/> Si CMOS    | <input type="checkbox"/> BiFET HBT           |
| <input type="checkbox"/> InGaP HBT   | <input type="checkbox"/> SiGe HBT    | <input type="checkbox"/> Si BJT     |                                              |

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## Absolute Maximum Ratings

| Parameter                                                                                              | Rating          | Unit  |
|--------------------------------------------------------------------------------------------------------|-----------------|-------|
| Drain Voltage ( $V_D$ )                                                                                | 150             | V     |
| Gate Voltage ( $V_G$ )                                                                                 | -8 to +2        | V     |
| Gate Current                                                                                           | 23              | mA    |
| Operational Voltage                                                                                    | 65              | V     |
| Ruggedness (VSWR)                                                                                      | 10:1            |       |
| Storage Temperature Range                                                                              | -55 to +125     | °C    |
| Operating Temperature Range ( $T_L$ )                                                                  | -40 to +85      | °C    |
| Operating Junction Temperature ( $T_J$ )                                                               | 200             | °C    |
| Human Body Model                                                                                       | Class 1A        |       |
| MTTF ( $T_J < 200^\circ\text{C}$ , 95% Confidence Limits)*                                             | $3 \times 10^6$ | hours |
| Thermal Resistance, $R_{TH}$ (junction to case)<br>measured at $T_C = 85^\circ\text{C}$ , DC bias only | 3.6             | °C/W  |

\*MTTF - median time to failure for wear-out failure mode (30% $I_{dss}$  degradation) which is determined by the technology reliability. Refer to product qualification report for FIT (random) Failure rate.

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page two.

Bias Conditions should also satisfy the following expression:

$$P_{DISS} < (T_J - T_C) / R_{TH} \text{ J-C and } T_C = T_{CASE}$$



**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

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RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

| Parameter                                            | Specification |      |      | Unit | Condition                                    |
|------------------------------------------------------|---------------|------|------|------|----------------------------------------------|
|                                                      | Min.          | Typ. | Max. |      |                                              |
| Recommended Operating Conditions                     |               |      |      |      |                                              |
| Drain Voltage (V <sub>DSQ</sub> )                    | 28            |      | 48   | V    |                                              |
| Gate Voltage (V <sub>GSQ</sub> )                     | -5            | -3   | -2.5 | V    |                                              |
| Drain Bias Current                                   |               | 130  |      | mA   |                                              |
| Frequency of Operation                               | DC            |      | 3500 | MHz  |                                              |
| Capacitance                                          |               |      |      |      |                                              |
| C <sub>RSS</sub>                                     |               | 4    |      | pF   | V <sub>G</sub> = -8V, V <sub>D</sub> = 0V    |
| C <sub>ISS</sub>                                     |               | 17   |      | pF   | V <sub>G</sub> = -8V, V <sub>D</sub> = 0V    |
| C <sub>OSS</sub>                                     |               | 12   |      | pF   | V <sub>G</sub> = -8V, V <sub>D</sub> = 0V    |
| DC Function Test                                     |               |      |      |      |                                              |
| I <sub>G (OFF)</sub> - Gate Leakage                  |               |      | 2    | mA   | V <sub>G</sub> = -8V, V <sub>D</sub> = 0V    |
| I <sub>D (OFF)</sub> - Drain Leakage                 |               |      | 2.5  | mA   | V <sub>G</sub> = -8V, V <sub>D</sub> = 48V   |
| V <sub>GS (TH)</sub> - Threshold Voltage             |               | -4.2 |      | V    | V <sub>G</sub> = -8V, I <sub>D</sub> = 6.6mA |
| V <sub>DS (ON)</sub> - Drain Voltage at high current |               | 0.25 |      | V    | V <sub>G</sub> = 0V, I <sub>D</sub> = 1.5A   |
| RF Function Test                                     |               |      |      |      | [1],[2]                                      |
| V <sub>GS (Q)</sub>                                  |               | -3.5 |      | V    | V <sub>D</sub> = 48V, I <sub>D</sub> = 130mA |
| Gain                                                 | 10            | 12   |      | dB   | CW, P <sub>OUT</sub> = 45.8dBm, f = 2140MHz  |
| Drain efficiency                                     | 55            | 60   |      | %    | CW, P <sub>OUT</sub> = 45.8dBm, f = 2140MHz  |
| Input Return Loss                                    |               | -12  | -10  | dB   | CW, P <sub>OUT</sub> = 45.8dBm, f = 2140MHz  |

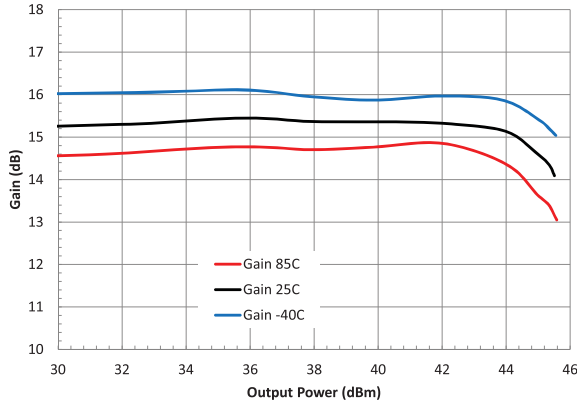
| Parameter                     | Specification |      |      | Unit | Condition       |
|-------------------------------|---------------|------|------|------|-----------------|
|                               | Min.          | Typ. | Max. |      |                 |
| <b>RF Typical Performance</b> |               |      |      |      | [1],[2]         |
| Small Signal Gain             |               | 20   |      | dB   | CW, f = 900MHz  |
| Small Signal Gain             |               | 14   |      | dB   | CW, f = 2140MHz |
| Output Power at P3dB          |               | 47   |      | dBm  | CW, f = 900MHz  |
| Output Power at P3dB          |               | 46.5 |      | dBm  | CW, f = 2140MHz |
| Drain Efficiency at P3dB      |               | 65   |      | %    | CW, f = 900MHz  |
| Drain Efficiency at P3dB      |               | 65   |      | %    | CW, f = 2140MHz |

[1] Test Conditions: CW Operation,  $V_{DSQ} = 48V$ ,  $I_{DQ} = 130mA$ ,  $T = 25^{\circ}C$

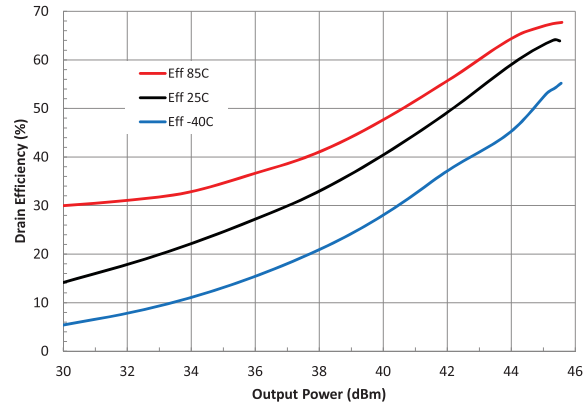
[2] Performance in a standard tuned test fixture

## Typical Performance in standard 2.14GHz fixed tuned test fixture (CW, T = 25 °C, unless noted)

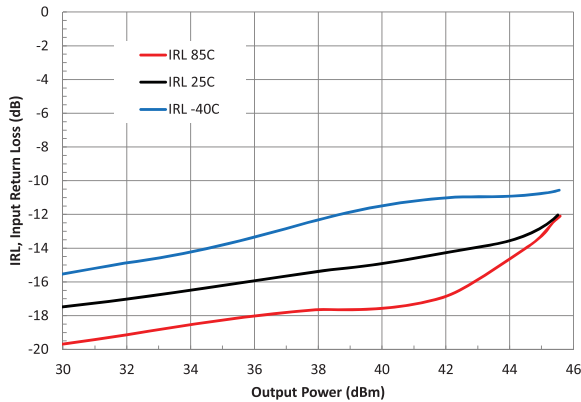
**Gain vs. Output Power (f = 2140MHz)**  
(Pulsed 10% duty cycle, 10uS, Vd = 48V, Idq = 130mA)



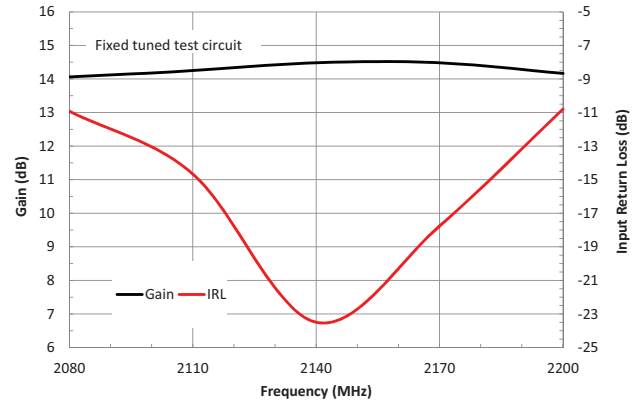
**Efficiency vs. Output Power (f = 2140MHz)**  
(Pulsed 10% duty cycle, 10uS, Vd = 48V, Idq = 130mA)



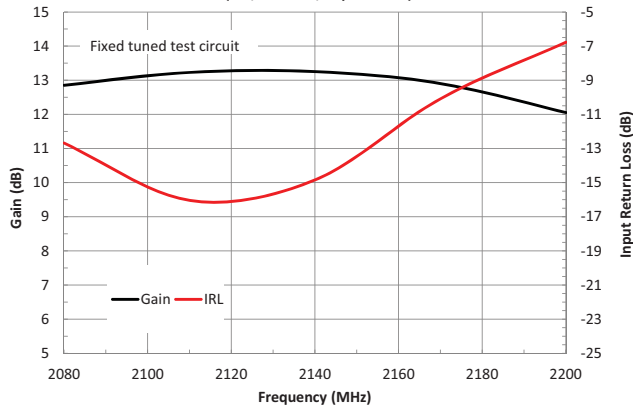
**Input Return Loss vs. Output Power (f = 2140MHz)**  
(Pulsed 10% duty cycle, 10uS, Vd = 48V, Idq = 130mA)



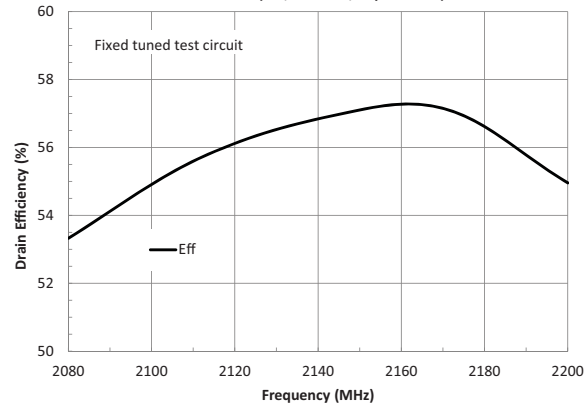
**Small Signal Performance vs. Frequency, Pout = 30dBm**  
(Vd = 48V, Idq = 130mA)

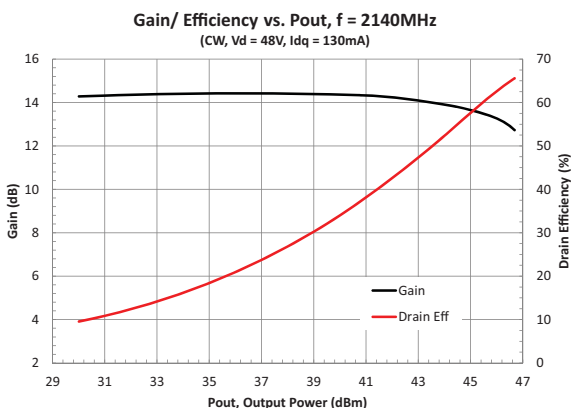
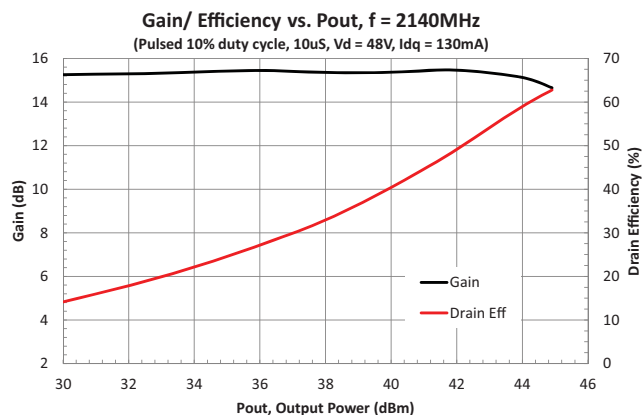
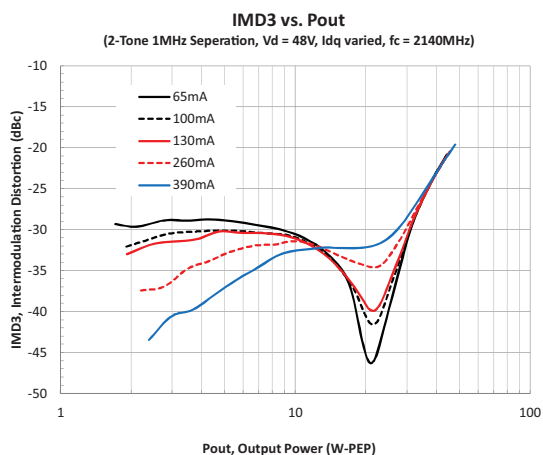
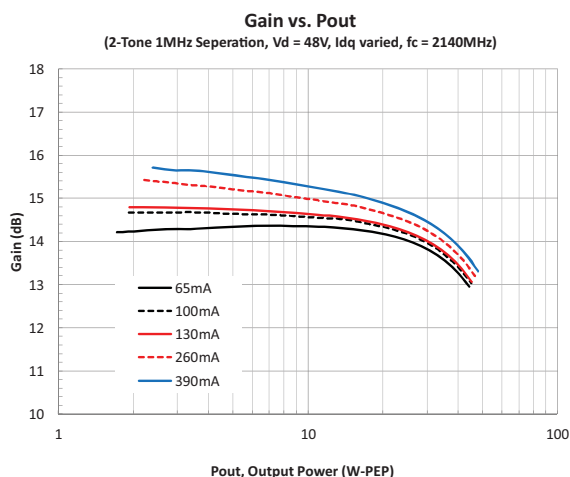
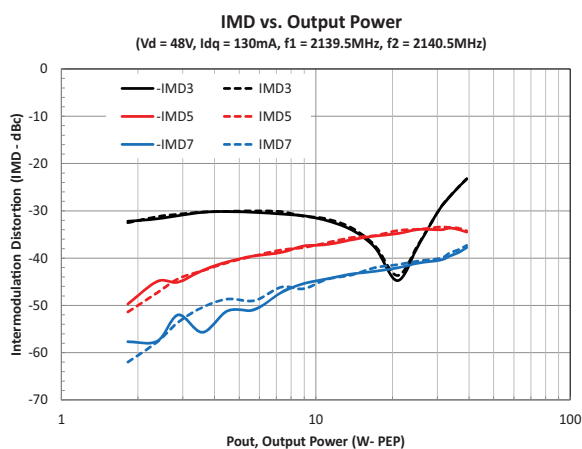


**Gain/IRL vs. Frequency, Pout = 46dBm**  
(CW, Vd = 48V, Idq = 130mA)

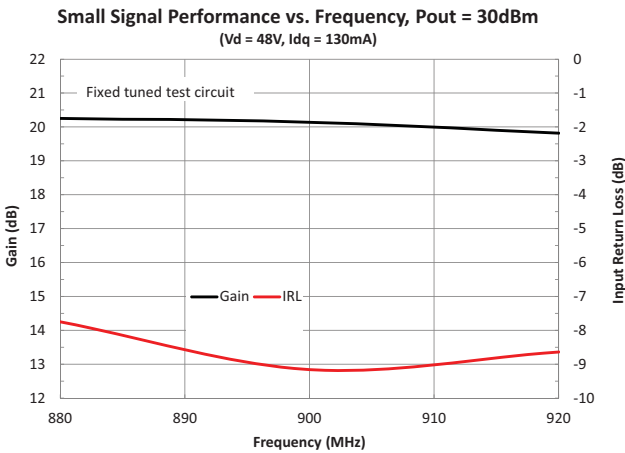
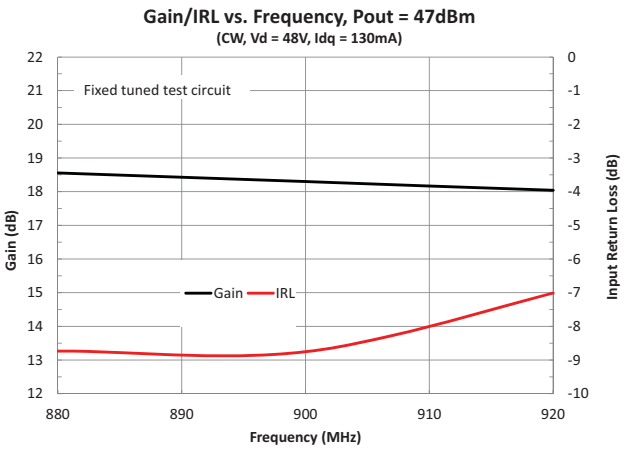
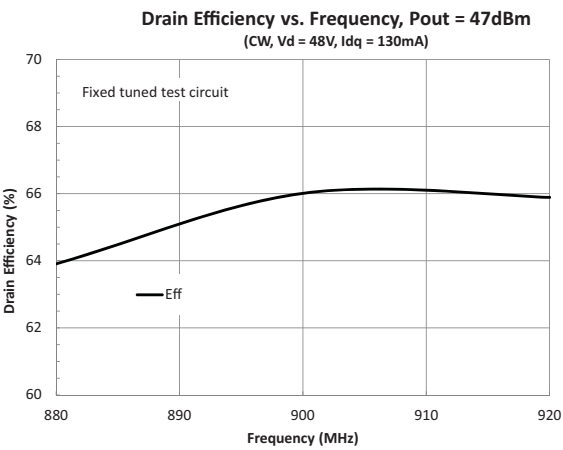
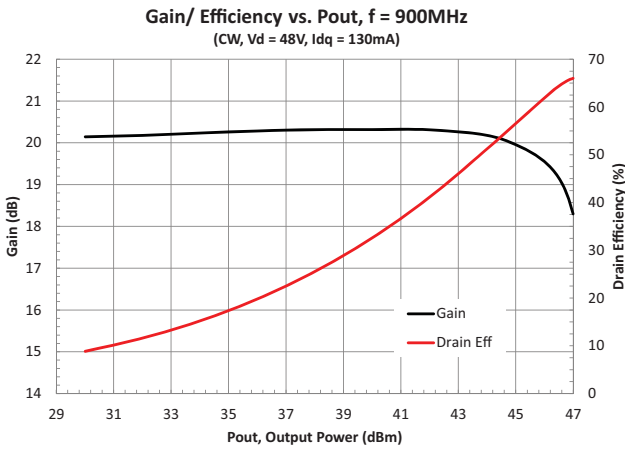


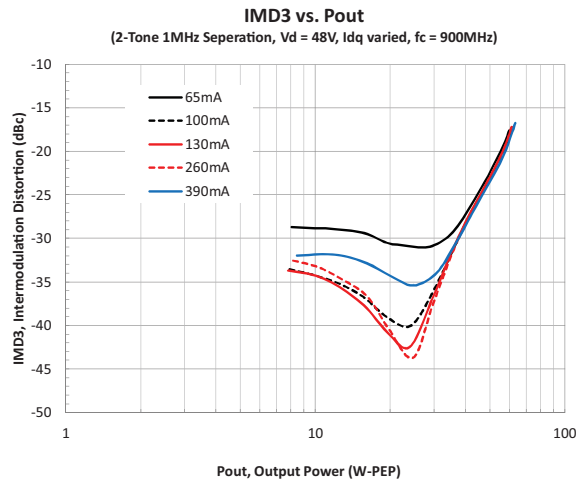
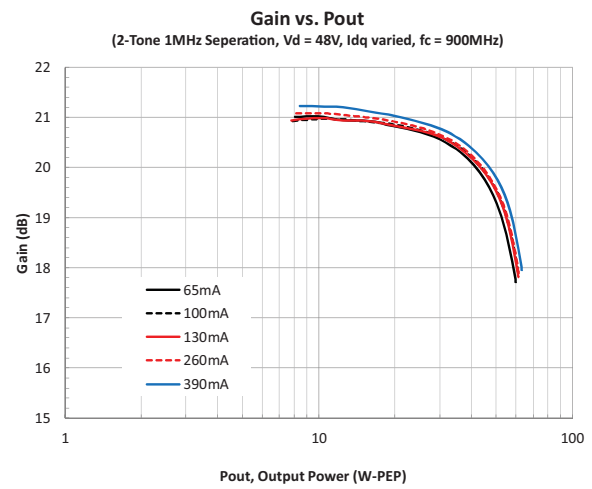
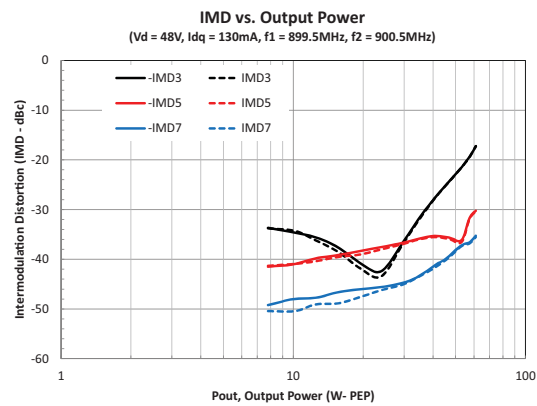
**Drain Efficiency vs. Frequency, Pout = 46dBm**  
(CW, Vd = 48V, Idq = 130mA)



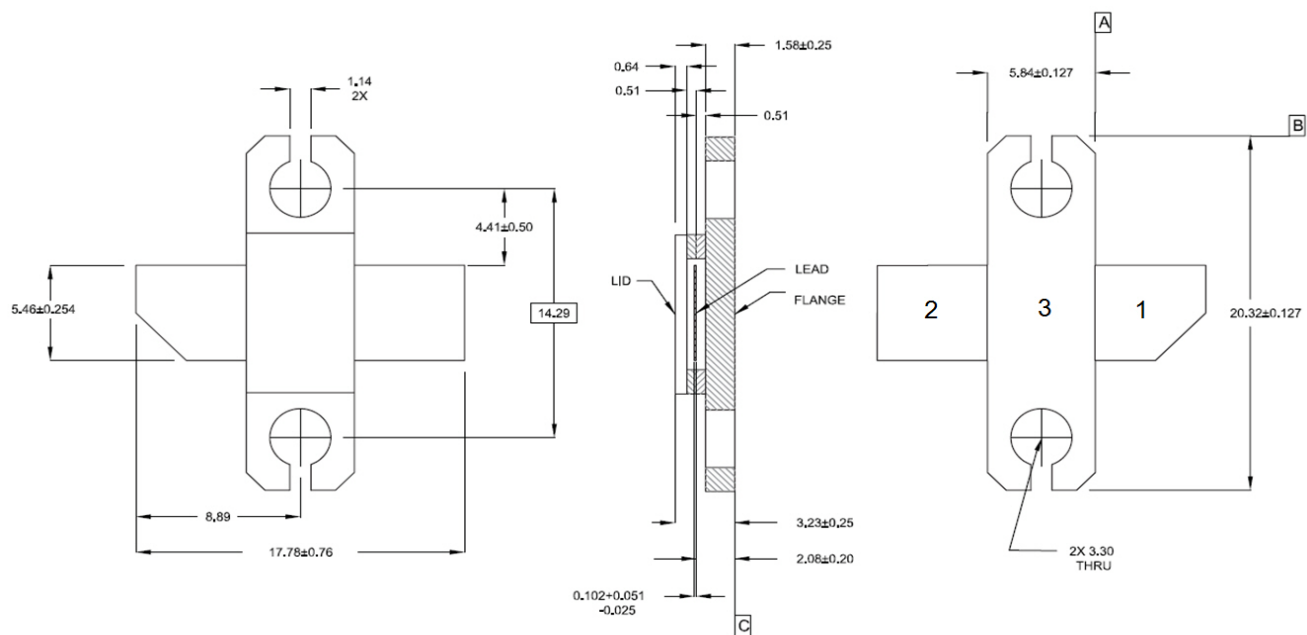


Typical Performance in standard 900MHz fixed tuned test fixture  
(CW, T = 25 °C, unless noted)





Package Drawing  
(Package Style: Flanged Ceramic)



Package Style: Flanged Ceramic

| Pin | Function | Description          |
|-----|----------|----------------------|
| 1   | Gate     | Gate - VG RF Input   |
| 2   | Drain    | Drain - VD RF Output |
| 3   | Source   | Source - Ground Base |

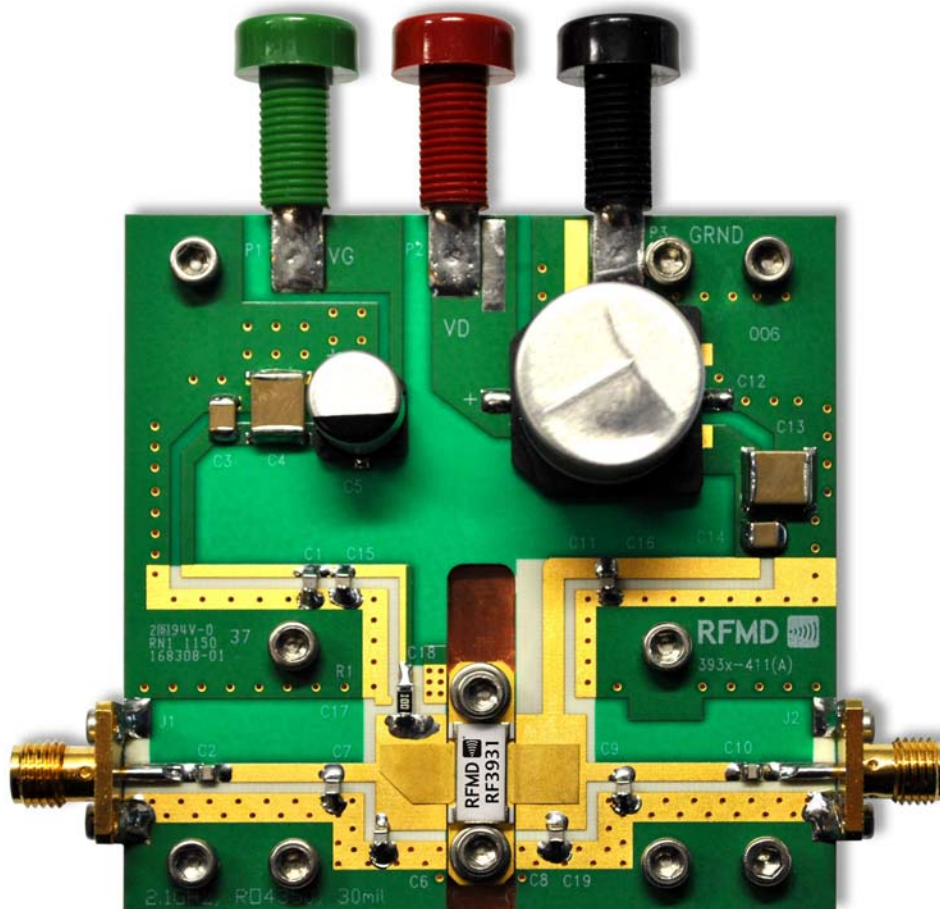
## Bias Instruction for RF3931 Evaluation Board

ESD Sensitive Material. Please use proper ESD precautions when handling devices of evaluation board.

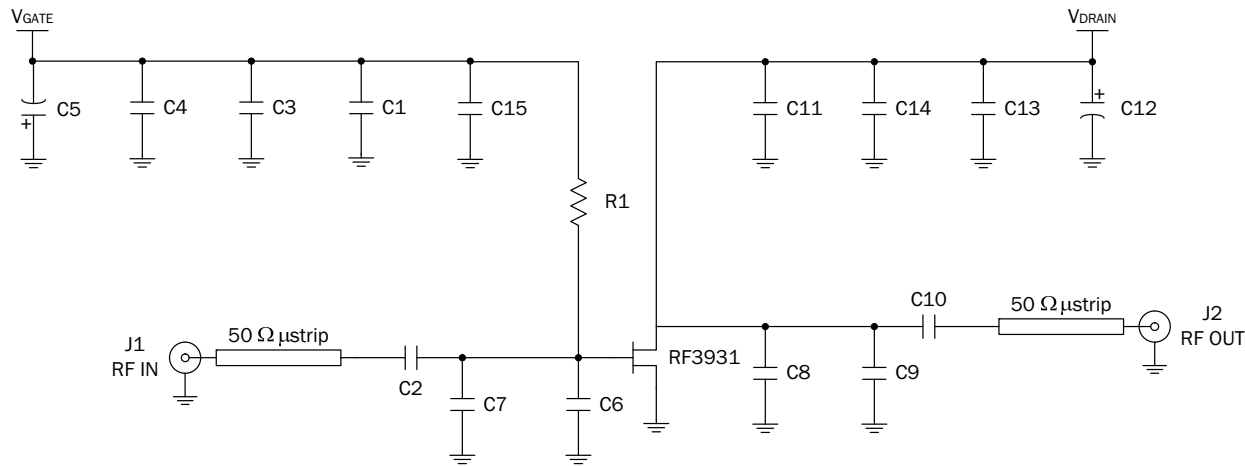
Evaluation board requires additional external fan cooling.

Connect all supplies before powering up the evaluation board.

1. Connect RF cables at RF<sub>IN</sub> and RF<sub>OUT</sub>.
2. Connect ground to the ground supply terminal, and ensure that both the V<sub>G</sub> and V<sub>D</sub> grounds are also connected to this ground terminal.
3. Apply -8V to V<sub>G</sub>.
4. Apply 48V to V<sub>D</sub>.
5. Increase V<sub>G</sub> until drain current reaches 130mA desired bias point.
6. Turn on the RF input.



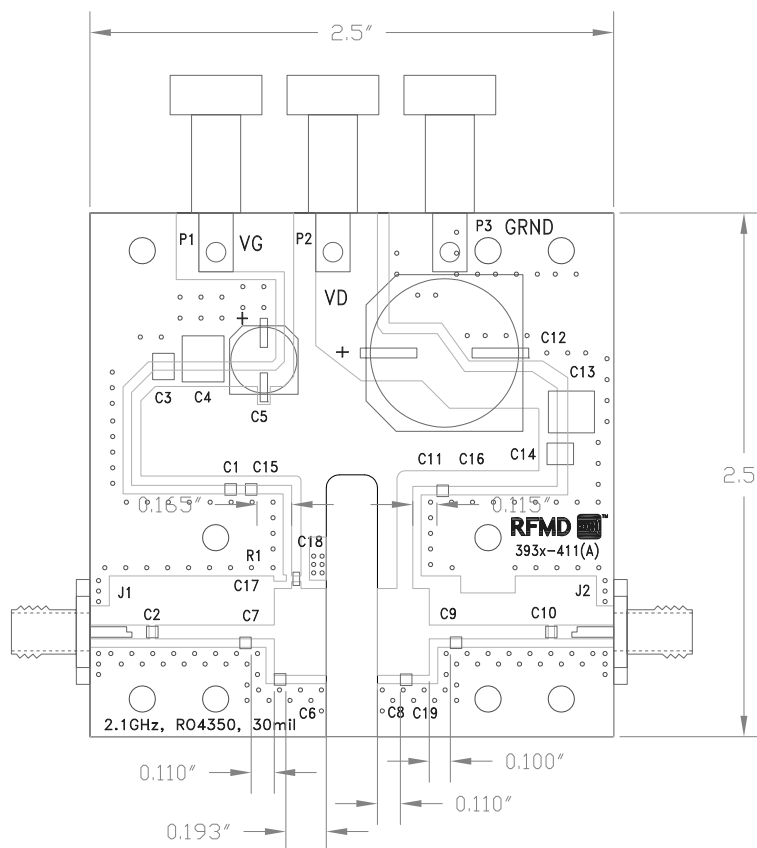
2.14GHz Evaluation Board Schematic



2.14GHz Evaluation Board Bill of Materials

| Component          | Value                           | Manufacturer | Part Number        |
|--------------------|---------------------------------|--------------|--------------------|
| C1, C2, C10, C11   | 33pF                            | ATC          | ATC800A330JT       |
| C3,C14             | 0.1μF                           | Murata       | GRM32NR72A104KA01L |
| C4,C13             | 4.7μF                           | Murata       | GRM55ER72A475KA01L |
| C5                 | 100μF                           | Panasonic    | ECE-V1HA101UP      |
| C6                 | 2.2pF                           | ATC          | ATC800A2R2BT       |
| C7                 | 0.7pF                           | ATC          | ATC800A0R7BT       |
| C8                 | 1.0pF                           | ATC          | ATC800A1R0BT       |
| C9                 | 3.3pF                           | ATC          | ATC800A3R3BT       |
| C12                | 100μF                           | Panasonic    | EEV-TG2A101M       |
| C15                | 10pF                            | ATC          | ATC800A100JT       |
| R1                 | 10Ω                             | Panasonic    | ERJ-8GEYJ100V      |
| C16, C17, C18, C19 | Not used                        | -            | -                  |
| PCB                | R04350, 0.030" thick dielectric | Rogers       | -                  |

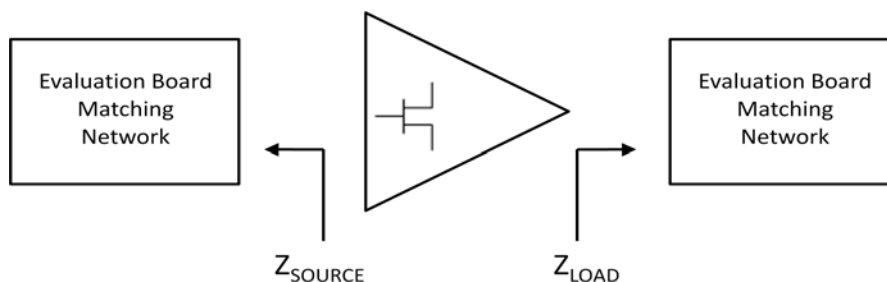
## 2.14GHz Evaluation Board Layout



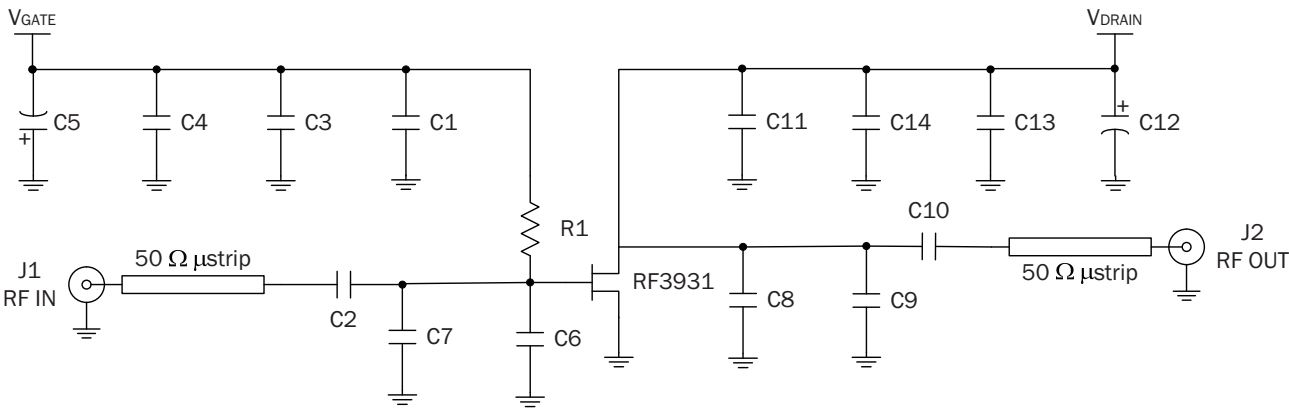
## Device Impedances

| Frequency (MHz) | Z Source ( $\Omega$ ) | Z Load ( $\Omega$ ) |
|-----------------|-----------------------|---------------------|
| 2110            | 2.6 - j3.1            | 6.5 + j5.8          |
| 2140            | 2.5 - j2.8            | 6.7 + j6.6          |
| 2170            | 2.4 - j2.5            | 7.0 + j7.4          |

**Note:** Device impedances reported are the measured evaluation board impedances chosen for a trade off of efficiency, peak power, and linearity performance across the entire frequency bandwidth.



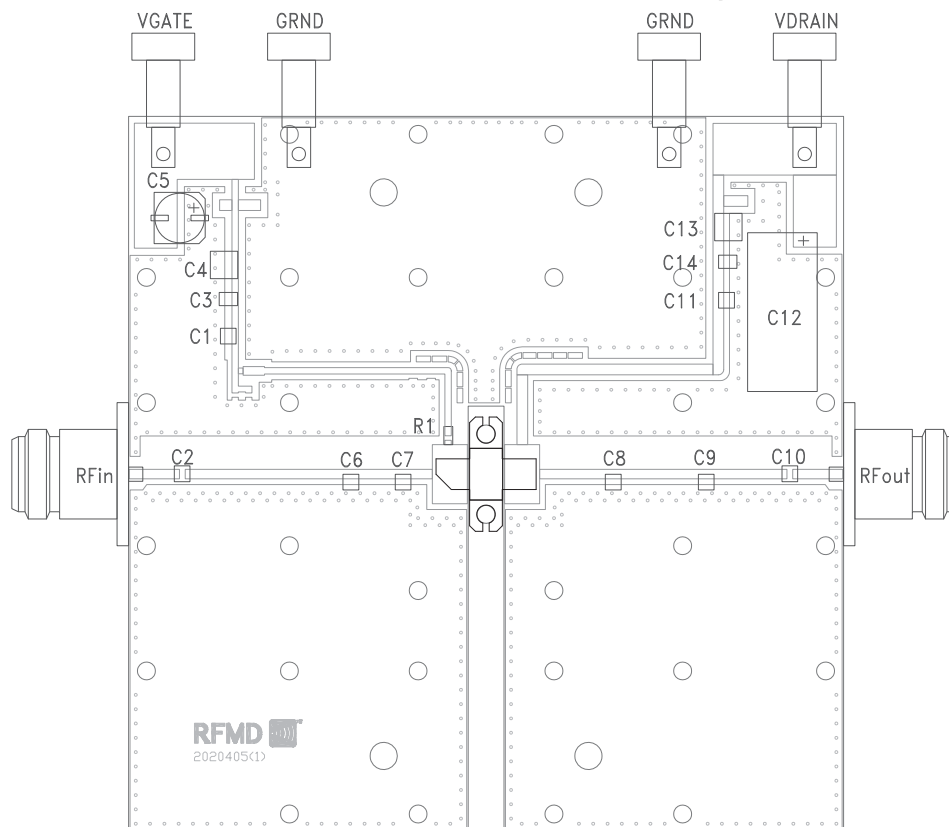
900MHz Evaluation Board Schematic



900MHz Evaluation Board Bill of Materials

| Component        | Value | Manufacturer | Part Number        |
|------------------|-------|--------------|--------------------|
| C1, C2, C10, C11 | 68pF  | ATC          | ATC800B680JT       |
| C3,C14           | 0.1μF | Murata       | GRM32NR72A104KA01L |
| C4,C13           | 4.7μF | Murata       | GRM55ER72A475KA01L |
| C5               | 100μF | Panasonic    | ECE-V1HA101UP      |
| C6               | 12pF  | ATC          | ATC800B120         |
| C7               | 5.6pF | ATC          | ATC800B5R6         |
| C8               | 6.8pF | ATC          | ATC800B6R8         |
| C9               | 2.0pF | ATC          | ATC800B2R0         |
| C12              | 330μF | Panasonic    | EEU-FC2A331        |
| R1               | 10Ω   | Panasonic    | ERJ-8GEYJ100V      |

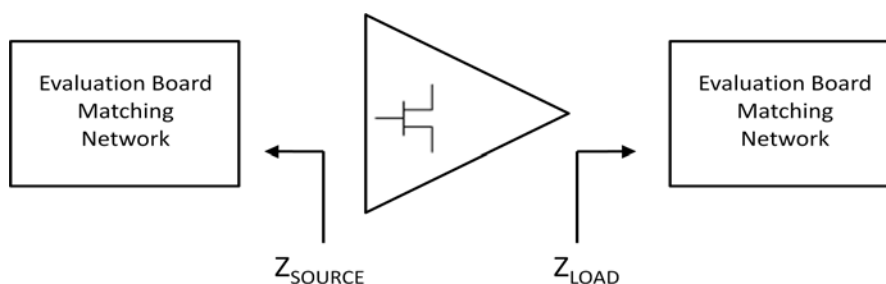
## 900MHz Evaluation Board Layout



## Device Impedances

| Frequency (MHz) | Z Source ( $\Omega$ ) | Z Load ( $\Omega$ ) |
|-----------------|-----------------------|---------------------|
| 880             | $4.2 + j9.0$          | $12.9 + j14.2$      |
| 900             | $4.3 + j10.0$         | $13.6 + j15.1$      |
| 920             | $4.4 + j11.3$         | $14.4 + j16.0$      |

**Note:** Device impedances reported are the measured evaluation board impedances chosen for a trade off of efficiency, peak power, and linearity performance across the entire frequency bandwidth.



Loadpull contours available on RFMD website.

**Device Handling/Environmental Conditions**

GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.

**GaN HEMT Capacitances**

The physical structure of the GaN HEMT results in three terminal capacitors similar to other FET technologies. These capacitances exist across all three terminals of the device. The physical manufactured characteristics of the device determine the value of the  $C_{DS}$  (drain to source),  $C_{GS}$  (gate to source) and  $C_{GD}$  (gate to drain). These capacitances change value as the terminal voltages are varied. RFMD presents the three terminal capacitances measured with the gate pinched off ( $V_{GS} = -8V$ ) and zero volts applied to the drain. During the measurement process, the parasitic capacitances of the package that holds the amplifier is removed through a calibration step. Any internal matching is included in the terminal capacitance measurements. The capacitance values presented in the typical characteristics table of the device represent the measured input ( $C_{ISS}$ ), output ( $C_{OSS}$ ), and reverse ( $C_{RSS}$ ) capacitance at the stated bias voltages. The relationship to three terminal capacitances is as follows:

$$C_{ISS} = C_{GD} + C_{GS}$$

$$C_{OSS} = C_{GD} + C_{DS}$$

$$C_{RSS} = C_{GD}$$

**DC Bias**

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts  $V_{GS}$  the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. RFMD recommends applying  $V_{GS} = -5V$  before applying any  $V_{DS}$ .

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current ( $I_{DQ}$ ) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance trade off.

**Mounting and Thermal Considerations**

The thermal resistance provided as  $R_{TH}$  (junction to case) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heatsink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200 °C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heatsinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.