



dsPIC33CH512MP508 FAMILY

48/64/80-Pin Dual Core, 16-Bit Digital Signal Controllers with High-Resolution PWM and CAN Flexible Data (FD)

Operating Conditions

- 3V to 3.6V, -40°C to +125°C:
 - Master: Up to 100 MIPS @ 200 MHz
 - Slave: Up to 120 MIPS @ 240 MHz

Core: Dual 16-Bit dsPIC33CH CPU

- Master/Slave Core Operation
- Independent Peripherals for Master Core and Slave Core
- Configurable Shared Resources for Master Core and Slave Core
- Master Core with 256-512 Kbytes of Program Flash with ECC and 32-48K Data RAM with BIST
- Slave Core with 72 Kbytes of Program RAM (PRAM) with ECC and 16K Data RAM with BIST
- Fast 6-Cycle Divide
- Live Update
- Message Boxes and FIFO to Communicate Between Master and Slave (MSI)
- Code Efficient (C and Assembly) Architecture
- 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle, Mixed-Sign MUL Plus Hardware Divide
- 32-Bit Multiply Support
- Five Sets of Interrupt Context Selected Registers per Core for Fast Interrupt Response
- Zero Overhead Looping

Clock Management

- Internal Oscillator
- Programmable PLLs and Oscillator Clock Sources
- Master Core Reference Clock Output
- Slave Core Reference Clock Output
- Fail-Safe Clock Monitor (FSCM)
- Fast Wake-up and Start-up
- Backup Internal Oscillator
- LPRC Oscillator

Power Management

- Low-Power Management Modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset

High-Resolution PWM with Fine Edge Placement

- Up to 12 PWM Channels:
 - 4 channels for Master Core
 - 8 channels for Slave Core
- 250 ps PWM Resolution
- Applications include:
 - DC/DC Converters
 - AC/DC power supplies
 - Uninterruptable Power Supply (UPS)
 - Motor control: BLDC, PMSM, SR, ACIM

Timers/Output Compare/Input Capture

- 2 General Purpose 16-Bit Timers:
 - 1 each for Master and Slave cores
- Peripheral Trigger Generator (PTG) Module:
 - 1 module for Master core
 - Slave can interrupt on select PTG sources
 - Useful for automating complex sequences
- 12 SCCP Modules:
 - 8 modules for Master core
 - 4 modules for Slave core
 - Timer, Capture/Compare and PWM modes
 - 16 or 32-bit time base
 - 16 or 32-bit capture
 - 4-deep capture buffer
 - Fully asynchronous operation, available in Sleep modes

Advanced Analog Features

- 4 ADC Modules:
 - 1 module for Master core
 - 3 modules for Slave core
 - 12-bit, 4 Msps ADC
 - Up to 18 conversion channels
 - 250 ns conversion latency
 - Capacitive Voltage Divider (CVD) for touch sensing
- 4 DAC/Analog Comparator Modules:
 - 1 module for Master core
 - 3 modules for Slave core
 - 12-bit DACs with hardware slope compensation
 - 15 ns analog comparators
- 3 PGA Modules:
 - 3 modules for Slave core
 - Can be read by Master Core ADC
- Shared DAC/Analog Output:
 - DAC/analog comparator outputs
 - PGA outputs

Communication Interfaces

- 3 UART Modules:
 - 2 modules for Master core
 - 1 module for Slave core
 - Support for LIN/J2602 protocols and IrDA®
- Three 4-Wire SPI/I²S Modules:
 - 2 modules for Master core
 - 1 module for Slave core
- 2 CAN Flexible Data (FD) Modules for the Master Core
- 3 I²C Modules:
 - 2 modules for Master core
 - 1 module for Slave core
 - Support for SMBus
- PPS to Allow Function Remap
- Programmable Cyclic Redundancy Check (CRC) for the Master
- 2 SENT Modules for Master Core

Direct Memory Access (DMA)

- 8 DMA Channels:
 - 6 channels for Master core
 - 2 channels for Slave core

Debugger Development Support

- In-Circuit and In-Application Programming
- Simultaneous Debugging Support for Master and Slave
- Master Only Debug and Slave Only Debug Support
- Master with 3 Complex, 5 Simple Breakpoints and Slave with 1 Complex, 2 Simple Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace Buffer and Run-Time Watch

Safety Features

- DMT (Deadman Timer)
- ECC (Error Correcting Code)
- WDT (Watchdog Timer)
- CodeGuard™ Security with Flash PED (Program Erase Disable)
- CRC (Cyclic Redundancy Check)
- RAM BIST (Built-In Self Test)

TABLE 1: MASTER AND SLAVE CORE FEATURES

Feature	Master	Slave	Shared
Core Frequency	100 MIPS @ 200 MHz	120 MIPS @ 240 MHz	—
Program Memory	256-512 Kbytes	72 Kbytes (PRAM)	—
Internal Data RAM	32-48 Kbytes	16 Kbytes	—
16-Bit Timer	1	1	—
DMA	6	2	—
SCCP (Capture/Compare/Timer)	8	4	—
UART	2	1	—
SPI/I ² S	2	1	—
I ² C	2	1	—
CAN FD	2	—	—
SENT	2	—	—
CRC	1	—	—
CVD	1	1	—
QEI	1	1	—
PTG	1	—	—
CLC	4	4	—
16-Bit High-Resolution PWM	4	8	—
12-Bit ADC	1	3	—
Digital Comparator	4	4	—
12-Bit DAC/Analog CMP Module	1	3	—
Watchdog Timer	1	1	—
Deadman Timer	1	1	—
Input/Output	69	69	69
Simple Breakpoints	5	2	—
PGAs ⁽¹⁾	—	3	3
DAC Output Buffer	—	—	1
Oscillator	—	—	1

Note 1: Slave owns the peripheral/feature, but it is shared with the Master.

dsPIC33CH512MP50X/20X PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in [Table 2](#) and [Table 3](#). The following pages show their pinout diagrams.

TABLE 2: dsPIC33CH512MP508 MOTOR CONTROL/POWER SUPPLY FAMILIES

Product	Core	Pins	Flash/(PRAM)	Data RAM	ADC Modules	ADC Channels	CVD Channels	16-Bit Timers	SCCP	CAN FD	SENT	UART	SPI/I ² S	I ² C	QEI	CLC	PTG	CRC	PWM (High Resolution)	12-Bit DAC/Analog CMP	PGA	Current Bias Source	REFO
Devices with CAN FD																							
dsPIC33CH256MP505	Master	48	256K	32K	1	16	11	1	8	2	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		(72K)	16K	3	15	10	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH512MP505	Master	48	512K	48K	1	16	11	1	8	2	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		(72K)	16K	3	15	10	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH256MP506	Master	64	256K	32K	1	16	11	1	8	2	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		(72K)	16K	3	18	13	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH512MP506	Master	64	512K	48K	1	16	11	1	8	2	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		(72K)	16K	3	18	13	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH256MP508	Master	80	256K	32K	1	16	11	1	8	2	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		(72K)	16K	3	18	13	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH512MP508	Master	80	512K	48K	1	16	11	1	8	2	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		(72K)	16K	3	18	13	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1

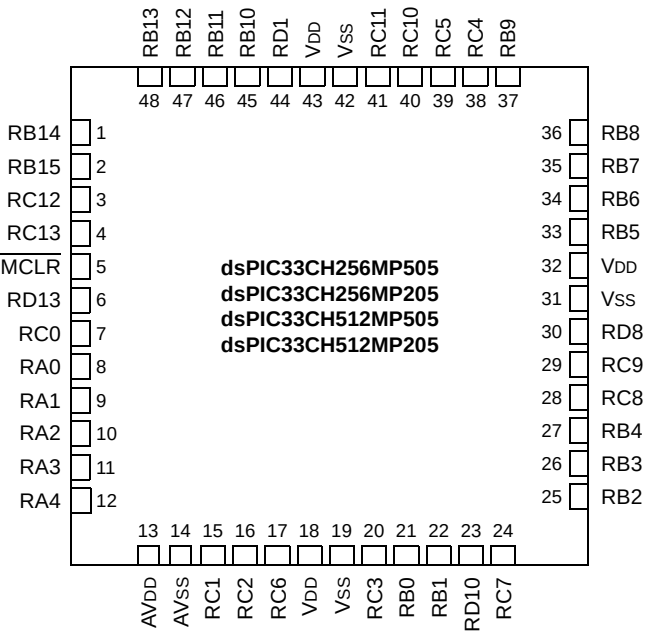
TABLE 3: dsPIC33CH512MP208 MOTOR CONTROL/POWER SUPPLY FAMILIES WITH NO CAN FD

Product	Core	Pins	Flash/(PRAM)	Data RAM	ADC Modules	ADC Channels	CVD Channels	16-Bit Timers	SCCP	CAN FD	SENT	UART	SPI/I ² S	I ² C	QEI	CLC	PTG	CRC	PWM (High Resolution)	12-Bit DAC/Analog CMP	PGA	Current Bias Source	REFO
Devices with No CAN FD																							
dsPIC33CH256MP205	Master	48	256K	32K	1	16	11	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		(72K)	16K	3	15	10	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH512MP205	Master	48	512K	48K	1	16	11	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		(72K)	16K	3	15	10	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH256MP206	Master	64	256K	32K	1	16	11	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		(72K)	16K	3	18	13	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH512MP206	Master	64	512K	48K	1	16	11	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		(72K)	16K	3	18	13	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH256MP208	Master	80	256K	32K	1	16	11	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		(72K)	16K	3	18	13	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH512MP208	Master	80	512K	48K	1	16	11	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		(72K)	16K	3	18	13	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1

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Pin Diagrams

48-Pin UQFN 6x6x0.5 mm/TQFP 7x7x1 mm



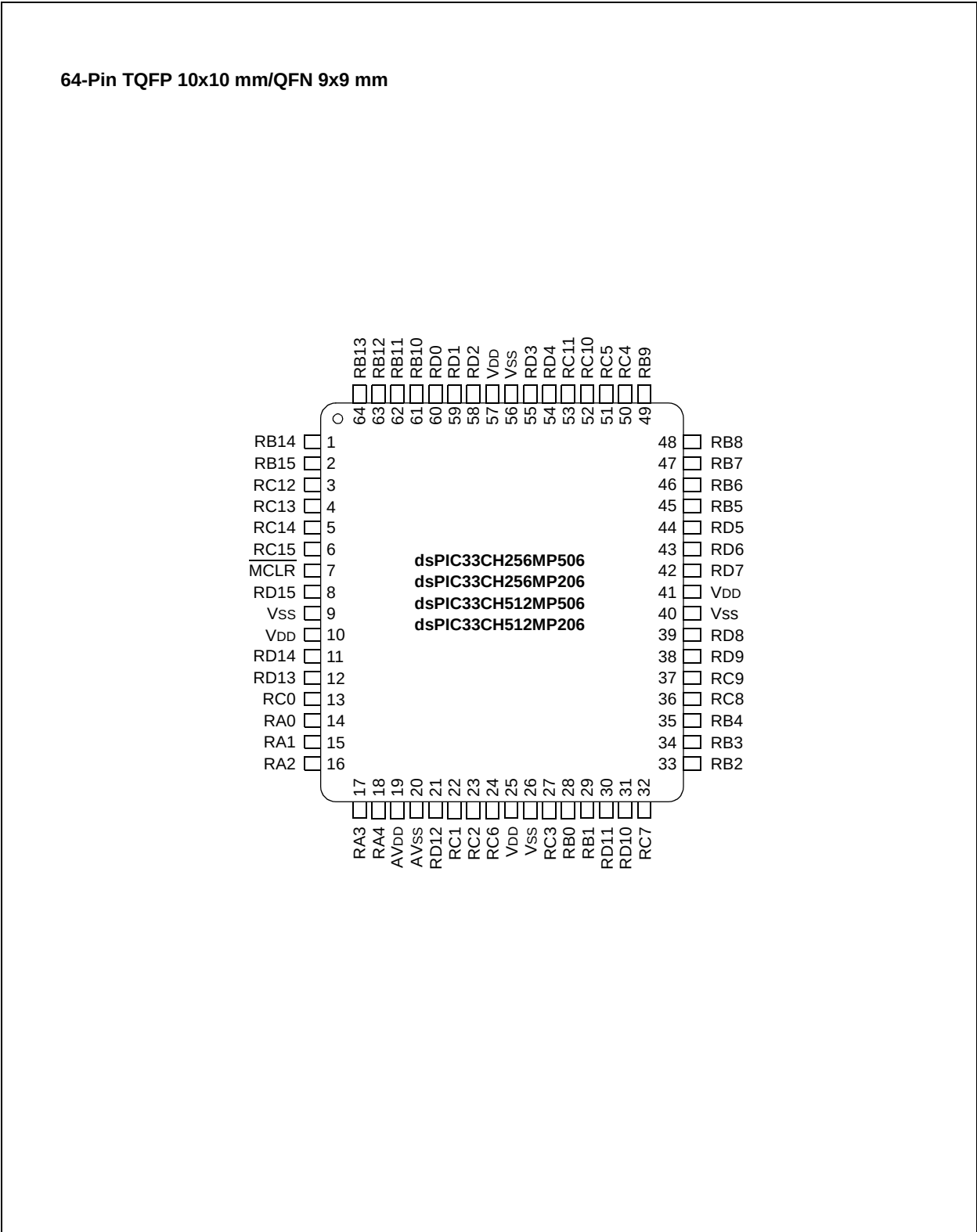
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TABLE 4: 48-PIN UQFN/TQFP

Pin #	Master Core	Slave Core
1	RP46/PWM1H/RB14	S1RP46/S1PWM6L/S1RB14
2	RP47/PWM1L/RB15	S1RP47/S1PWM6H/S1RB15
3	RP60/RC12	S1RP60/S1PWM3H/S1RC12
4	RP61/RC13	S1RP61/S1PWM3L/S1RC13
5	MCLR	MCLR
6	RD13	S1ANN0/S1PGA1N2/S1RD13
7	AN12/IBIAS3/RP48/RC0	S1AN10/S1RP48/S1RC0
8	AN0/CMP1A/RA0	S1RA0
9	AN1/RA1	S1AN15/S1RA1
10	AN2/RA2	S1AN16/S1RA2
11	AN3/IBIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
12	AN4/IBIAS1/RA4	S1MCLR3/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
13	AVDD	AVDD
14	AVSS	AVSS
15	AN13/ISRC0/RP49/RC1	S1ANA1/S1RP49/S1RC1
16	AN14/ISRC1/RP50/RC2	S1ANA0/S1RP50/S1RC2
17	RP54/RC6	S1AN11/S1CMP1B/S1RP54/S1RC6
18	VDD	VDD
19	VSS	VSS
20	CMP1B/RP51/RC3	S1AN8/S1CMP3B/S1RP51/S1RC3
21	OSCI/CLKI/AN5/RP32/RB0	S1AN5/S1RP32/S1RB0
22	OSCO/CLKO/AN6/IBIAS2/RP33/RB1	S1AN4/S1RP33/S1RB1
23	ISRC3/RD10	S1AN13/S1CMP2B/S1RD10
24	AN15/ISRC2/RP55/RC7	S1AN12/S1RP55/S1RC7
25	DACOUT/AN7/CMP1D/RP34/INT0/RB2	S1MCLR2/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/S1RP34/S1INT0/S1RB2
26	PGD2/AN8/RP35/RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/S1RP35/S1RB3
27	PGC2/RP36/RB4	S1PGC2/S1AN9/S1RP36/S1PWM5L/S1RB4
28	RP56/ASDA1/SCK2/RC8	S1RP56/S1ASDA1/S1SCK1/S1RC8
29	RP57/ASCL1/SDI2/RC9	S1RP57/S1ASCL1/S1SDI1/S1RC9
30	SDO2/PCI19/RD8	S1SDO1/S1PCI19/S1RD8
31	VSS	VSS
32	VDD	VDD
33	PGD3/RP37/SDA2/RB5	S1PGD3/S1RP37/S1RB5
34	PGC3/RP38/SCL2/RB6	S1PGC3/S1RP38/S1RB6
35	TDO/AN9/RP39/RB7	S1MCLR1/S1AN6/S1RP39/S1PWM5H/S1RB7
36	PGD1/AN10/RP40/SCL1/RB8	S1PGD1/S1AN7/S1RP40/S1SCL1/S1RB8
37	PGC1/AN11/RP41/SDA1/RB9	S1PGC1/S1RP41/S1SDA1/S1RB9
38	RP52/RC4	S1RP52/S1PWM2H/S1RC4
39	RP53/RC5	S1RP53/S1PWM2L/S1RC5
40	RP58/RC10	S1RP58/S1PWM1H/S1RC10
41	RP59/RC11	S1RP59/S1PWM1L/S1RC11
42	VSS	VSS
43	VDD	VDD
44	RP65/RD1	S1RP65/S1PWM4H/S1RD1
45	TMS/RP42/PWM3H/RB10	S1RP42/S1PWM8L/S1RB10
46	TCK/RP43/PWM3L/RB11	S1RP43/S1PWM8H/S1RB11
47	TDI/RP44/PWM2H/RB12	S1RP44/S1PWM7L/S1RB12
48	RP45/PWM2L/RB13	S1RP45/S1PWM7H/S1RB13

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Pin Diagrams (Continued)



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TABLE 5: 64-PIN TQFP/QFN

Pin #	Master Core	Slave Core
1	RP46/PWM1H/RB14	S1RP46/S1RB14
2	RP47/PWM1L/RB15	S1RP47/S1RB15
3	RP60/PWM4H/RC12	S1RP60/S1RC12
4	RP61/PWM4L/RC13	S1RP61/S1RC13
5	RP62/RC14	S1RP62/S1PWM7H/S1RC14
6	RP63/RC15	S1RP63/S1PWM7L/S1RC15
7	MCLR	MCLR
8	PCI22/RD15	S1PCI22/S1RD15
9	Vss	Vss
10	VDD	VDD
11	PCI21/RD14	S1ANN1/S1PGA2N2/S1PCI21/S1RD14
12	RD13	S1ANN0/S1PGA1N2/S1RD13
13	AN12/BIAS3/RP48/RC0	S1AN10/S1RP48/S1RC0
14	AN0/CMP1A/RA0	S1RA0
15	AN1/RA1	S1AN15/S1RA1
16	AN2/RA2	S1AN16/S1RA2
17	AN3/BIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
18	AN4/BIAS1/RA4	S1MCLR3/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
19	AVDD	AVDD
20	AVss	AVss
21	RD12	S1AN14/S1PGA2P2/S1RD12
22	AN13/ISRC0/RP49/RC1	S1ANA1/S1RP49/S1RC1
23	AN14/ISRC1/RP50/RC2	S1ANA0/S1RP50/S1RC2
24	RP54/RC6	S1AN11/S1CMP1B/S1RP54/S1RC6
25	VDD	VDD
26	Vss	Vss
27	CMP1B/RP51/RC3	S1AN8/S1CMP3B/S1RP51/S1RC3
28	OSCI/CLKI/AN5/RP32/RB0	S1AN5/S1RP32/S1RB0
29	OSCO/CLKO/AN6/BIAS2/RP33/RB1	S1AN4/S1RP33/S1RB1
30	RD11	S1AN17/S1PGA1P2/S1RD11
31	ISRC3/RD10	S1AN13/S1CMP2B/S1RD10
32	AN15/ISRC2/RP55/RC7	S1AN12/S1RP55/S1RC7
33	DACOUT/AN7/CMP1D/RP34/INT0/RB2	S1MCLR2/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/S1RP34/S1INT0/S1RB2
34	PGD2/AN8/RP35/RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/S1RP35/S1RB3
35	PGC2/RP36/RB4	S1PGC2/S1AN9/S1RP36/S1PWM5L/S1RB4
36	RP56/ASDA1/SCK2/RC8	S1RP56/S1ASDA1/S1SCK1/S1RC8
37	RP57/ASCL1/SDI2/RC9	S1RP57/S1ASCL1/S1SDI1/S1RC9
38	PCI20/RD9	S1PCI20/S1RD9
39	SDO2/PCI19/RD8	S1SDO1/S1PCI19/S1RD8
40	Vss	Vss
41	VDD	VDD
42	RP71/RD7	S1RP71/S1PWM8H/S1RD7
43	RP70/RD6	S1RP70/S1PWM6H/S1RD6
44	RP69/RD5	S1RP69/S1PWM6L/S1RD5
45	PGD3/RP37/SDA2/RB5	S1PGD3/S1RP37/S1RB5
46	PGC3/RP38/SCL2/RB6	S1PGC3/S1RP38/S1RB6
47	TDO/AN9/RP39/RB7	S1MCLR1/S1AN6/S1RP39/S1PWM5H/S1RB7
48	PGD1/AN10/RP40/SCL1/RB8	S1PGD1/S1AN7/S1RP40/S1SCL1/S1RB8
49	PGC1/AN11/RP41/SDA1/RB9	S1PGC1/S1RP41/S1SDA1/S1RB9
50	RP52/RC4	S1RP52/S1PWM2H/S1RC4
51	RP53/RC5	S1RP53/S1PWM2L/S1RC5

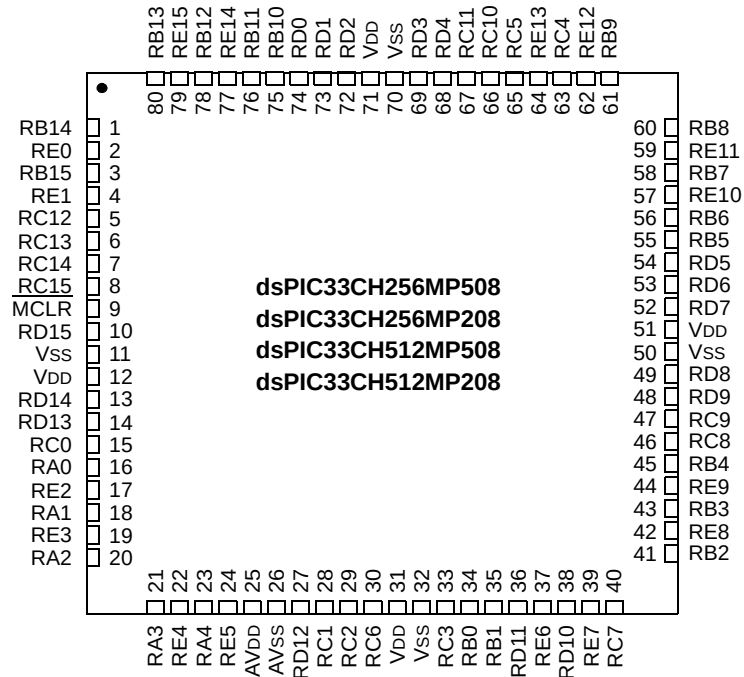
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TABLE 5: 64-PIN TQFP/QFN (CONTINUED)

Pin #	Master Core	Slave Core
52	RP58/RC10	S1RP58/S1PWM1H/S1RC10
53	RP59/RC11	S1RP59/S1PWM1L/S1RC11
54	RP68/RD4	S1RP68/S1PWM3H/S1RD4
55	RP67/RD3	S1RP67/S1PWM3L/S1RD3
56	Vss	Vss
57	VDD	VDD
58	RP66/RD2	S1RP66/S1PWM8L/S1RD2
59	RP65/RD1	S1RP65/S1PWM4H/S1RD1
60	RP64/RD0	S1RP64/S1PWM4L/S1RD0
61	TMS/RP42/PWM3H/RB10	S1RP42/S1RB10
62	TCK/RP43/PWM3L/RB11	S1RP43/S1RB11
63	TDI/RP44/PWM2H/RB12	S1RP44/S1RB12
64	RP45/PWM2L/RB13	S1RP45/S1RB13

Pin Diagrams (Continued)

80-Pin TQFP 12x12 mm



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TABLE 6: 80-PIN TQFP

Pin #	Master Core	Slave Core
1	RP46/PWM1H/RB14	S1RP46/S1RB14
2	RE0	S1RE0
3	RP47/PWM1L/RB15	S1RP47/S1RB15
4	RE1	S1RE1
5	RP60/PWM4H/RC12	S1RP60/S1RC12
6	RP61/PWM4L/RC13	S1RP61/S1RC13
7	RP62/RC14	S1RP62/S1PWM7H/S1RC14
8	RP63/RC15	S1RP63/S1PWM7L/S1RC15
9	MCLR	MCLR
10	PCI22/RD15	S1PCI22/S1RD15
11	Vss	Vss
12	VDD	VDD
13	PCI21/RD14	S1ANN1/S1PGA2N2/S1PCI21/S1RD14
14	RD13	S1ANN0/S1PGA1N2/S1RD13
15	AN12/IBIAS3/RP48/RC0	S1AN10/S1RP48/S1RC0
16	AN0/CMP1A/RA0	S1RA0
17	RE2	S1RE2
18	AN1/RA1	S1AN15/S1RA1
19	RE3	S1RE3
20	AN2/RA2	S1AN16/S1RA2
21	AN3/IBIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
22	RE4	S1RE4
23	AN4/IBIAS1/RA4	S1MCLR3/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
24	RE5	S1RE5
25	AVDD	AVDD
26	AVss	AVss
27	RD12	S1AN14/S1PGA2P2/S1RD12
28	AN13/ISRC0/RP49/RC1	S1ANA1/S1RP49/S1RC1
29	AN14/ISRC1/RP50/RC2	S1ANA0/S1RP50/S1RC2
30	RP54/RC6	S1AN11/S1CMP1B/S1RP54/S1RC6
31	VDD	VDD
32	Vss	Vss
33	CMP1B/RP51/RC3	S1AN8/S1CMP3B/S1RP51/S1RC3
34	OSCI/CLKI/AN5/RP32/RB0	S1AN5/S1RP32/S1RB0
35	OSCO/CLKO/AN6/IBIAS2/RP33/RB1	S1AN4/S1RP33/S1RB1
36	RD11	S1AN17/S1PGA1P2/S1RD11
37	RE6	S1PGA3N2/S1RE6
38	ISRC3/RD10	S1AN13/S1CMP2B/S1RD10
39	RE7	S1RE7
40	AN15/ISRC2/RP55/RC7	S1AN12/S1RP55/S1RC7
41	DACOUT/AN7/CMP1D/RP34/INT0/RB2	S1MCLR2/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/S1RP34/S1INT0/S1RB2
42	RE8	S1RE8
43	PGD2/AN8/RP35/RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/S1RP35/S1RB3

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TABLE 6: 80-PIN TQFP (CONTINUED)

Pin #	Master Core	Slave Core
44	RE9	S1RE9
45	PGC2/RP36/RB4	S1PGC2/S1AN9/S1RP36/S1PWM5L/S1RB4
46	RP56/ASDA1/SCK2/RC8	S1RP56/S1ASDA1/S1SCK1/S1RC8
47	RP57/ASCL1/SDI2/RC9	S1RP57/S1ASCL1/S1SDI1/S1RC9
48	PCI20/RD9	S1PCI20/S1RD9
49	SDO2/PCI19/RD8	S1SDO1/S1PCI19/S1RD8
50	Vss	Vss
51	VDD	VDD
52	RP71/RD7	S1RP71/S1PWM8H/S1RD7
53	RP70/RD6	S1RP70/S1PWM6H/S1RD6
54	RP69/RD5	S1RP69/S1PWM6L/S1RD5
55	PGD3/RP37/SDA2/RB5	S1PGD3/S1RP37/S1RB5
56	PGC3/RP38/SCL2/RB6	S1PGC3/S1RP38/S1RB6
57	RE10	S1RE10
58	TDO/AN9/RP39/RB7	S1MCLR1/S1AN6/S1RP39/S1PWM5H/S1RB7
59	RE11	S1RE11
60	PGD1/AN10/RP40/SCL1/RB8	S1PGD1/S1AN7/S1RP40/S1SCL1/S1RB8
61	PGC1/AN11/RP41/SDA1/RB9	S1PGC1/S1RP41/S1SDA1/S1RB9
62	ASCL2/RE12	S1RE12
63	RP52/RC4	S1RP52/S1PWM2H/S1RC4
64	ASDA2/RE13	S1RE13
65	RP53/RC5	S1RP53/S1PWM2L/S1RC5
66	RP58/RC10	S1RP58/S1PWM1H/S1RC10
67	RP59/RC11	S1RP59/S1PWM1L/S1RC11
68	RP68/RD4	S1RP68/S1PWM3H/S1RD4
69	RP67/RD3	S1RP67/S1PWM3L/S1RD3
70	Vss	Vss
71	VDD	VDD
72	RP66/RD2	S1RP66/S1PWM8L/S1RD2
73	RP65/RD1	S1RP65/S1PWM4H/S1RD1
74	RP64/RD0	S1RP64/S1PWM4L/S1RD0
75	TMS/RP42/PWM3H/RB10	S1RP42/S1RB10
76	TCK/RP43/PWM3L/RB11	S1RP43/S1RB11
77	RE14	S1RE14
78	TDI/RP44/PWM2H/RB12	S1RP44/S1RB12
79	RE15	S1RE15
80	RP45/PWM2L/RB13	S1RP45/S1RB13

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NOTES:

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ISBN: 978-1-5224-1674-6

Worldwide Sales and Service

AMERICAS

Corporate Office
 2355 West Chandler Blvd.
 Chandler, AZ 85224-6199
 Tel: 480-792-7200
 Fax: 480-792-7277
 Technical Support:
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 Web Address:
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ASIA/PACIFIC

Asia Pacific Office
 Suites 3707-14, 37th Floor
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 Harbour City, Kowloon

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