U2P

DATA SHEET

UPA to PCI Interface

DESCRIPTION

The U2P* chip is the primary connection on an UltraSPARC CPU board between the UPA System Bus (including UltraSPARC Processors and Memory) and a PCI based I/O Subsystem. Its major functions are UPA port interface, PCI bus interface, processor I/O data transfers, DMA data transfers and interrupt dispatch.

Features

- Full master and slave port connection to the high-speed UltraSPARC UPA Interconnect Architecture. The UPA is a split address/data packet-switched bus which has a potential data throughput rate of over one gigabyte/sec. UPA data is ECC protected.
- Two physically separate PCI bus segments, with full master and slave support.

  PCI Bus A has the following features:

  - 5 volt or 3.3 volt signalling.
  - 64-bit data bus.
  - Compatible with the PCI Rev 2.1 Specification.
  - Compatible with the PCI 66MHz extensions.
  - Support for up to four master devices (at 33MHz only).

  PCI Bus B has the following features:

  - 5 volt signalling.
  - 64-bit data bus.
  - Compatible with the PCI Rev 2.1 Specification.
  - Support for up to six master devices.
- Two separate 16-entry streaming caches, one for each bus segment, for accelerating some kinds of PCI DVMA activity. Single IOMMU with 16-entry TLB for mapping DVMA addresses for both busses.
- A “Mondo-Vector” Dispatch Unit, or MDU, for delivering Interrupt requests to UltraSparc CPU modules, including support for PCI interrupts from up to six total slots, as well as interrupts from on board IO devices.

* U2P was code named Psycho+

PRODUCT SUMMARY

The U2P uses the standard cell library from Lucent Technologies. It is implemented in 0.35 micron, 3 level metal and 3.3 volt optimized CMOS technology.

The U2P die has 352 signal pads (including specialty power / grounds) and 104 VSS / VDD pads for a total pad count of 456. The U2P package is a 456 pin PBGA, with 352 signal pins and 104 VSS / VDD pins. Its die consists of 170k gates and 29k bits of RAM.

The U2P design includes the following non-standard cells:

- 5V tolerant PCI pads.
- 66MHz capable PCI pads.
- UPA pads (without holding amps).
- PLL and PECL receiver for UPA clock.
- PLL for main clock.

The UPA operation is up to 100 MHz (10ns). Its main internal clock is up to 66.7 MHz (15 ns). The PCI bus A clocks at 1x or 0.5x internal clock (synchronous). The PCI bus B clocks at 0.5x internal clock (synchronous). The maximum power consumption is 3 watts.

Typical System Partition

Figure 1. shows one possible configuration of U2P in a PCI UltraSPARC system. U2P connects to the System Controller chip and other UPA ports via UPA address, control and data busses. The system has both PCI and EPCI slots, as well as an on board PCI device (PCIO). Interrupt information is provided by the RIC chip, and a JTAG port is provided for board testing as well as in-circuit testing and debugging of U2P.

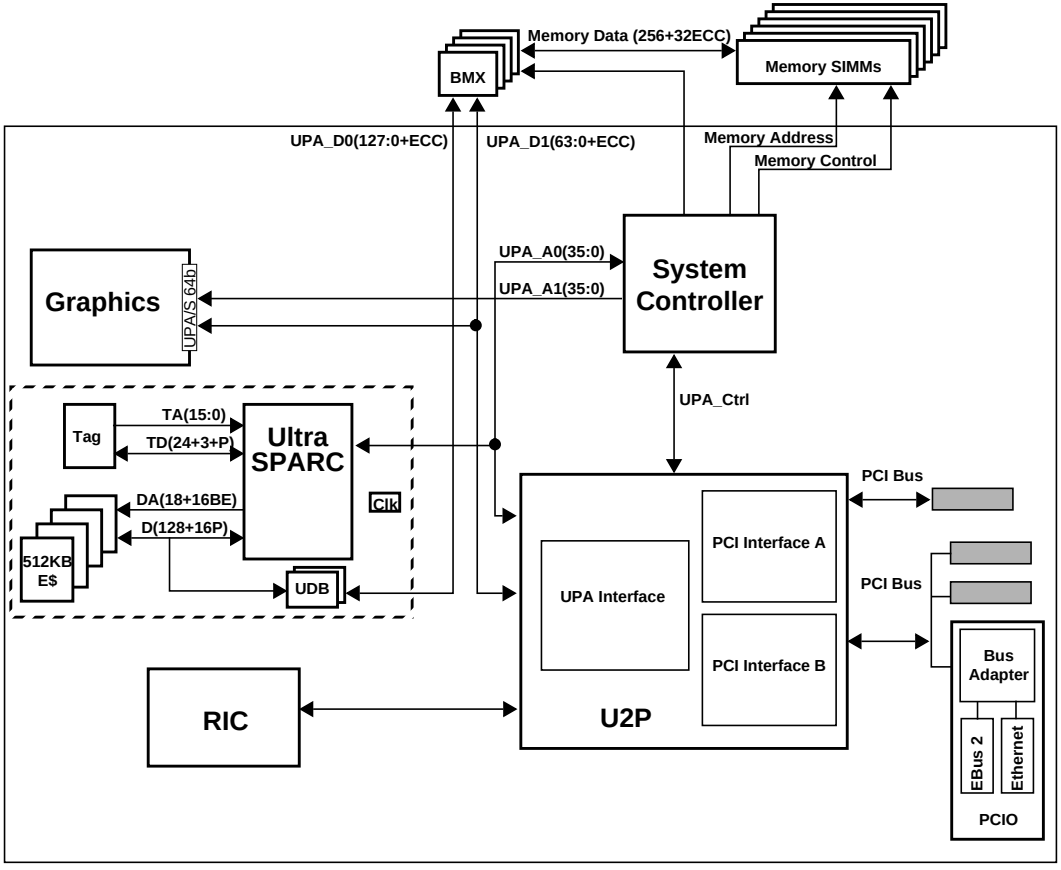


Figure 1. Typical System Block Diagram

External Interfaces

Figure 2. summarizes the external interfaces and pins of U2P.

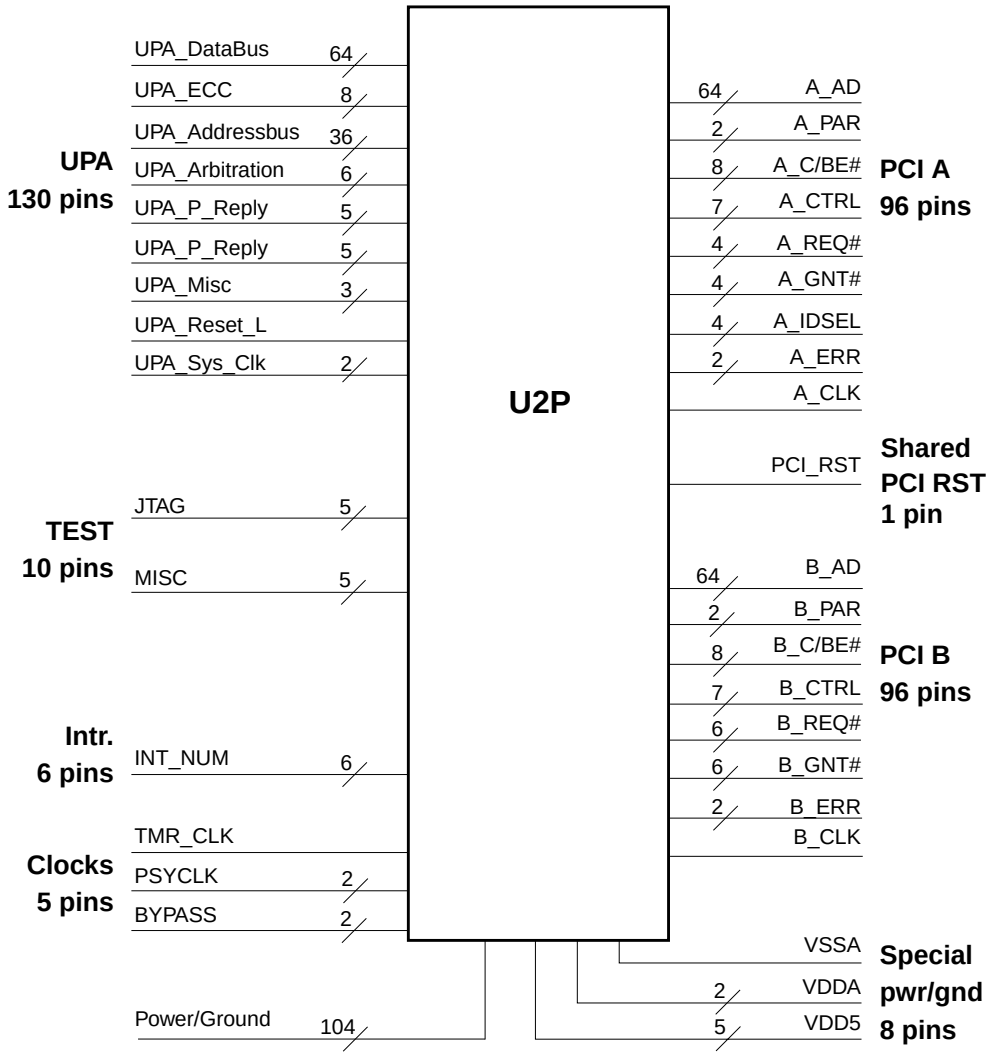


Figure 2. U2P External Interfaces

Block Diagram

Figure 3. shows a conceptual block diagram of U2P. The actual implementation is somewhat different - for example, there are no internal bidirectional busses. Block diagrams with the actual implementation details can be found in the U2P Users Manual.

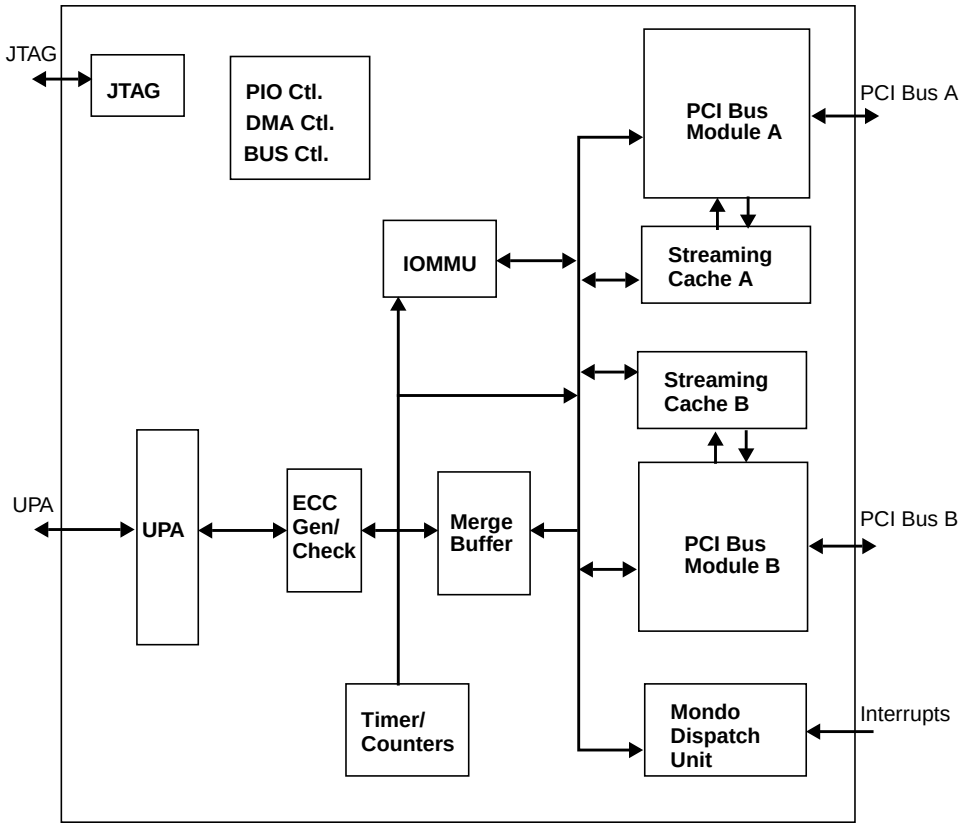


Figure 3. U2P Internal Block Diagram

Functional Block Overviews

This section gives a brief description of each top level functional block. A more detailed description of each block can be found in the U2P Users Manual. Each block is described in its own individual chapter in the U2P Users Manual. The top level blocks in U2P fall into one of five categories:

- UPA.
- PCI.
- Interrupt.
- Internal Control.
- Miscellaneous.

UPA Interface blocks

The UPA is UltraSPARC's packet switched main system bus. In an UltraSPARC system, the UPA can operate up to 100 MHz. Data and address have independent flow controls. Each type of UPA cycle (PIO read, PIO write, DMA read, etc.) uses its own FIFO-based queueing. There is a synchronization boundary between the UPA interface blocks and other U2P blocks, which run at 66.7 MHz.

- **UPA Master/Slave**: This block deals exclusively with UPA address control. It listens to UPA_A when U2P is a slave. It also arbitrates for and drives UPA_A when U2P is a master.
- **UPA_Reply:** This block deals exclusively with UPA data. It generates P_REPLY to the System Controller (SC) ASIC during PIO and copyback cycles. It also listens to S_REPLY from the SC and manages the UPA data FIFO's accordingly.
- **ECC Generate:** Generates ECC on the outgoing 64-bit UPA data path.
- **ECC Check:** Checks ECC on the incoming 64-bit UPA data path.

PCI Interface blocks

- **PBM (PCI Bus Module):** This is the main portion of the PCI interface. U2P contains two nearly identical copies of this block. One is designed to support a 64-bit PCI bus at 66 MHz or 33 MHz with up to four master devices. The other supports a 64-bit PCI bus at 33MHz with up to six master devices. The PBM adheres to all PCI protocol guidelines as contained in the PCI Revision 2.1 specification. Each PBM controls arbitration, flow control and error handling for its bus segment. Each PBM also handles the big- to little-endian byte twisting required for correct operation of both PIO and DVMA datapaths.
- **IOMMU:** For the portion of the PCI memory address space which is reserved for DMA to the UPA bus, the IOMMU maps the PCI address into the appropriate UPA physical address. The IOMMU keeps the 16 most recently used translations in a TLB, and automatically performs hardware tablewalks on TLB misses. There is a single IOMMU supporting both PCI busses. Only a single translation can be in progress at a time, and during tablewalks, translations from the other bus segment will be delayed.
- **Streaming Cache:** The Streaming Cache (STC) is used to accelerate PCI DMA activity. For DMA reads, the STC will speculatively prefetch 64-byte cache lines. For DMA writes, the STC buffers up 64-byte lines before sending to the UPA interface. There are two separate STC blocks in U2P, one associated with each PBM block. Each STC contains storage for 16 virtual address tagged entries and their data, which is stored in 64-byte lines, allocated on a least recently used basis.

Interrupt block

Mondo Dispatch Unit (MDU): In the Sun-4U architecture, interrupts to a processor are sent as packets on the UPA bus. The MDU in U2P is a system resource for generating such packets. The MDU accepts interrupt requests from the UPA slave ports, PCI busses and internal U2P sources and dispatches interrupt packets to the UPA.

Internal Control

- **Merge Buffer:** In order to allow sub-line writes into a 64-byte memory line, it is necessary to perform a read-modify-write operation on the UPA. The Merge Buffer is responsible for generating the correct UPA read, merging the partial line, and writing the whole block to the UPA.
- **PIO Control:** Decodes slave requests from the UPA_A request FIFO, arbitrates for the appropriate resource and dispatches the request.
- **Bus Control:** This is an internal arbiter shared by the PIO Control and DMA Control blocks. It schedules the use of the main internal data paths.
- **DMA Control:** Arbitrates and decodes requests from internal DMA sources (PBM, STC, IOMMU, MDU), and arbitrates for the appropriate UPA FIFO.

Miscellaneous

- **Timer/Counter:** Contains two identical 32-bit timer-counters as specified by the Sun-4U architecture. Used for system scheduling and profiling.
- **JTAG Control:** Provides the necessary control for the standard IEEE 1149.1 JTAG port, as well as additional scan based features that are useful for debugging purposes.

PCI Address Map Overview

Complete information on address maps and other software visible features of U2P can be found in the Programmer's Model chapter of the U2P Users Manual. A simplified diagram showing PIO and normal DVMA address spaces is in Figure 4.

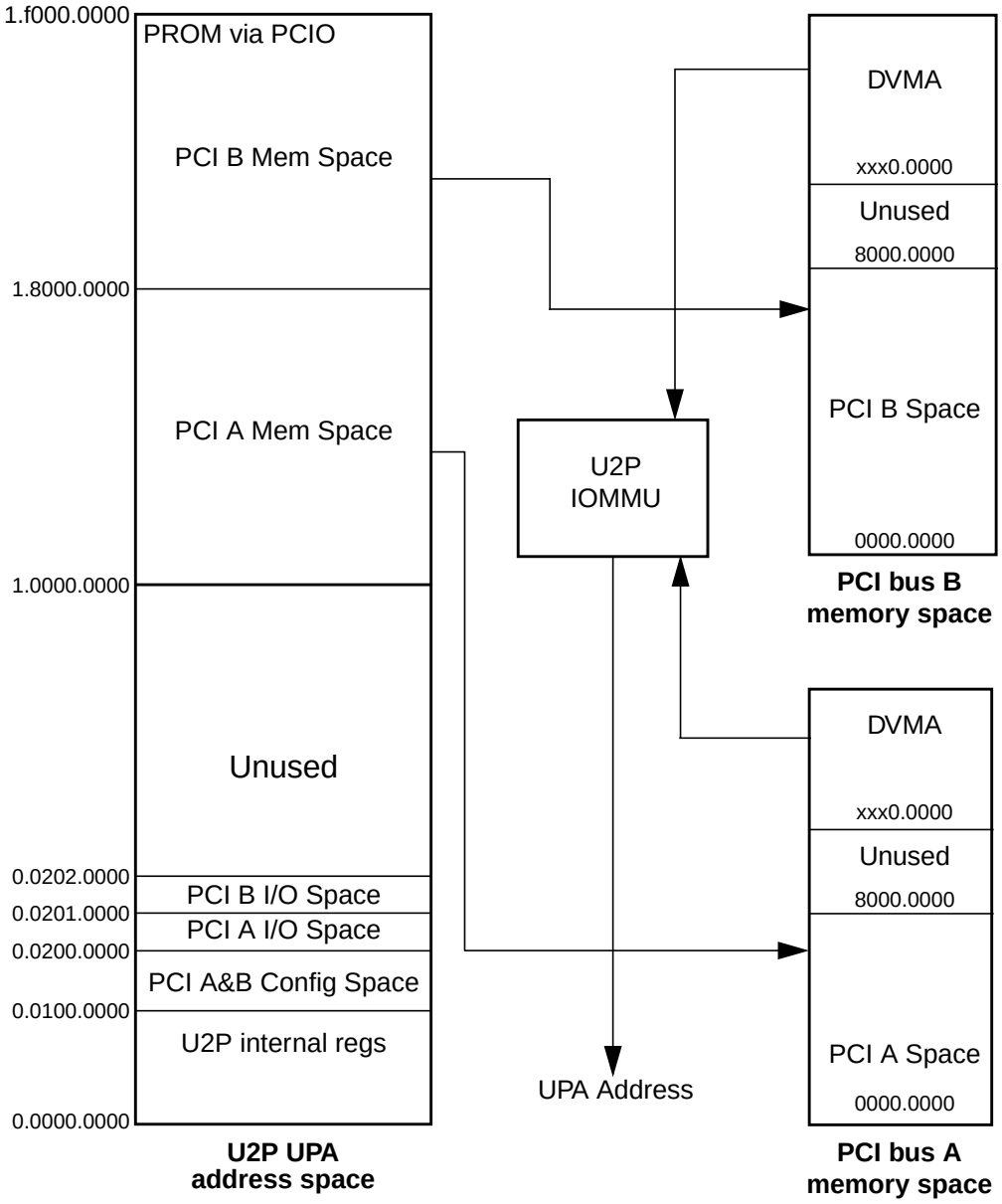


Figure 4. PIO and DVMA address spaces

SIGNAL DESCRIPTION

Pin naming conventions

- Active low signals are denoted by an underscore or underscore L, following the signal name, examples: B_CBE_[0] and UPA_CLK_L.
- Direction is input (I), output (O), and bidirectional (IO).

TABLE 1: Signal Name Prefixes

Functional Block	Prefix
PCI66 Bus (66MHz)	A_
PCI Bus (33MHz)	B_
UPA bus	UPA_
JTAG Port	PSY_T

Pin Summary

TABLE 2: Pin Count

Section	Pins	What It Includes
UPA Interface	130	UPA Master/Slave/Interrupter 64 bit interface
PCIA Interface	97	66MHz, 64 bit PCI interface, shared PCI Reset
PCIB Interface	96	33MHz, 64 bit PCI interface
Clock inputs	5	UPA, U2P core, Timer clocks and bypass
Miscellaneous	11	Interrupts, reset, ext/int_event
Test	5	JTAG port and diagnostics
Signal Total	**344**	
Power/Ground	**112**	Including 8 special Power/Ground Pins
Total	**456**	

Pinout by Pin Number

TABLE 3: PBGA Pinout

Signal Name	Ball	Direction	Cell Type	Description
VDD	A1			
VSS	A2			
ECC_VLD	A3	I	BIN02S	UPA ECC is valid
UPA_SRLY[2]	A4	I	BIN02S	UPA system reply
VDD	A5			
VSS	A6			
UPA_CR	A7	I	BIN02S	UPA SC request
UPA_AP	A8	IO	BN02Z24S	UPA address parity
UPA_A[3]	A9	IO	BN02Z24S	UPA address
VDD	A10			
VSS	A11			
UPA_A[14]	A12	IO	BN02Z24S	UPA address
UPA_A[19]	A13	IO	BN02Z24S	UPA address
UPA_A[24]	A14	IO	BN02Z24S	UPA address
UPA_A[29]	A15	IO	BN02Z24S	UPA address
VSS	A16			
VDD	A17			
INT_NUM[4]	A18	I	B5IN03S	Interrupt number
BOOT_BUS	A19	I	BIN06S	1= boot device on PCIB, 0= boot device on PCIA
PCI_RST_	A20	O	PCI21MUS	PCI reset
VSS	A21			
VDD	A22			
VDD5	A23		NVDD5P	PCIA input diode clamp reference voltage (note 1)
A_AD[2]	A24	IO	PCIMXI21	PCIA address/data bus
VSS	A25			
VDD	A26			
VSS	B1			
UPA_ECC[5]	B2	IO	BN02Z24S	UPA ECC bus
UPA_SRLY[0]	B3	I	BIN02S	UPA system reply
UPA_SRLY[4]	B4	I	BIN02S	UPA system reply
UPA_PRLY[1]	B5	O	BOZ24S	UPA port reply
UPA_PRLY[3]	B6	O	BOZ24S	UPA port reply
UPA_RIN[0]	B7	I	BIN02S	UPA request in
UPA_A[0]	B8	IO	BN02Z24S	UPA address
UPA_A[4]	B9	IO	BN02Z24S	UPA address

TABLE 3: PBGA Pinout (Continued)

Signal Name	Ball	Direction	Cell Type	Description
UPA_A[8]	B10	IO	BN02Z24S	UPA address
UPA_A[11]	B11	IO	BN02Z24S	UPA address
UPA_A[15]	B12	IO	BN02Z24S	UPA address
UPA_A[20]	B13	IO	BN02Z24S	UPA address
UPA_A[23]	B14	IO	BN02Z24S	UPA address
UPA_A[28]	B15	IO	BN02Z24S	UPA address
UPA_A[32]	B16	IO	BN02Z24S	UPA address
UPA_RST_L	B17	I	PINX02S	UPA reset. Main U2P reset.
INT_NUM[3]	B18	I	B5IN03S	Interrupt number
EXT_EVENT	B19	IO	PNAXZ24S	External event interrupt
INT_EVENT	B20	O	BOZ24S	Internal event interrupt
UPA_CLK	B21	I	BIED03S	UPA 100MHz input clock (pos, PECL)
UPA_BYPASS	B22	I	BIN06NA	UPA PLL bypass
PSYCLOPS_CLK	B23	I	BIN02NA	66MHz main clock
A_AD[1]	B24	IO	PCIMXI21	PCIA address/data bus
A_AD[3]	B25	IO	PCIMXI21	PCIA address/data bus
VSS	B26			
UPA_ECC[4]	C1	IO	BN02Z24S	UPA ECC bus
UPA_ECC[3]	C2	IO	BN02Z24S	UPA ECC bus
UPA_ECC[7]	C3	IO	BN02Z24S	UPA ECC bus
UPA_SRLY[1]	C4	I	BIN02S	UPA system reply
UPA_DTST	C5	I	BIN02S	UPA data stall
UPA_PRLY[2]	C6	O	BOZ24S	UPA port reply
UPA_ARBRST_L	C7	I	BIN02S	UPA arbitration reset
UPA_RIN[2]	C8	I	BIN02S	UPA request in
UPA_A[2]	C9	IO	BN02Z24S	UPA address
UPA_A[6]	C10	IO	BN02Z24S	UPA address
UPA_A[10]	C11	IO	BN02Z24S	UPA address
UPA_A[13]	C12	IO	BN02Z24S	UPA address
UPA_A[18]	C13	IO	BN02Z24S	UPA address
UPA_A[25]	C14	IO	BN02Z24S	UPA address
UPA_A[30]	C15	IO	BN02Z24S	UPA address
UPA_A[33]	C16	IO	BN02Z24S	UPA address
INT_NUM[1]	C17	I	B5IN03S	Interrupt number
INT_NUM[5]	C18	I	B5IN03S	Interrupt number
PSY_TMS	C19	I	PINA02S	JTAG Test mode select
VDDA-VA1	C20		NVDDAN	PLL 3.3V supply, filtered

TABLE 3: PBGA Pinout (Continued)

Signal Name	Ball	Direction	Cell Type	Description
VSSA-VS1	C21		NVSSAN	PLL ground
VDDA-VA2	C22		NVDDAN	PLL 3.3V supply, filtered
A_AD[0]	C23	IO	PCIMXI21	PCIA address/data bus
A_AD[6]	C24	IO	PCIMXI21	PCIA address/data bus
A_AD[8]	C25	IO	PCIMXI21	PCIA address/data bus
A_AD[7]	C26	IO	PCIMXI21	PCIA address/data bus
UPA_ECC[1]	D1	IO	BN02Z24S	UPA ECC bus
UPA_DB[63]	D2	IO	BN02Z24S	UPA data bus
UPA_ECC[2]	D3	IO	BN02Z24S	UPA ECC bus
VSS	D4			
UPA_PRLY[0]	D5	O	BOZ24S	UPA port reply
UPA_PRLY[4]	D6	O	BOZ24S	UPA port reply
UPA_RIN[1]	D7	I	BIN02S	UPA request in
UPA_A[1]	D8	IO	BN02Z24S	UPA address
UPA_A[5]	D9	IO	BN02Z24S	UPA address
UPA_A[9]	D10	IO	BN02Z24S	UPA address
UPA_A[12]	D11	IO	BN02Z24S	UPA address
UPA_A[16]	D12	IO	BN02Z24S	UPA address
UPA_A[21]	D13	IO	BN02Z24S	UPA address
UPA_A[22]	D14	IO	BN02Z24S	UPA address
UPA_A[27]	D15	IO	BN02Z24S	UPA address
UPA_A[31]	D16	IO	BN02Z24S	UPA address
UPA_A[34]	D17	IO	BN02Z24S	UPA address
INT_NUM[2]	D18	I	B5IN03S	Interrupt number
VDD5	D19		NVDD5P	5V input diode clamp reference voltage (note 2)
PSY_TRST_L	D20	I	PINA02S	JTAG Test reset
UPA_CLK_L	D21	I	BIED03S	UPA 100MHz input clock (neg, PECL)
PSY_BYPASS	D22	I	BIN06NA	PSYCLK PLL bypass
VSS	D23			
A_AD[9]	D24	IO	PCIMXI21	PCIA address/data bus
A_AD[12]	D25	IO	PCIMXI21	PCIA address/data bus
A_AD[10]	D26	IO	PCIMXI21	PCIA address/data bus
VDD	E1			
UPA_DB[60]	E2	IO	BN02Z24S	UPA data bus
UPA_DB[62]	E3	IO	BN02Z24S	UPA data bus
UPA_DB[61]	E4	IO	BN02Z24S	UPA data bus
VDD	E5			

TABLE 3: PBGA Pinout (Continued)

Signal Name	Ball	Direction	Cell Type	Description
B_CPU_GNT_	E6	O	BOZ24S	PCIB internal grant (debug only)
VSS	E7			
UPA_SRLY[3]	E8	I	BIN02S	UPA system reply
UPA_ROUT	E9	O	BOZ24S	UPA request out
UPA_AV	E10	IO	BN02Z24S	UPA address valid
VDD	E11			
UPA_A[7]	E12	IO	BN02Z24S	UPA address
UPA_A[17]	E13	IO	BN02Z24S	UPA address
UPA_A[26]	E14	IO	BN02Z24S	UPA address
INT_NUM[0]	E15	I	B5IN03S	Interrupt number
VDD	E16			
PSY_TCLK	E17	I	BIN02S	JTAG Test clock
PSY_TDO	E18	O	B5OZ10S	JTAG Test data output
PSYCLOPS_CLKR	E19	I	REFPAD	66MHz clock reference pad to connect ext cap
VSS	E20			
A_AD[4]	E21	IO	PCIMXI21	PCIA address/data bus
VDD	E22			
A_AD[14]	E23	IO	PCIMXI21	PCIA address/data bus
A_AD[13]	E24	IO	PCIMXI21	PCIA address/data bus
A_AD[15]	E25	IO	PCIMXI21	PCIA address/data bus
VDD	E26			
VSS	F1			
UPA_DB[58]	F2	IO	BN02Z24S	UPA data bus
UPA_DB[59]	F3	IO	BN02Z24S	UPA data bus
UPA_DB[57]	F4	IO	BN02Z24S	UPA data bus
UPA_ECC[6]	F5	IO	BN02Z24S	UPA ECC bus
A_AD[5]	F22	IO	PCIMXI21	PCIA address/data bus
A_AD[18]	F23	IO	PCIMXI21	PCIA address/data bus
A_AD[16]	F24	IO	PCIMXI21	PCIA address/data bus
A_AD[17]	F25	IO	PCIMXI21	PCIA address/data bus
VSS	F26			
UPA_DB[54]	G1	IO	BN02Z24S	UPA data bus
UPA_DB[53]	G2	IO	BN02Z24S	UPA data bus
UPA_DB[56]	G3	IO	BN02Z24S	UPA data bus
UPA_DB[52]	G4	IO	BN02Z24S	UPA data bus
VSS	G5			
VSS	G22			

TABLE 3: PBGA Pinout (Continued)

Signal Name	Ball	Direction	Cell Type	Description
A_AD[23]	G23	IO	PCIMXI21	PCIA address/data bus
A_AD[19]	G24	IO	PCIMXI21	PCIA address/data bus
A_AD[22]	G25	IO	PCIMXI21	PCIA address/data bus
A_AD[21]	G26	IO	PCIMXI21	PCIA address/data bus
UPA_DB[49]	H1	IO	BN02Z24S	UPA data bus
UPA_DB[48]	H2	IO	BN02Z24S	UPA data bus
UPA_DB[51]	H3	IO	BN02Z24S	UPA data bus
UPA_DB[47]	H4	IO	BN02Z24S	UPA data bus
UPA_ECC[0]	H5	IO	BN02Z24S	UPA ECC bus
A_AD[11]	H22	IO	PCIMXI21	PCIA address/data bus
A_AD[28]	H23	IO	PCIMXI21	PCIA address/data bus
A_AD[24]	H24	IO	PCIMXI21	PCIA address/data bus
A_AD[27]	H25	IO	PCIMXI21	PCIA address/data bus
A_AD[26]	H26	IO	PCIMXI21	PCIA address/data bus
UPA_DB[45]	J1	IO	BN02Z24S	UPA data bus
UPA_DB[44]	J2	IO	BN02Z24S	UPA data bus
UPA_DB[46]	J3	IO	BN02Z24S	UPA data bus
UPA_DB[43]	J4	IO	BN02Z24S	UPA data bus
UPA_DB[55]	J5	IO	BN02Z24S	UPA data bus
A_AD[20]	J22	IO	PCIMXI21	PCIA address/data bus
A_AD[32]	J23	IO	PCIMXI21	PCIA address/data bus
A_AD[29]	J24	IO	PCIMXI21	PCIA address/data bus
A_AD[31]	J25	IO	PCIMXI21	PCIA address/data bus
A_AD[30]	J26	IO	PCIMXI21	PCIA address/data bus
VDD	K1			
UPA_DB[40]	K2	IO	BN02Z24S	UPA data bus
UPA_DB[42]	K3	IO	BN02Z24S	UPA data bus
UPA_DB[39]	K4	IO	BN02Z24S	UPA data bus
UPA_DB[50]	K5	IO	BN02Z24S	UPA data bus
A_AD[25]	K22	IO	PCIMXI21	PCIA address/data bus
A_AD[36]	K23	IO	PCIMXI21	PCIA address/data bus
A_AD[33]	K24	IO	PCIMXI21	PCIA address/data bus
A_AD[35]	K25	IO	PCIMXI21	PCIA address/data bus
VDD	K26			
VSS	L1			
UPA_DB[37]	L2	IO	BN02Z24S	UPA data bus
UPA_DB[38]	L3	IO	BN02Z24S	UPA data bus

TABLE 3: PBGA Pinout (Continued)

Signal Name	Ball	Direction	Cell Type	Description
UPA_DB[36]	L4	IO	BN02Z24S	UPA data bus
VDD	L5			
VSS	L11			
VSS	L12			
VSS	L13			
VSS	L14			
VSS	L15			
VSS	L16			
VDD	L22			
A_AD[39]	L23	IO	PCIMXI21	PCIA address/data bus
A_AD[37]	L24	IO	PCIMXI21	PCIA address/data bus
A_AD[38]	L25	IO	PCIMXI21	PCIA address/data bus
VSS	L26			
UPA_DB[34]	M1	IO	BN02Z24S	UPA data bus
UPA_DB[33]	M2	IO	BN02Z24S	UPA data bus
UPA_DB[35]	M3	IO	BN02Z24S	UPA data bus
UPA_DB[32]	M4	IO	BN02Z24S	UPA data bus
UPA_DB[41]	M5	IO	BN02Z24S	UPA data bus
VSS	M11			
VSS	M12			
VSS	M13			
VSS	M14			
VSS	M15			
VSS	M16			
A_AD[34]	M22	IO	PCIMXI21	PCIA address/data bus
A_AD[43]	M23	IO	PCIMXI21	PCIA address/data bus
A_AD[40]	M24	IO	PCIMXI21	PCIA address/data bus
A_AD[42]	M25	IO	PCIMXI21	PCIA address/data bus
A_AD[41]	M26	IO	PCIMXI21	PCIA address/data bus
UPA_DB[29]	N1	IO	BN02Z24S	UPA data bus
UPA_DB[28]	N2	IO	BN02Z24S	UPA data bus
UPA_DB[30]	N3	IO	BN02Z24S	UPA data bus
UPA_DB[27]	N4	IO	BN02Z24S	UPA data bus
UPA_DB[31]	N5	IO	BN02Z24S	UPA data bus
VSS	N11			
VSS	N12			
VSS	N13			

TABLE 3: PBGA Pinout (Continued)

Signal Name	Ball	Direction	Cell Type	Description
VSS	N14			
VSS	N15			
VSS	N16			
A_AD[44]	N22	IO	PCIMXI21	PCIA address/data bus
A_AD[48]	N23	IO	PCIMXI21	PCIA address/data bus
A_AD[45]	N24	IO	PCIMXI21	PCIA address/data bus
A_AD[47]	N25	IO	PCIMXI21	PCIA address/data bus
A_AD[46]	N26	IO	PCIMXI21	PCIA address/data bus
UPA_DB[24]	P1	IO	BN02Z24S	UPA data bus
UPA_DB[25]	P2	IO	BN02Z24S	UPA data bus
UPA_DB[23]	P3	IO	BN02Z24S	UPA data bus
UPA_DB[26]	P4	IO	BN02Z24S	UPA data bus
UPA_DB[22]	P5	IO	BN02Z24S	UPA data bus
VSS	P11			
VSS	P12			
VSS	P13			
VSS	P14			
VSS	P15			
VSS	P16			
A_AD[53]	P22	IO	PCIMXI21	PCIA address/data bus
A_AD[49]	P23	IO	PCIMXI21	PCIA address/data bus
A_AD[52]	P24	IO	PCIMXI21	PCIA address/data bus
A_AD[50]	P25	IO	PCIMXI21	PCIA address/data bus
A_AD[51]	P26	IO	PCIMXI21	PCIA address/data bus
UPA_DB[19]	R1	IO	BN02Z24S	UPA data bus
UPA_DB[20]	R2	IO	BN02Z24S	UPA data bus
UPA_DB[18]	R3	IO	BN02Z24S	UPA data bus
UPA_DB[21]	R4	IO	BN02Z24S	UPA data bus
UPA_DB[12]	R5	IO	BN02Z24S	UPA data bus
VSS	R11			
VSS	R12			
VSS	R13			
VSS	R14			
VSS	R15			
VSS	R16			
A_AD[63]	R22	IO	PCIMXI21	PCIA address/data bus
A_AD[54]	R23	IO	PCIMXI21	PCIA address/data bus

TABLE 3: PBGA Pinout (Continued)

Signal Name	Ball	Direction	Cell Type	Description
A_AD[57]	R24	IO	PCIMXI21	PCIA address/data bus
A_AD[55]	R25	IO	PCIMXI21	PCIA address/data bus
A_AD[56]	R26	IO	PCIMXI21	PCIA address/data bus
VSS	T1			
UPA_DB[16]	T2	IO	BN02Z24S	UPA data bus
UPA_DB[15]	T3	IO	BN02Z24S	UPA data bus
UPA_DB[17]	T4	IO	BN02Z24S	UPA data bus
VDD	T5			
VSS	T11			
VSS	T12			
VSS	T13			
VSS	T14			
VSS	T15			
VSS	T16			
VDD	T22			
A_AD[58]	T23	IO	PCIMXI21	PCIA address/data bus
A_AD[60]	T24	IO	PCIMXI21	PCIA address/data bus
A_AD[59]	T25	IO	PCIMXI21	PCIA address/data bus
VSS	T26			
VDD	U1			
UPA_DB[13]	U2	IO	BN02Z24S	UPA data bus
UPA_DB[11]	U3	IO	BN02Z24S	UPA data bus
UPA_DB[14]	U4	IO	BN02Z24S	UPA data bus
UPA_DB[3]	U5	IO	BN02Z24S	UPA data bus
VDD5	U22		NVDD5P	PCIA input diode clamp reference voltage (note 1)
A_AD[61]	U23	IO	PCIMXI21	PCIA address/data bus
A_CBE_[0]	U24	IO	PCIMXI21	PCIA command/byte enable bus
A_AD[62]	U25	IO	PCIMXI21	PCIA address/data bus
VDD	U26			
UPA_DB[8]	V1	IO	BN02Z24S	UPA data bus
UPA_DB[9]	V2	IO	BN02Z24S	UPA data bus
UPA_DB[7]	V3	IO	BN02Z24S	UPA data bus
UPA_DB[10]	V4	IO	BN02Z24S	UPA data bus
VDD5	V5		NVDD5P	5V input diode clamp reference voltage (note 2)
A_ACK64_	V22	IO	PCIMXI21	PCIA 64bit ACK
A_CBE_[1]	V23	IO	PCIMXI21	PCIA command/byte enable bus
A_CBE_[4]	V24	IO	PCIMXI21	PCIA command/byte enable bus

TABLE 3: PBGA Pinout (Continued)

Signal Name	Ball	Direction	Cell Type	Description
A_CBE_[2]	V25	IO	PCIMXI21	PCIA command/byte enable bus
A_CBE_[3]	V26	IO	PCIMXI21	PCIA command/byte enable bus
UPA_DB[4]	W1	IO	BN02Z24S	UPA data bus
UPA_DB[5]	W2	IO	BN02Z24S	UPA data bus
UPA_DB[2]	W3	IO	BN02Z24S	UPA data bus
UPA_DB[6]	W4	IO	BN02Z24S	UPA data bus
B_AD[56]	W5	IO	PCI21LUS	PCIB address/data bus
A_IDSEL[3]	W22	O	PCI21MUN	PCIA Config cycle chip selects
A_CBE_[5]	W23	IO	PCIMXI21	PCIA command/byte enable bus
A_PAR	W24	IO	PCIMXI21	PCIA AD[31:0]/CBE[3:0] even parity
A_CBE_[6]	W25	IO	PCIMXI21	PCIA command/byte enable bus
A_CBE_[7]	W26	IO	PCIMXI21	PCIA command/byte enable bus
TMR_CLK	Y1	I	B5IN03N	10MHz Timer input clock
UPA_DB[0]	Y2	IO	BN02Z24S	UPA data bus
B_CPU_REQ_	Y3	O	PCI21LUS	PCIB internal request (debug only)
UPA_DB[1]	Y4	IO	BN02Z24S	UPA data bus
VSS	Y5			
VSS	Y22			
A_PAR64	Y23	IO	PCIMXI21	PCIA AD[63:32]/CBE[7:4] even parity
A_TRDY_	Y24	IO	PCIMXI21	PCIA target ready
A_FRAME_	Y25	IO	PCIMXI21	PCIA frame
A_REQ64_	Y26	IO	PCIMXI21	PCIA 64 bit request
VSS	AA1			
B_AD[62]	AA2	IO	PCI21LUS	PCIB address/data bus
B_AD[61]	AA3	IO	PCI21LUS	PCIB address/data bus
B_AD[63]	AA4	IO	PCI21LUS	PCIB address/data bus
B_AD[50]	AA5	IO	PCI21LUS	PCIB address/data bus
A_REQ_[0]	AA22	I	PCI21MIN	PCIA bus request
A_IRDY_	AA23	IO	PCIMXI21	PCIA initiator ready
A_STOP_	AA24	IO	PCIMXI21	PCIA stop
PSY_TDI	AA25	I	PINA02N	JTAG Test data in
VSS	AA26			
VDD	AB1			
B_AD[60]	AB2	IO	PCI21LUS	PCIB address/data bus
B_AD[58]	AB3	IO	PCI21LUS	PCIB address/data bus
B_AD[59]	AB4	IO	PCI21LUS	PCIB address/data bus
VDD	AB5			

TABLE 3: PBGA Pinout (Continued)

Signal Name	Ball	Direction	Cell Type	Description
B_AD[49]	AB6	IO	PCI21LUS	PCIB address/data bus
VSS	AB7			
B_AD[43]	AB8	IO	PCI21LUS	PCIB address/data bus
B_AD[34]	AB9	IO	PCI21LUS	PCIB address/data bus
B_AD[29]	AB10	IO	PCI21LUS	PCIB address/data bus
VDD	AB11			
B_AD[20]	AB12	IO	PCI21LUS	PCIB address/data bus
B_AD[10]	AB13	IO	PCI21LUS	PCIB address/data bus
B_AD[1]	AB14	IO	PCI21LUS	PCIB address/data bus
B_CBE_[0]	AB15	IO	PCI21LUS	PCIB command/byte enable bus
VDD	AB16			
B_PAR64	AB17	IO	PCI21LUS	PCIB AD[63:32]/CBE[7:4] even parity
B_GNT_[2]	AB18	O	PCI21LUS	PCIB bus grant
B_SERR_	AB19	I	PCI21LIS	PCIB system error
VSS	AB20			
A_REQ_[1]	AB21	I	PCI21MIN	PCIA bus request
VDD	AB22			
A_IDSEL[0]	AB23	O	PCI21MUN	PCIA Config cycle chip selects
A_IDSEL[1]	AB24	O	PCI21MUN	PCIA Config cycle chip selects
A_DEVSEL_	AB25	IO	PCIMXI21	PCIA device select
VDD	AB26			
B_AD[55]	AC1	IO	PCI21LUS	PCIB address/data bus
B_AD[57]	AC2	IO	PCI21LUS	PCIB address/data bus
B_AD[54]	AC3	IO	PCI21LUS	PCIB address/data bus
VSS	AC4			
B_AD[40]	AC5	IO	PCI21LUS	PCIB address/data bus
B_AD[36]	AC6	IO	PCI21LUS	PCIB address/data bus
B_AD[31]	AC7	IO	PCI21LUS	PCIB address/data bus
B_AD[26]	AC8	IO	PCI21LUS	PCIB address/data bus
B_AD[22]	AC9	IO	PCI21LUS	PCIB address/data bus
B_AD[18]	AC10	IO	PCI21LUS	PCIB address/data bus
B_AD[15]	AC11	IO	PCI21LUS	PCIB address/data bus
B_AD[11]	AC12	IO	PCI21LUS	PCIB address/data bus
B_AD[6]	AC13	IO	PCI21LUS	PCIB address/data bus
B_AD[5]	AC14	IO	PCI21LUS	PCIB address/data bus
B_AD[0]	AC15	IO	PCI21LUS	PCIB address/data bus
B_CBE_[5]	AC16	IO	PCI21LUS	PCIB command/byte enable bus

TABLE 3: PBGA Pinout (Continued)

Signal Name	Ball	Direction	Cell Type	Description
B_CBE_[2]	AC17	IO	PCI21LUS	PCIB command/byte enable bus
B_REQ64_	AC18	IO	PCI21LUS	PCIB 64 bit request
B_STOP_	AC19	IO	PCI21LUS	PCIB stop
B_GNT_[5]	AC20	O	PCI21LUS	PCIB bus grant
B_GNT_[0]	AC21	O	PCI21LUS	PCIB bus grant
B_REQ_[2]	AC22	I	PCI21LIS	PCIB bus request
VSS	AC23			
A_GNT_[0]	AC24	O	PCI21MUN	PCIA bus grant
A_IDSEL[2]	AC25	O	PCI21MUN	PCIA Config cycle chip selects
A_PERR_	AC26	IO	PCIMXI21	PCIA bus parity error
B_AD[52]	AD1	IO	PCI21LUS	PCIB address/data bus
B_AD[53]	AD2	IO	PCI21LUS	PCIB address/data bus
B_AD[51]	AD3	IO	PCI21LUS	PCIB address/data bus
B_AD[45]	AD4	IO	PCI21LUS	PCIB address/data bus
B_AD[41]	AD5	IO	PCI21LUS	PCIB address/data bus
B_AD[38]	AD6	IO	PCI21LUS	PCIB address/data bus
B_AD[35]	AD7	IO	PCI21LUS	PCIB address/data bus
B_AD[30]	AD8	IO	PCI21LUS	PCIB address/data bus
B_AD[25]	AD9	IO	PCI21LUS	PCIB address/data bus
B_AD[21]	AD10	IO	PCI21LUS	PCIB address/data bus
B_AD[17]	AD11	IO	PCI21LUS	PCIB address/data bus
B_AD[14]	AD12	IO	PCI21LUS	PCIB address/data bus
B_AD[9]	AD13	IO	PCI21LUS	PCIB address/data bus
B_AD[2]	AD14	IO	PCI21LUS	PCIB address/data bus
B_CBE_[6]	AD15	IO	PCI21LUS	PCIB command/byte enable bus
B_CBE_[3]	AD16	IO	PCI21LUS	PCIB command/byte enable bus
B_ACK64_	AD17	IO	PCI21LUS	PCIB 64bit ACK
B_IRDY_	AD18	IO	PCI21LUS	PCIB initiator ready
B_PAR	AD19	IO	PCI21LUS	PCIB AD[31:0]/CBE[3:0] even parity
B_GNT_[1]	AD20	O	PCI21LUS	PCIB bus grant
B_REQ_[4]	AD21	I	PCI21LIS	PCIB bus request
B_REQ_[1]	AD22	I	PCI21LIS	PCIB bus request
A_CLK	AD23	I	PCI21MIN	PCIA bus clock phase detect (note 3)
A_REQ_[2]	AD24	I	PCI21MIN	PCIA bus request
A_GNT_[1]	AD25	O	PCI21MUN	PCIA bus grant
A_GNT_[2]	AD26	O	PCI21MUN	PCIA bus grant
VSS	AE1			

TABLE 3: PBGA Pinout (Continued)

Signal Name	Ball	Direction	Cell Type	Description
B_AD[48]	AE2	IO	PCI21LUS	PCIB address/data bus
B_AD[46]	AE3	IO	PCI21LUS	PCIB address/data bus
B_AD[42]	AE4	IO	PCI21LUS	PCIB address/data bus
B_AD[39]	AE5	IO	PCI21LUS	PCIB address/data bus
B_AD[37]	AE6	IO	PCI21LUS	PCIB address/data bus
B_AD[32]	AE7	IO	PCI21LUS	PCIB address/data bus
B_AD[27]	AE8	IO	PCI21LUS	PCIB address/data bus
B_AD[23]	AE9	IO	PCI21LUS	PCIB address/data bus
B_AD[19]	AE10	IO	PCI21LUS	PCIB address/data bus
B_AD[16]	AE11	IO	PCI21LUS	PCIB address/data bus
B_AD[12]	AE12	IO	PCI21LUS	PCIB address/data bus
B_AD[7]	AE13	IO	PCI21LUS	PCIB address/data bus
B_AD[4]	AE14	IO	PCI21LUS	PCIB address/data bus
VDD5	AE15		NVDD5P	5V input diode clamp reference voltage (note2)
B_CBE_[4]	AE16	IO	PCI21LUS	PCIB command/byte enable bus
B_CBE_[1]	AE17	IO	PCI21LUS	PCIB command/byte enable bus
B_FRAME_	AE18	IO	PCI21LUS	PCIB frame
B_DEVSEL_	AE19	IO	PCI21LUS	PCIB device select
B_GNT_[4]	AE20	O	PCI21LUS	PCIB bus grant
B_REQ_[5]	AE21	I	PCI21LIS	PCIB bus request
B_REQ_[3]	AE22	I	PCI21LIS	PCIB bus request
B_REQ_[0]	AE23	I	PCI21LIS	PCIB bus request
A_SERR_	AE24	I	PCI21MIN	PCIA system error
A_GNT_[3]	AE25	O	PCI21MUN	PCIA bus grant
VSS	AE26			
VDD	AF1			
VSS	AF2			
B_AD[47]	AF3	IO	PCI21LUS	PCIB address/data bus
B_AD[44]	AF4	IO	PCI21LUS	PCIB address/data bus
VDD	AF5			
VSS	AF6			
B_AD[33]	AF7	IO	PCI21LUS	PCIB address/data bus
B_AD[28]	AF8	IO	PCI21LUS	PCIB address/data bus
B_AD[24]	AF9	IO	PCI21LUS	PCIB address/data bus
VDD	AF10			
VSS	AF11			
B_AD[13]	AF12	IO	PCI21LUS	PCIB address/data bus

TABLE 3: PBGA Pinout (Continued)

Signal Name	Ball	Direction	Cell Type	Description
B_AD[8]	AF13	IO	PCI21LUS	PCIB address/data bus
B_AD[3]	AF14	IO	PCI21LUS	PCIB address/data bus
B_CBE_[7]	AF15	IO	PCI21LUS	PCIB command/byte enable bus
VSS	AF16			
VDD	AF17			
B_TRDY_	AF18	IO	PCI21LUS	PCIB target ready
B_PERR_	AF19	IO	PCI21LUS	PCIB bus parity error
B_GNT_[3]	AF20	O	PCI21LUS	PCIB bus grant
VSS	AF21			
VDD	AF22			
B_CLK	AF23	I	PCI21LIS	PCIB bus clock phase detect (note 3)
A_REQ_[3]	AF24	I	PCI21MIN	PCIA bus request
VSS	AF25			
VDD	AF26			

(1) PCIA VDD5 - For proper noise immunity, tie to 3.3V for PCI cards which use 3V signalling, tie to 5V for PCI cards which use 5V signalling.

(2) MISC VDD5 - Tie to 5V. Internal to U2P these three pins are part of a single voltage rail.

(3) A_CLK, B_CLK - used by U2P to determine the clock phase of a given PCIA, PCIB cycle, respectively. Required since either bus can be running at half the frequency of the internal clock.

Input Buffers

U2P implements four types of input buffers:

1. TTL — UPA and JTAG inputs
2. 5V tolerant TTL — INT_NUM and TMR_CLK inputs
3. PCI — PCI inputs (5V tolerant)
4. PECL — UPA_CLK and UPA_CLK_L inputs

Note: *Refer to the Lucent Technologies HL350C 3 Volt 0.35 micron. CMOS Standard-Cell Library data book for full specification on the buffer types. Generally an input buffer is 5 Volt tolerant if it is a PCI buffer (and VDD5 is tied to 5 Volts) or if it is of type B5xxxx.*

ELECTRICAL SPECIFICATIONS

Absolute Maximum ratings

Stresses beyond those listed in the following table may cause physical damage to the device and should be avoided.

TABLE 4: Absolute Maximum Ratings

Symbol	Parameter	Limit	Unit
VDD	DC Power Supply Voltage	-0.5 to 5.0 (note 1)	V
VDD5	DC Power Supply Voltage	-0.5 to 7.0 (note 1)	V
Vin, Vout	DC Input, Output Voltage	VSS - 0.3 to VDD + 0.3 (note 2)	V
I	DC Current Drain per VDD and VSS pair	100	mA
T_{stg}	Storage Temperature	-40 to 125	°C
T_{CM}	Maximum Case Temperature	85	°C
Pd	Power dissipation	3.0	Watts

(1) The 5V supply should be powered up before the 3V supply. In any case the 5V supply should never be more than 0.4V below the 3V supply.
(2) Except 5V tolerant PCI buffers where VIN max = VDD5 + 0.3V

Recommended Operating Conditions

TABLE 5: Recommended Operating Conditions

Symbol	Parameter	Limit	Unit
VDD	DC Power Supply Voltage	3.135 to 3.465	V
VDD5	PCI input reference voltage	4.75 to 5.25 when VDD5 = 5V 3.135 to 3.465 when VDD5 = 3.3V	V
Vin, Vout	DC Input, Output Voltage	0 to VDD	V
T_{CO}	Operating CaseTemperature	0 to 70	°C

DC Characteristics

TABLE 6: DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Vil	Input Low Voltage				
	TTL			0.8	V
	PCI		-0.3	0.3 VDD	V
	PECL	UPA_CLK, UPA_CLK_L		VDD -1.475	
Vih	Input High Voltage				
	TTL		2.0		V
	PCI		0.5VDD	VDD +0.5	V
	PECL	UPA_CLK, UPA_CLK_L	VDD -1.165		
Vol	Output Low Voltage				
	TTL	Iol = -4, -8, -16 mA		0.4	V
	PCIA (DC)	Iol = 1.5 mA		0.1 VDD	V
	PCIB (DC)	Iol = 6.0 mA		0.55	V
Voh	Output High Voltage				
	TTL	Ioh = -4, -8, -16 mA	2.4		V
	PCIA (DC)	Ioh = - 0.5 mA	0.9 VDD		V
	PCIB (DC)	Ioh = - 2.0 mA	2.4		V
Iin	Input Leakage			± 1	µA
Ioz	Tri-state outputs	Voh = VSS or VDD		± 9	µA
Cin	Input Capacitance	Any input/bidir buffer	2.5	6	pF
Cout	Output Capacitance	Any output buffer	2.5	6	pF

Environmental ELectrical Protection

TABLE 7: Environmental Electrical Protection

ESD	Latch UP
Minimum	Minimum
2KV	150 mA

AC Characteristics

All UPA inputs and outputs are referenced to the PECL clock input UPA_SYS_CLK + and UPA_SYS_CLK -. This clock input also controls an on-chip Phase Lock Loop (PLL). All UPA inputs and outputs are clocked by the rising edge of CLK + at the crossover between CLK +and CLK -, where both signals are at the same voltage. All UPA inputs are applied with a rise and fall time of 1.0 ns (nanosecond).

PCI inputs and outputs are referenced to PCIA_CLK and PCIB_CLK respectively.

Other U2P internal blocks run at the PSYCLOPS_CLK, which is fixed at 66.7 MHz (15ns). There is a synchronization boundary between the UPA interface block and other internal blocks.

The JTAG signals are referenced to JTAG Test Clock PSY_TCLK. They are asynchronous signals with respect to UPA and PCI signals. The design of the U2P ASIC was done under the conditions specified in TABLE 8:.

TABLE 8: Internal Timing Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
upaclk	Operating Frequency, UPA_CLK	3.15V, Tj = 85C		100	MHz
psyclk	Operating Frequency, PSYCLOPS_CLK	3.15V, Tj = 85C		66	MHz
clkskew	Internal Skew and Jitter		- 0.5	0.5	ns

Note: *Worst Case Slow Motive claims operation of the two clock domains at the following max frequencies; upaclk = 105.9 MHz, psyclk = 67.5 MHz.*

PLL Clock Distribution and Characteristics

Figure 5. shows the PLL scheme inside the U2P.

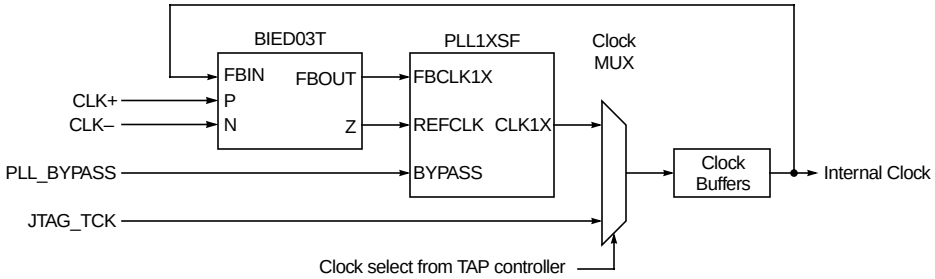


Figure 5. PLL Clock Distribution Circuitry

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TABLE 9: PLL Characteristics

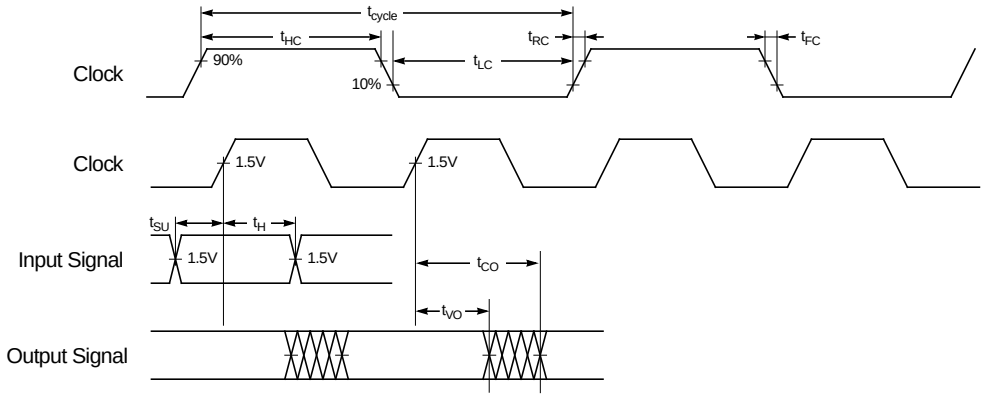
Symbol	Parameter	Conditions	Min	Max	Unit
upaclk	Operating Frequency, UPA_CLK		40	125	MHz
psyclk	Operating Frequency, PSYCLOPS_CLK		40	85	MHz
clkskew	Internal Skew and Jitter	125MHz		400	ps
		100MHz		450	ps
		66MHz		500	ps
		35MHz		600	ps

Note: *If the clock is stopped after the PLL is locked and the feedback loop is not broken, the PLL will go to the low frequency state, i.e., 4-10MHz. If the clock recovers and resumes normal operation the PLL will catch up with the input clock within 250 µsec.*

Note: *If the feedback loop is broken and the input frequency is higher than the feedback frequency, there will be run-away i.e., PLL will go to high frequency state. The only way to recover is to bring BYPASS up for 200 µsec.*

UPA Timing

A timing diagram is shown in Figure 6. as a reference for the data in the timing tables. UPA input and output signals are referenced to the rising edge of UPA_CLKTiming Diagrams



Parameter Definitions

t_{SU}: Required setup time of a chip input referenced to a given (clock) edge.

t_H : Required hold time of a chip input referenced to a given (clock) edge.

t_{CO}: Guaranteed propagation time of an output referenced to a given (clock) edge.

t_{VO}: Guaranteed output hold time of an output referenced to a given (clock) edge.

t_{HC}: Required clock high time.

t_{LC}: Required clock low time.

t_{RC}: Required clock rise time.

t_{FC}: Required clock fall time.

Figure 6. Timing Waveforms

TABLE 10: UPA_CLK Characteristics

Signal Name	Description	DC Levels	Min	Max	Unit
tcycle	Clock cycle time	$V_{IL}<V_{DD}$ - 1.475	40	100	MHz
t_{HC}	Clock high time	$V_{IH} > V_{DD}$ - 1.165	4.4		ns
t_{LC}	Clock low time		4.4		ns
t_{RC}	Clock rise time			600	ps
t_{FC}	Clock fall time			600	ps

The maximum skews between the rising edge and the falling edge of UPA_CLK + and UPA_CLK - are 50 ps. That is, the rising edge of UPA_CLK + can be shared at most 50 ps after / before the falling edge of UPA_CLK -. The falling edge of UPA_CLK + can be skewed at most 50 ps after / before the rising edge of UPA_CLK -.

TABLE 11: UPA Input and Output Timing

Signal Name	Description	Condition	Min	Max	Unit
t_{SU}	Input Setup Time		2.1		ns
t_{H}	Input Hold Time		0.5		ns
t_{CO}	Output Propagation Time	55pf	0	4.1	ns
t_{VO}	Output Hold Time	55pf	0.5		ns
t_{RI}	Input Rise Time			1.0	ns
t_{FI}	Input Fall Time			1.0	ns

Note: *Worst Case Slow Motive shows tco_max = 4.1 ns @ 70 pf.*

PCI Timing

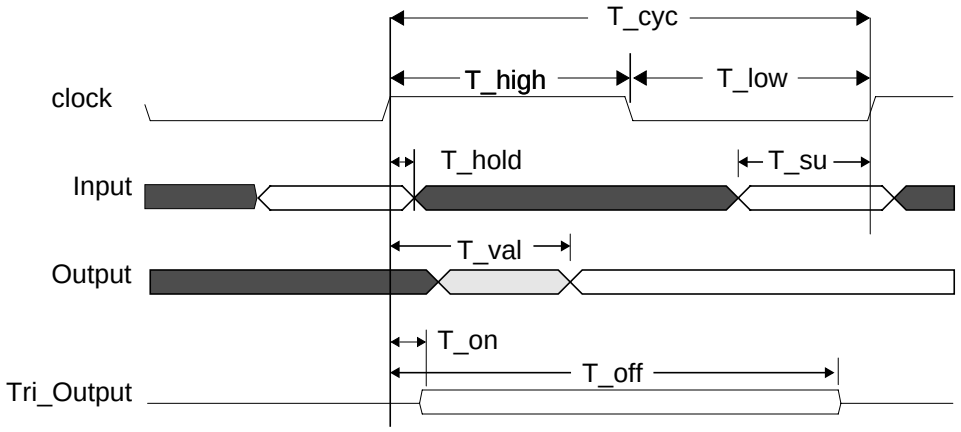


Figure 7. AC Timing Parameters

TABLE 12: PCIA AC Timing Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
T_cyc	pci_clk Cycle Time		15	30	ns
T_high	pci_clk High Time		6		ns
T_low	pci_clk Low Time		6		ns
PCI Inputs					
T_su	Input Setup Time to pci_clk - bused		5		ns
T_su(ptp)	Input Setup Time to pci_clk - pci_req_		5		ns
T_hold	Input Hold Time from pci_clk		0		ns
PCI Outputs @ 66 MHz					
T_val	pci_clk to Signal Valid Delay - bused	(See Note)	1	6	ns
T_val(ptp)	pci_clk to Signal Valid Delay - pci_req_l	(See Note)	1	6	ns
T_on	Float to Active Delay	(See Note)	1		ns
T_off	Active to Float Delay			14	ns
PCI Outputs @ 33 MHz					
T_val	pci_clk to Signal Valid Delay - bused	(See Note)	2	11	ns
T_val(ptp)	pci_clk to Signal Valid Delay - pci_req_l	(See Note)	2	12	ns
T_on	Float to Active Delay	(See Note)	2		ns
T_off	Active to Float Delay			28	ns

Note: Measurement conditions for Tval (max) rise = 25 Ohm/10pf parallel to ground, and for Tval (max) fall = 10pf to ground, 25 Ohm to VDD. Refer to PCI 2.1 Specification, Chapter 7, for full AC specifications on output buffers.

TABLE 13: PCIB AC Timing Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
T_cyc	pci_clk Cycle Time		30	DC	ns
T_high	pci_clk High Time		11		ns
T_low	pci_clk Low Time		11		ns
PCI Inputs					
T_su	Input Setup Time to pci_clk - bused		7		ns
T_su(ptp)	Input Setup Time to pci_clk - pci_req_		12		ns
T_hold	Input Hold Time from pci_clk		0		ns
PCI Outputs					
T_val	pci_clk to Signal Valid Delay - bused	(See Note)	2	11	ns

TABLE 13: PCIB AC Timing Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_val(ptp)	pci_clk to Signal Valid Delay - pci_req_l	(See Note)	2	12	ns
T_on	Float to Active Delay	(See Note)	2		ns
T_off	Active to Float Delay			28	ns

Note: Measurement conditions for Tval (max) rise = 25 Ohm/10pf parallel to ground, and for Tval (max) fall = 10pf to ground, 25 Ohm to VDD. Refer to PCI 2.1 Specification, Chapter 7, for full AC specifications on output buffers.

A_CLK, B_CLK Timing

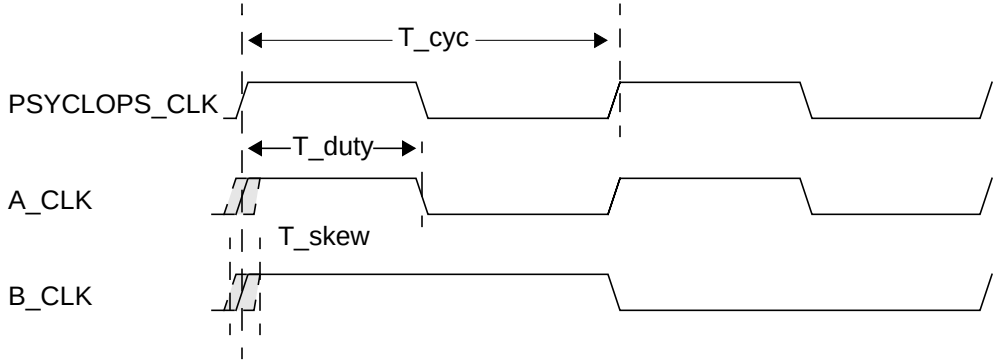


Figure 8. A_CLK, B_CLK AC timing parameters

TABLE 14: A_CLK, B_CLK timing parameters

Symbol	Parameter	Conditions	Min	Max	Unit
T_cyc	PSYCLOPS_CLK cycle time		15	25	ns
T_skew	clock skew to PSYCLOPS_CLK		-750	+750	ps
T_duty	A_CLK, B_CLK duty cycle requirement		Tcyc/2 -750	Tcyc/2 +750	ps

JTAG Timing

TABLE 15: JTAG Timing Characteristics

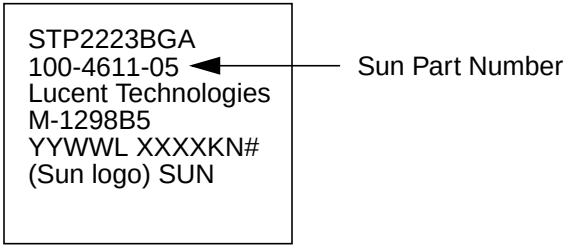
Symbol	Parameter	Conditions	Min	Max	Unit
JTAG clock					
T_cyc	JTAG clk Cycle Time		100		ns
JTAG Inputs					

TABLE 15: JTAG Timing Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_su(rx)	JTAG Inputs Setup Time to jtag_clk		30		ns
T_hld(rx)	JTAG Inputs Hold Time to jtag_clk		20		ns
T_val	JTAG Output Valid Time from jtag_clk negative edge	30pF Load		49	ns

MECHANICAL INFORMATION

Package Marking (Production Version)



YYWW	Year and Work Week
L	Assembly site
XXXX	Wafer Lot
KN	Clean Room number
#	Chip version

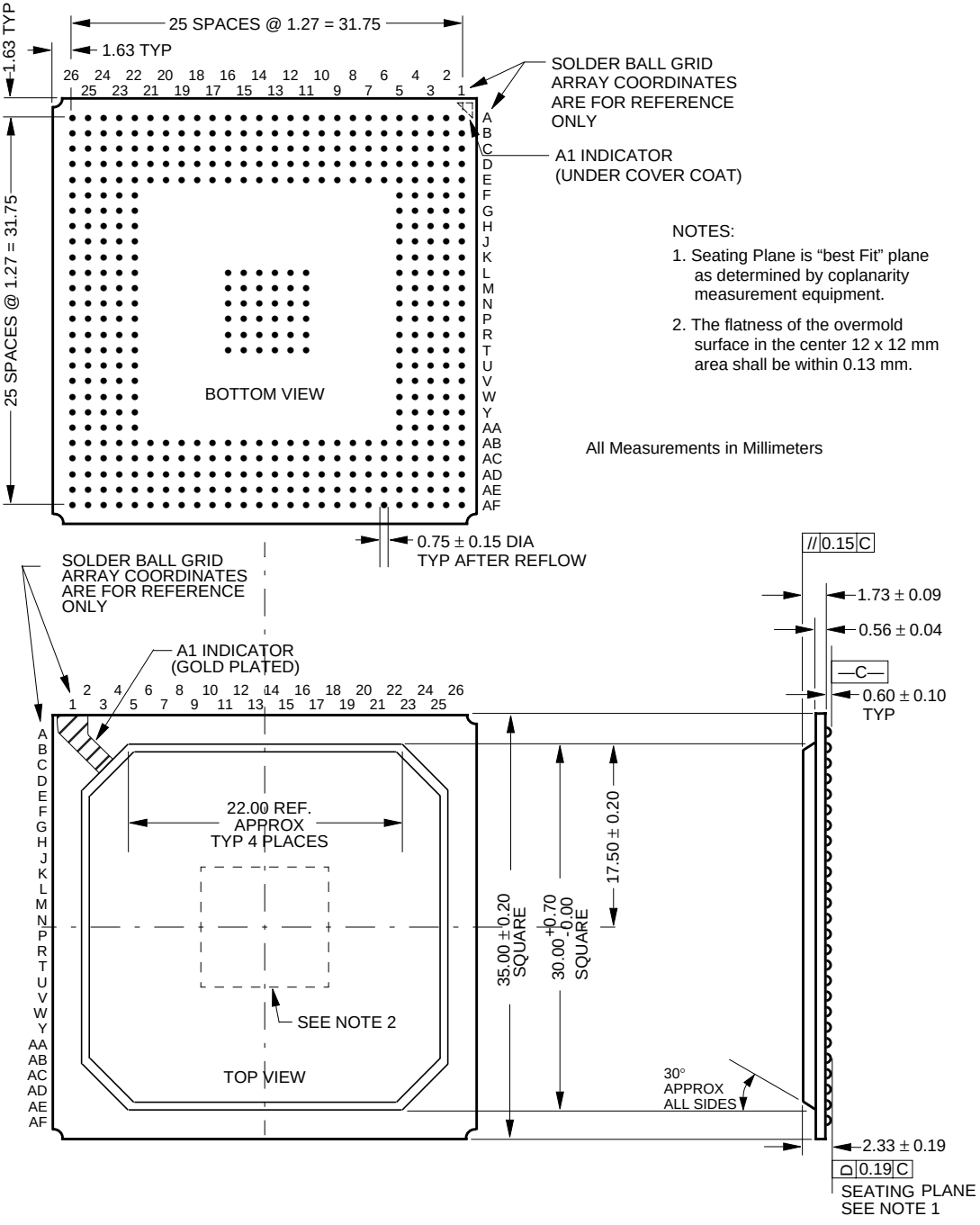
Thermal Data and Characteristics

TABLE 16: Thermal Characteristics

Package type	Theta_JA	Theta_JC	Unit
456 PBGA/4 layers	12.8 (1)	3.7	°C/W
	11.8 (2)		

(1) 0 LFM, no heatsink, 4W thermal die, 20°C ambient, sea level
(2) 100 LFM, no heatsink, 4W thermal die, 20°C ambient, sea level

Package Drawing



ORDERING INFORMATION

Part Number	Speed	Description
STP2223BGA		UPA to PCI Interface

Document Part Number: 802-7834-02