

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (L^2 - π -MOSV)

2SK2311

Unit: mm

Chopper Regulator, DC-DC Converter and Switching Regulator Applications

- 4-V gate drive
- Low drain-source ON resistance : $R_{DS(ON)} = 36 \text{ m}\Omega$ (typ.)
- High forward transfer admittance : $|Y_{fs}| = 16 \text{ S}$ (typ.)
- Low leakage current : $I_{DSS} = 100 \text{ }\mu\text{A}$ (max) ($V_{DS} = 60 \text{ V}$)
- Enhancement mode : $V_{th} = 0.8 \sim 2.0 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	60	V
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	V_{DGR}	60	V
Gate-source voltage	V_{GSS}	± 20	V
Drain current	DC (Note 1)	I_D	A
	Pulse (Note 1)	I_{DP}	A
Drain power dissipation ($T_c = 25^\circ\text{C}$)	P_D	40	W
Single pulse avalanche energy (Note 2)	E_{AS}	156	mJ
Avalanche current	I_{AR}	25	A
Repetitive avalanche energy (Note 3)	E_{AR}	3.5	mJ
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature range	T_{stg}	$-55 \sim 150$	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Thermal Characteristics

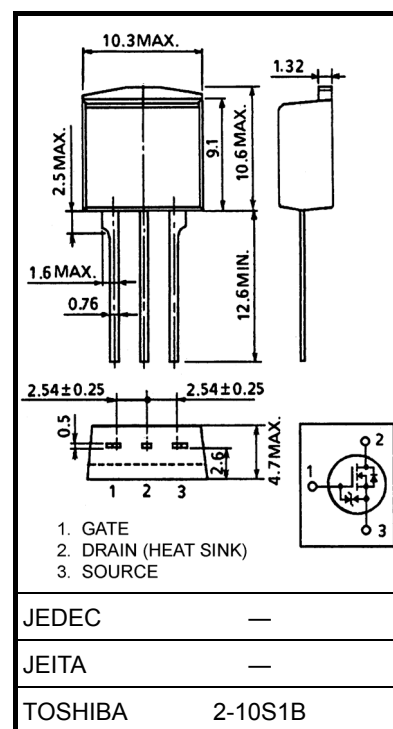
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	3.125	$^\circ\text{C} / \text{W}$
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	83.3	$^\circ\text{C} / \text{W}$

Note 1: Ensure that the channel temperature does not exceed 150°C .

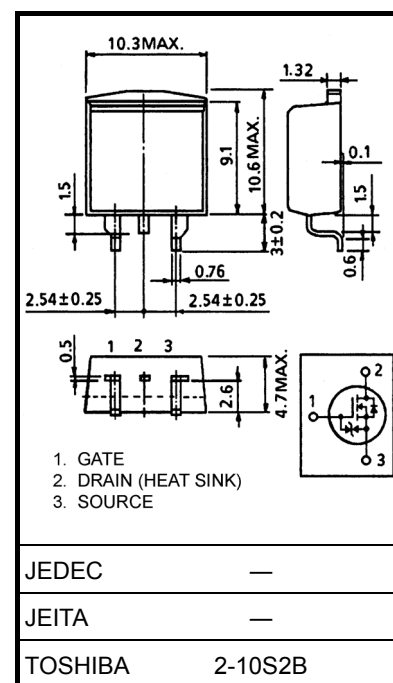
Note 2: $V_{DD} = 25 \text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 339 \text{ }\mu\text{H}$, $R_G = 25 \text{ }\Omega$, $I_{AR} = 25 \text{ A}$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device.
Please handle with caution.

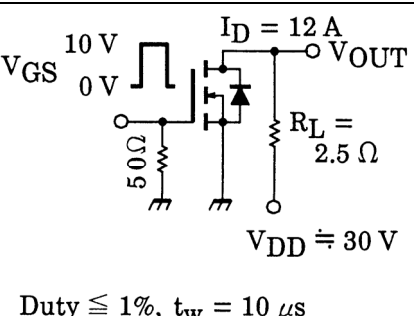


Weight: 1.5 g (typ.)



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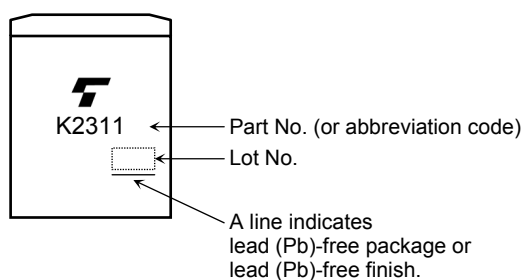
Electrical Characteristics (Ta = 25°C)

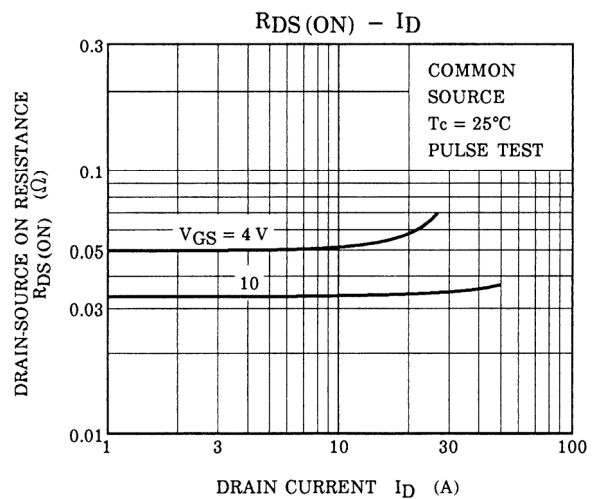
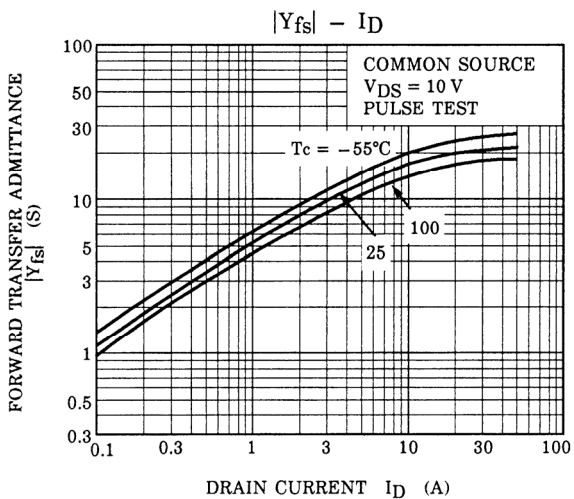
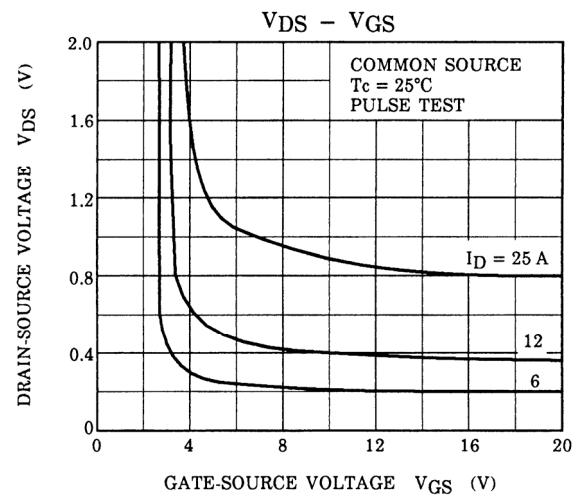
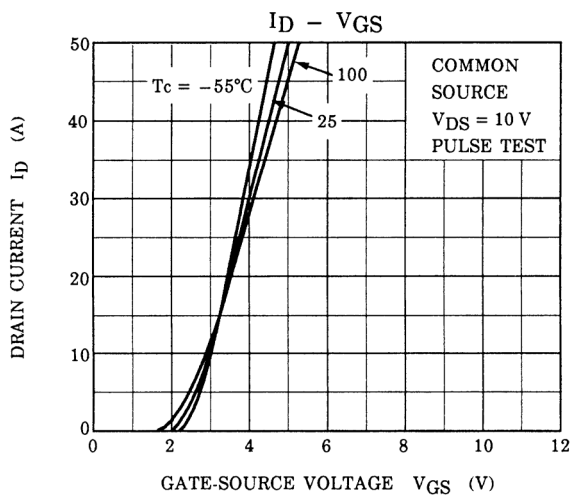
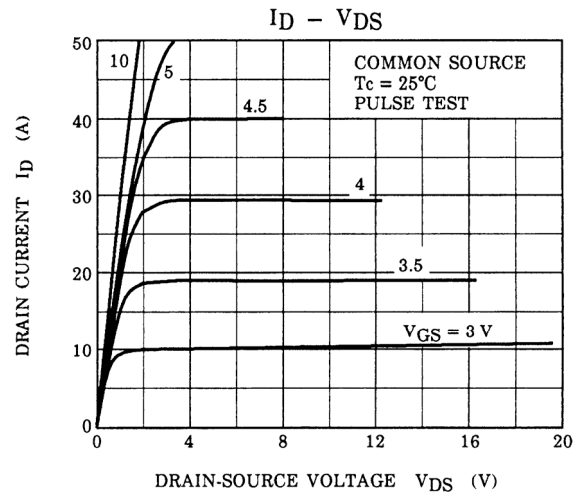
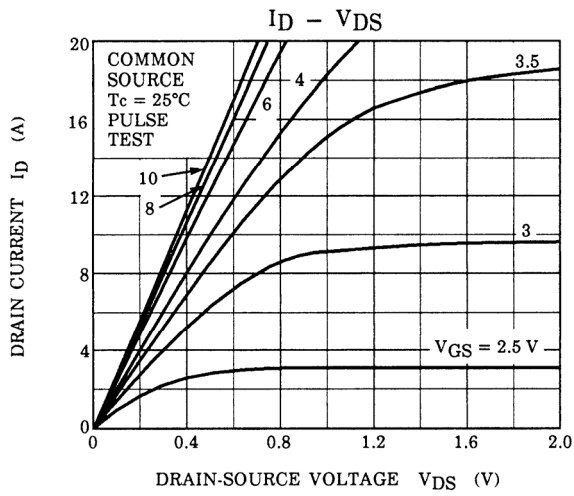
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 10	μA
Drain cut-off current		I_{DSS}	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR) DSS}$	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	60	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$	0.8	—	2.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 4 \text{ V}, I_D = 12 \text{ A}$	—	57	80	m Ω
			$V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$	—	36	46	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10 \text{ V}, I_D = 12 \text{ A}$	10	16	—	S
Input capacitance		C_{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	1000	—	pF
Reverse transfer capacitance		C_{rss}		—	200	—	
Output capacitance		C_{oss}		—	550	—	
Switching time	Rise time	t_r		—	20	—	ns
	Turn-on time	t_{on}		—	30	—	
	Fall time	t_f		—	55	—	
	Turn-off time	t_{off}		—	130	—	
Total gate charge (Gate-source plus gate-drain)		Q_g	$V_{DD} \approx 48 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 25 \text{ A}$	—	38	—	nC
Gate-source charge		Q_{gs}		—	25	—	
Gate-drain ("miller") charge		Q_{gd}		—	13	—	

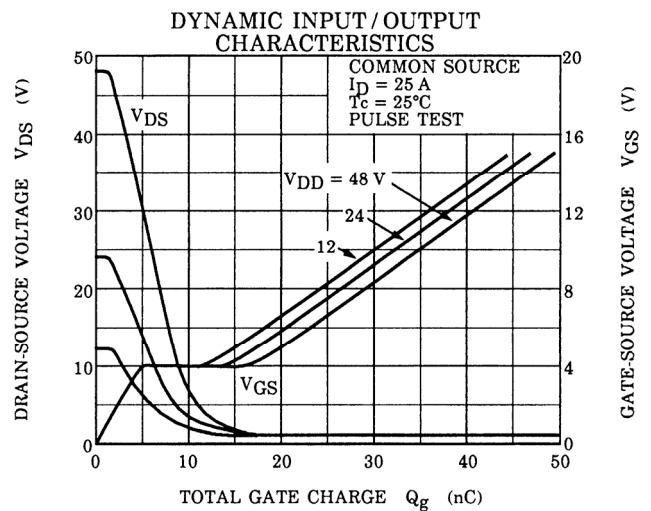
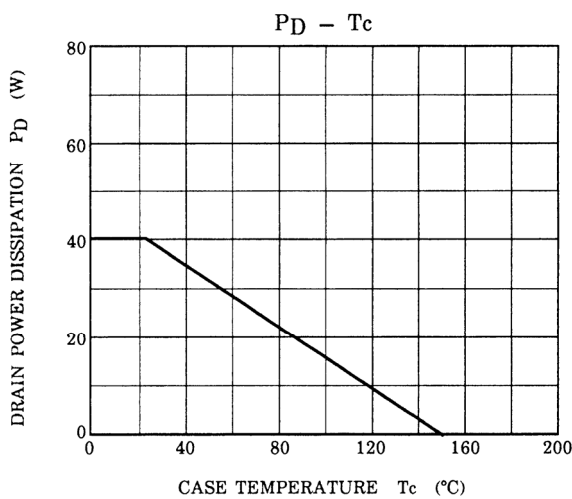
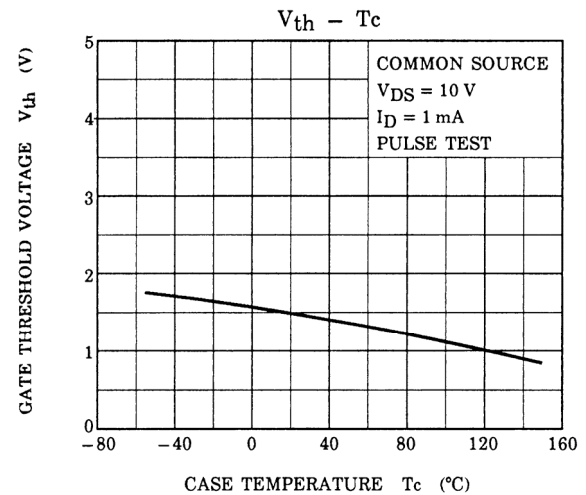
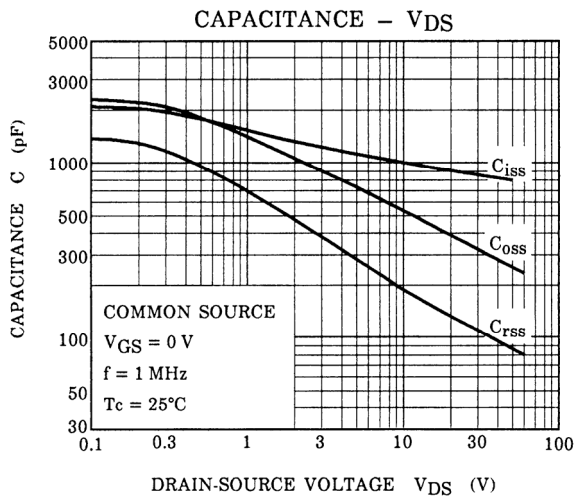
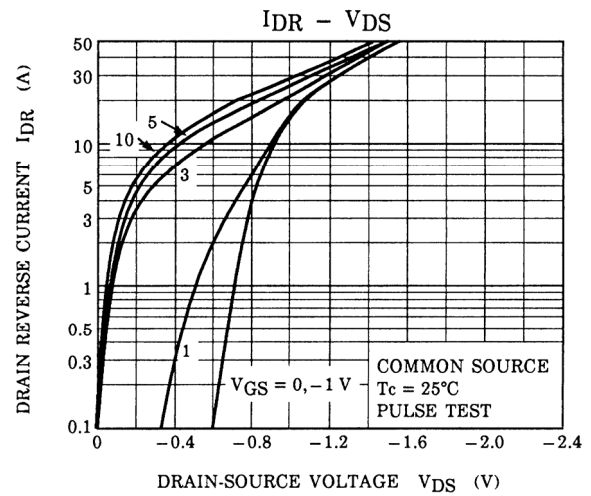
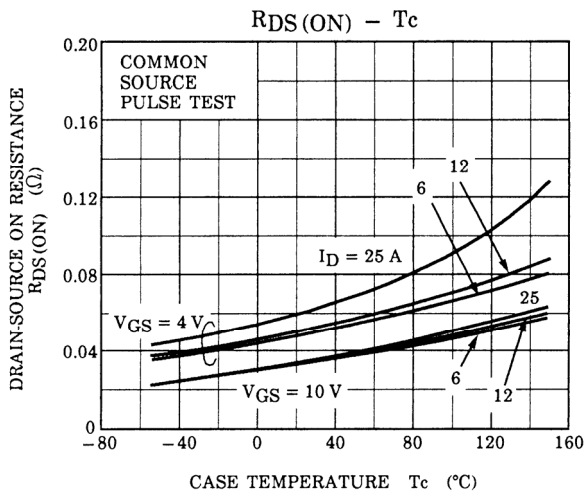
Source-Drain Ratings and Characteristics (Ta = 25°C)

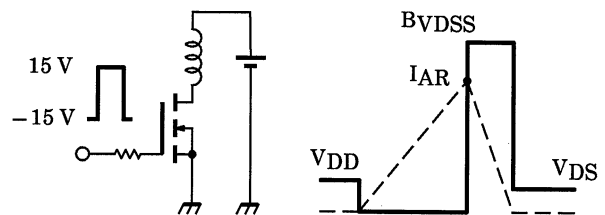
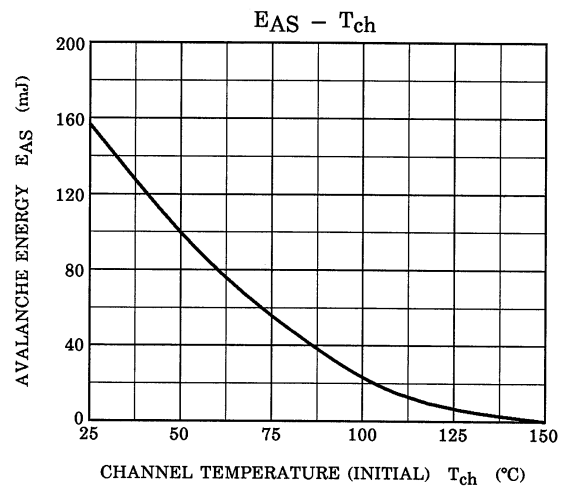
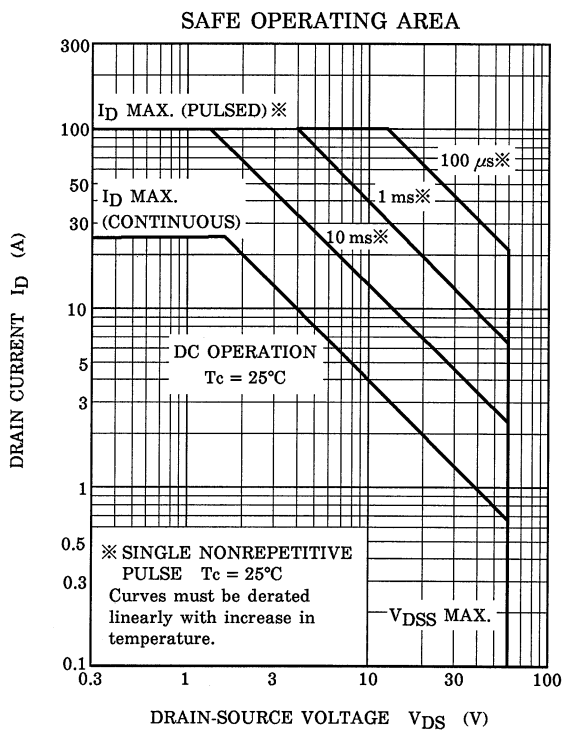
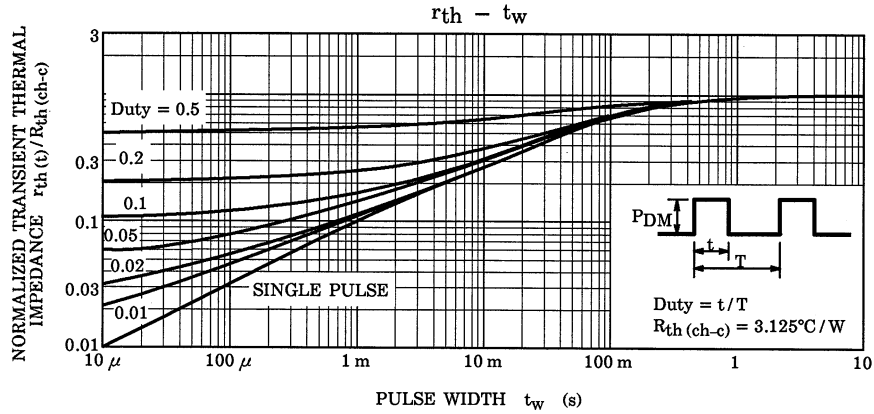
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	25	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	100	A
Forward voltage (diode)	V_{DSF}	$I_{DR} = 25 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	-1.8	V
Reverse recovery time	t_{rr}	$I_{DR} = 25 \text{ A}, V_{GS} = 0 \text{ V}$	—	50	—	ns
Reverse recovery charge	Q_{rr}	$dI_{DR} / dt = 50 \text{ A} / \mu\text{s}$	—	35	—	μC

Marking









TEST CIRCUIT

WAVE FORM

$$R_G = 25 \, \Omega$$

$$V_{DD} = 25 \, \text{V}, L = 339 \, \mu\text{H}$$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{BVDSS}{BVDSS - V_{DD}} \right)$$

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20070701-EN

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