Improved Quad SPST CMOS Analog Switches

DESCRIPTION

The DG441B, DG442B are monolithic quad analog switches designed to provide high speed, low error switching of analog and audio signals. The DG441B, DG442B are upgrades to the original DG441, DG442.

Combing low on-resistance (45 Ω, typ.) with high speed (t_{ON} 120 ns, typ.), the DG441B, DG442B are ideally suited for Data Acquisition, Communication Systems, Automatic Test Equipment, or Medical Instrumentation. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

The DG441B, DG442B are built using Vishay Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

When on, each switch conducts equally well in both directions and blocks input voltages to the supply levels when off.

FEATURES

- **Halogen-free according to IEC 61249-2-21 Definition**
- Low On-Resistance: 45 Ω
- Low Power Consumption: 1 mW
- Fast Switching Action - t_{ON}: 120 ns
- Low Charge Injection - Q: - 1 pC
- TTL/CMOS-Compatible Logic
- Single Supply Capability
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE

BENEFITS

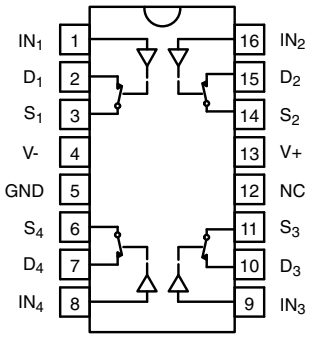
- Less Signal Errors and Distortion
- Reduced Power Supply Requirements
- Faster Throughput
- Reduced Pedestal Errors
- Simple Interfacing

APPLICATIONS

- Audio Switching
- Data Acquisition
- Sample-and-Hold Circuits
- Communication Systems
- Automatic Test Equipment
- Medical Instruments

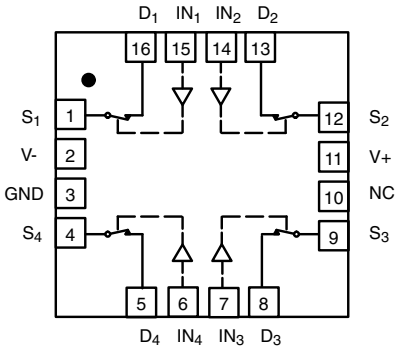
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG441B
Dual-In-Line and SOIC



Top View

DG441B
QFN16 (4 x 4 mm)



Top View

TRUTH TABLE

Logic	DG441B	DG442B
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 °C to 85 °C	16-pin Plastic DIP	DG441BDJ
		DG441BDJ-E3
		DG442BDJ
		DG442BDJ-E3
	16-pin Narrow SOIC	DG441BDY-E3
		DG441BDY-T1-E3
		DG442BDY-E3
		DG442BDY-T1-E3
	16 pin QFN 4 x 4 mm	DG441BDN-T1-E4
		DG442BDN-T1-E4

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ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
V+ to V-			44	V
GND to V-			25	
Digital Inputs[a], V_S, V_D			(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Continuous Current (Any Terminal)			30	mA
Current, S or D (Pulsed at 1 ms, 10 % duty cycle)			100	
Storage Temperature			- 65 to 125	°C
Power Dissipation (Package)[b]	16-pin Plastic DIP[c]		470	mW
	16-pin Narrow Body SOIC[d]		900	
	QFN-16[d]		850	

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75 °C.
d. Derate 12 mW/°C above 75 °C.

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SPECIFICATIONS[a] (for dual supplies)							
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 15 V, V- = - 15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	**Temp.**[b]	**Limits** - 40 °C to 85 °C **Min.**[d]	**Typ.**[c]	**Max.**[d]	**Unit**
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	- 15		15	V
Drain-Source On-Resistance	$R_{DS(on)}$	I_S = 1 mA, V_D = ± 10 V	Room Full		45	80 95	Ω
On-Resistance Match Between Channels[e]	$\Delta R_{DS(on)}$	I_S = 1 mA, V_D = ± 10 V	Room Full		2	4 5	Ω
Switch Off Leakage Current	$I_{S(off)}$	V_D = ± 14 V, V_S = ± 14 V	Room Full	- 0.5 - 5	± 0.01	0.5 5	nA
	$I_{D(off)}$		Room Full	- 0.5 - 5	± 0.01	0.5 5	nA
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = ± 14 V	Room Full	- 0.5 - 10	± 0.02	0.5 10	nA
Digital Control							
Input Voltage Low	V_{INL}		Full			0.8	V
Input Voltage High	V_{INH}		Full	2.4			V
Input Current V_{IN} Low	I_{INL}	V_{IN} under test = 0.8 V All Other = 2.4 V	Full	- 1	- 0.01	1	µA
Input Current V_{IN} High	I_{INH}	V_{IN} under test = 2.4 V All Other = 0.8 V	Full	- 1	0.01	1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF V_S = 10 V, See Figure 2	Room		120	220	ns
Turn-Off Time	t_{OFF}		Room		65	120	ns
Charge Injection[e]	Q	C_L = 1 nF, V_S = 0 V V_{gen} = 0 V, R_{gen} = 0 Ω	Room		- 1		pC
Off Isolation[e]	OIRR	R_L = 50 Ω , C_L = 15 pF V_S = 1 V_{RMS}, f = 100 kHz	Room		- 90		dB
Crosstalk (Channel-to-Channel)	X_{TALK}		Room		- 95		dB
SourceOff Capacitance[e]	$C_{S(off)}$	f = 1 MHz	Room		4		pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room		4		pF
Channel On Capacitance[e]	$C_{D(on)}$	V_S = V_D = 0 V, f = 1 MHz	Room		16		pF
Power Supplies							
Positive Supply Current	I+	V+ = 16.5 V, V- = - 16.5 V V_{IN} = 0 or 5 V	Room Full			1 5	µA
Negative Supply Current	I-		Room Full	- 1 - 5			µA

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SPECIFICATIONS (for single supply)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V- = 0 V V_{IN} = 2.4 V, 0.8 V[e]	Temp.[b]	Limits - 40 °C to 85 °C Min.[d]	Typ.[c]	Max.[d]	Unit
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	0		12	V
Drain-Source On-Resistance	$R_{DS(on)}$	I_S = 1 mA, V_D = 3 V, 8 V	Room Full		90	160 200	Ω
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, V_S = 8 V See Figure 2	Room		120	300	ns
Turn-Off Time	t_{OFF}		Room		60	200	
Charge Injection	Q	C_L = 1 nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room		4		pC
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 V or 5 V	Room Full			1 5	µA
Negative Supply Current	I-		Room Full	- 1 - 5			

Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM (typical channel)

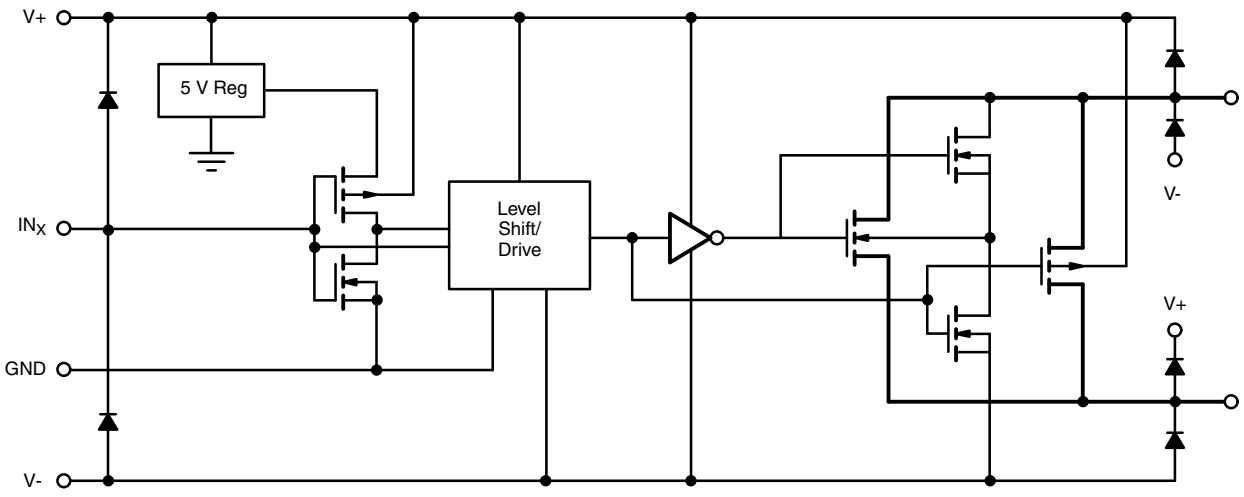
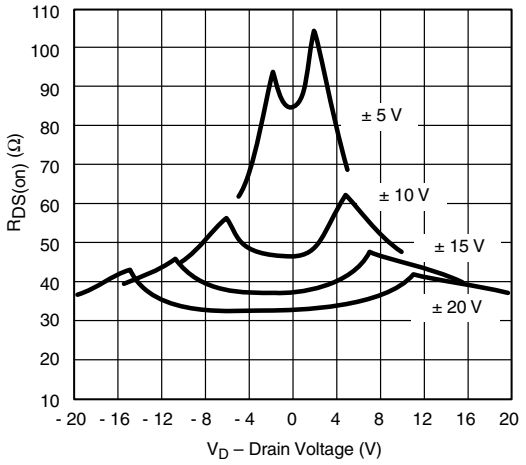


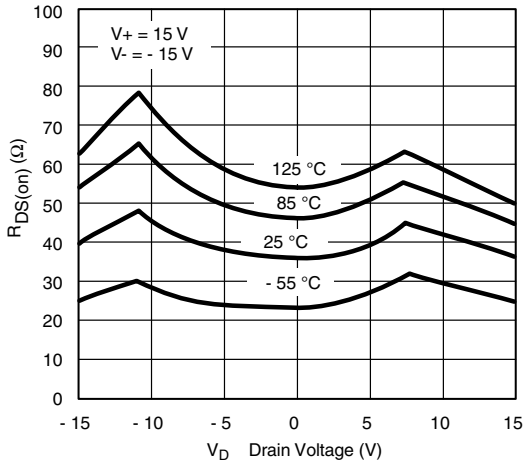
Figure 1.

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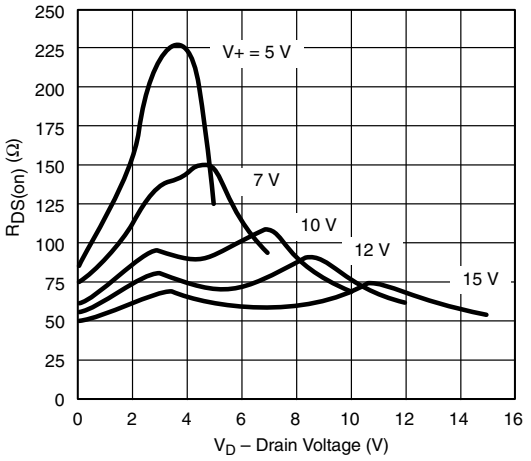
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



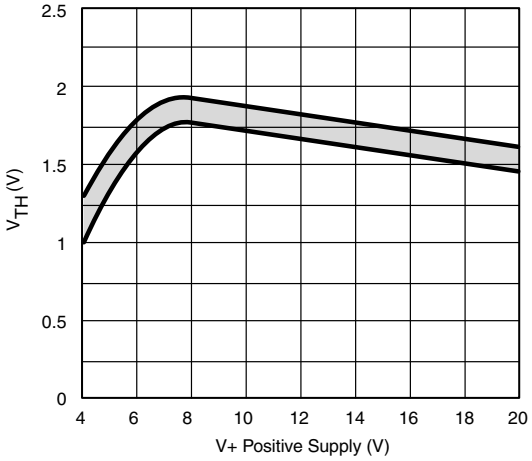
$R_{DS(on)}$ vs. V_D and Power Supply Voltages



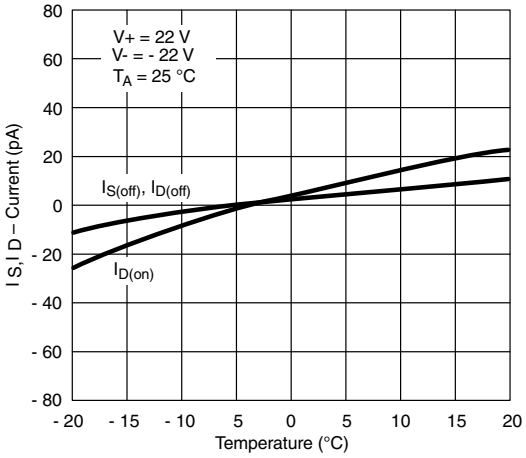
$R_{DS(on)}$ vs. V_D and Temperature



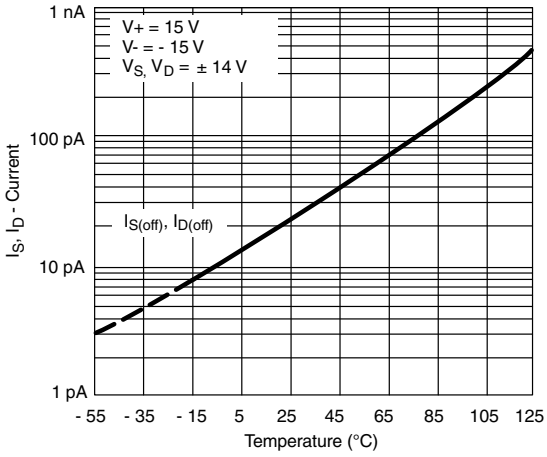
$R_{DS(on)}$ vs. V_D and Single Power Supply Voltages



Input Switching Threshold vs. Supply Voltage



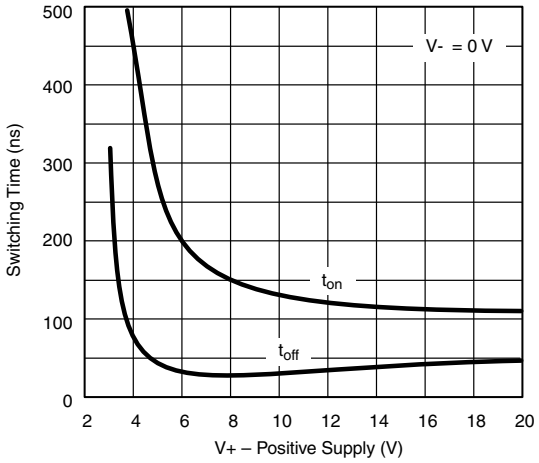
Leakage Currents vs. Analog Voltage



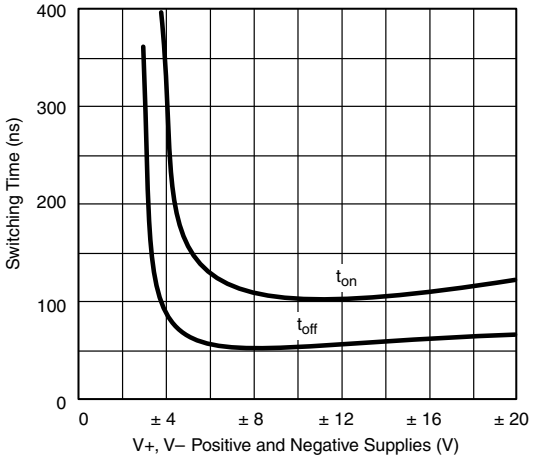
Leakage Currents vs. Temperature

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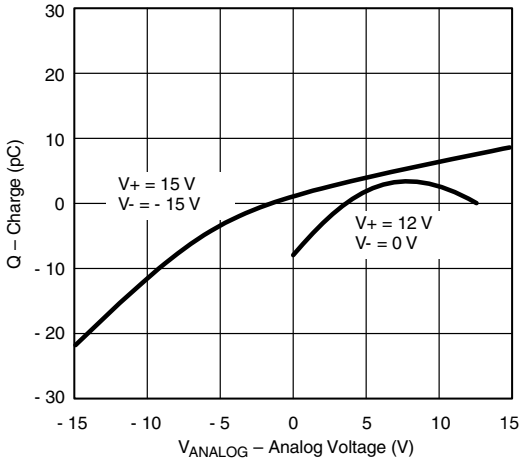
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



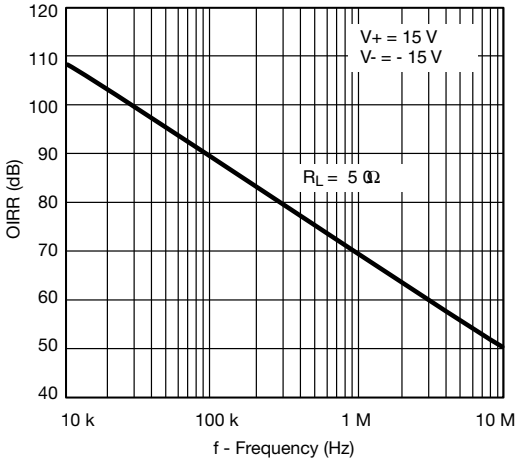
Switching Time vs. Single Supply Voltage



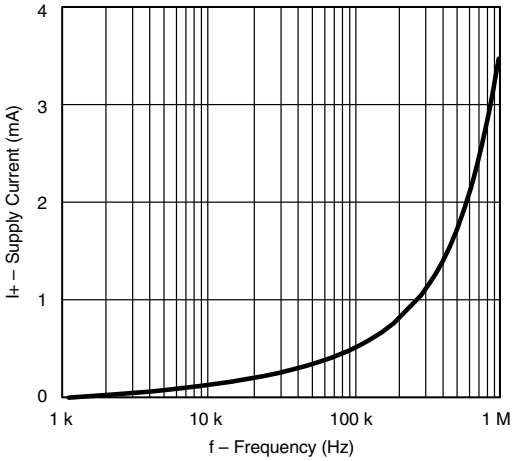
Switching Times vs. Power Supply Voltage



Q_S, Q_D - Charge Injection vs. Analog Voltage



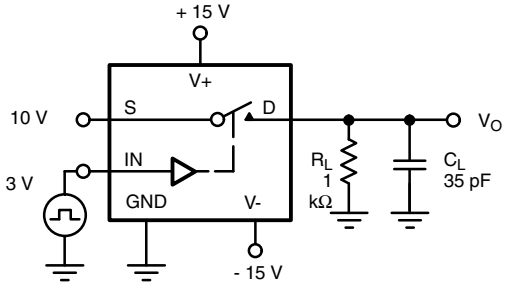
Off Isolation vs. Frequency



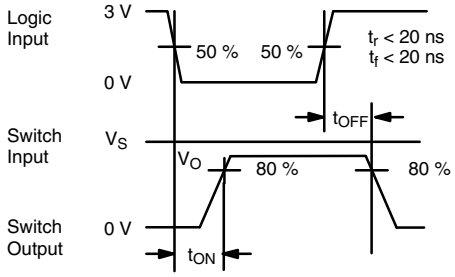
Supply Current vs. Switching Frequency

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TEST CIRCUITS

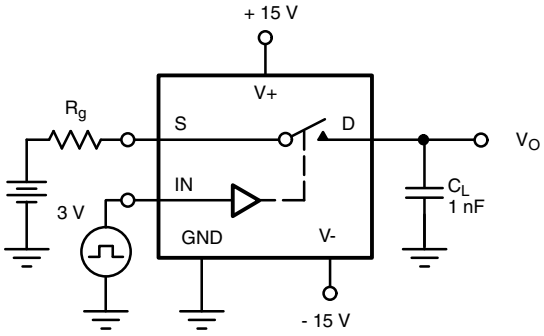


C_L (includes fixture and stray capacitance)



Note: Logic input waveform is inverted for DG442.

Figure 2. Switching Time



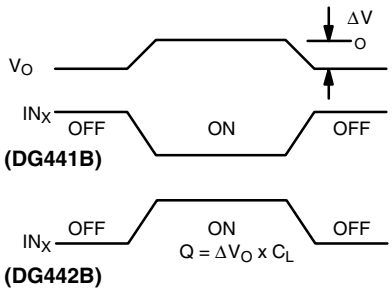
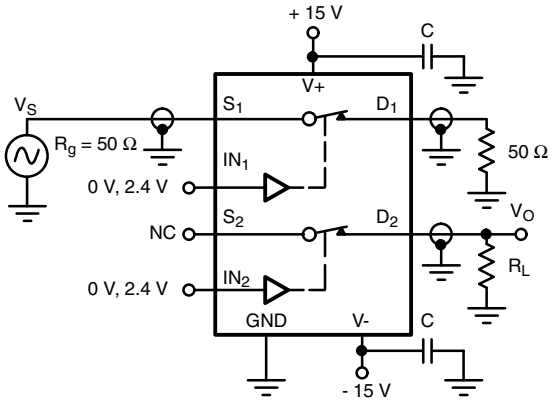


Figure 3. Charge Injection

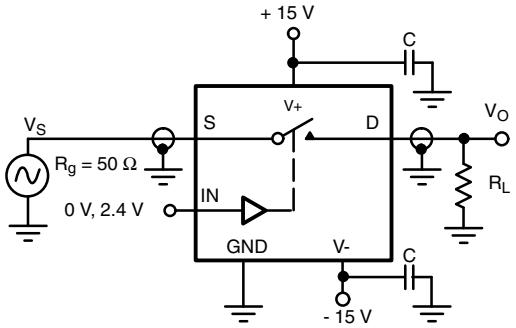
C = 1 mF tantalum in parallel with 0.01 mF ceramic



X_{TALK} Isolation = 20 log $\left|\frac{V_S}{V_O}\right|$

C = RF bypass

Figure 4. Crosstalk



Off Isolation = 20 log $\left|\frac{V_S}{V_O}\right|$

Figure 5. Off Isolation

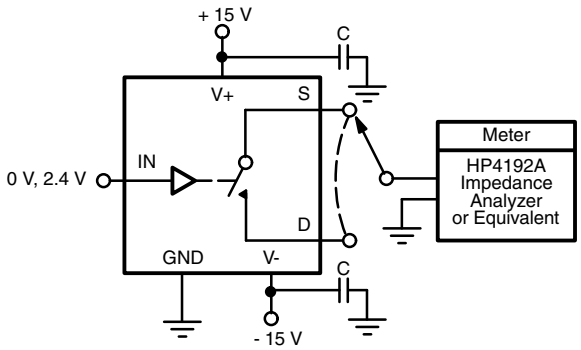


Figure 6. Source/Drain Capacitances

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APPLICATIONS

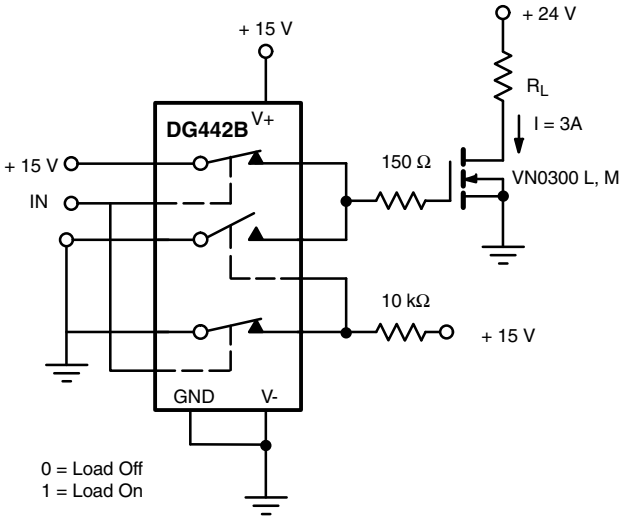


Figure 7. Power MOSFET Driver

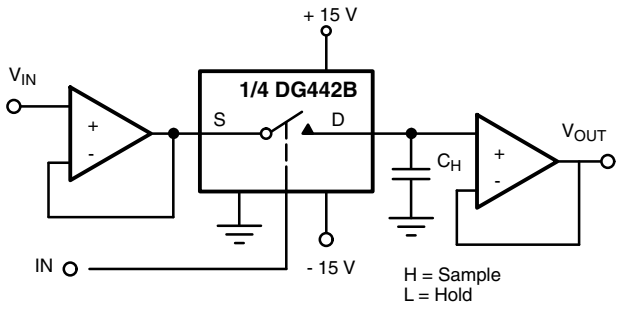


Figure 8. Open Loop Sample-and-Hold

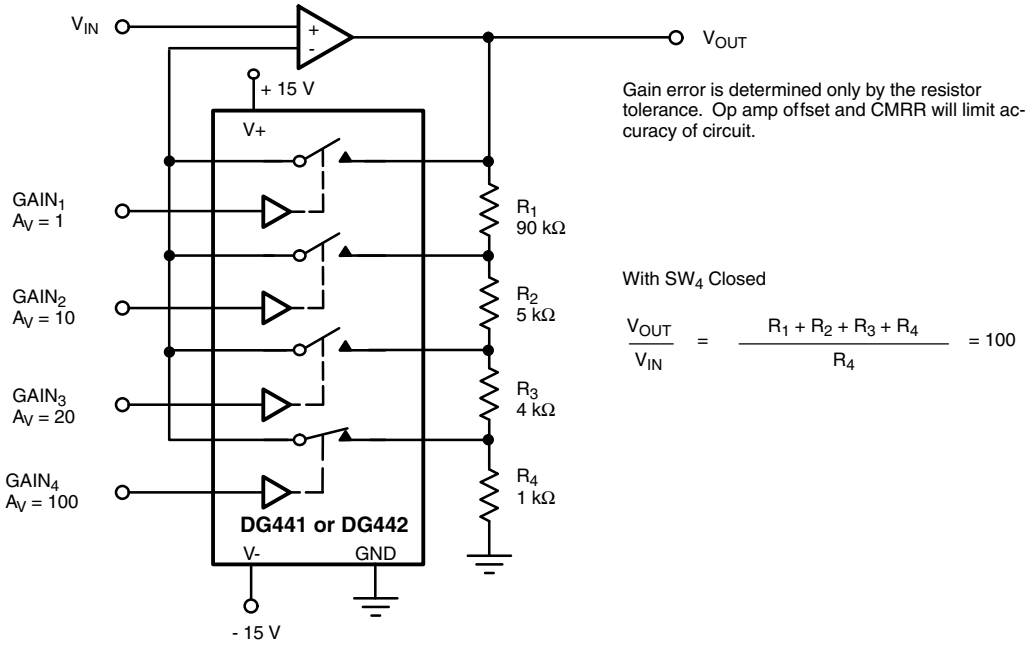


Figure 9. Precision-Weighted Resistor Programmable-Gain Amplifier

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72625.

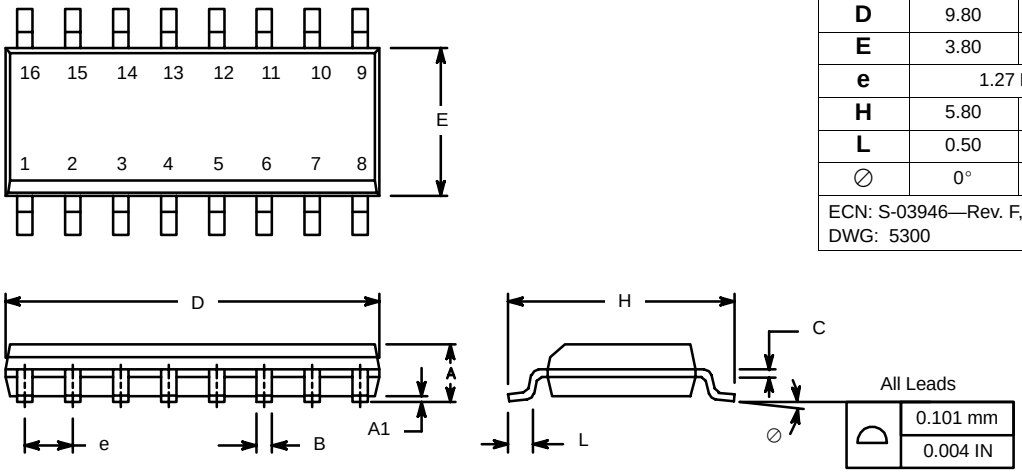
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SOIC (NARROW): 16-LEAD

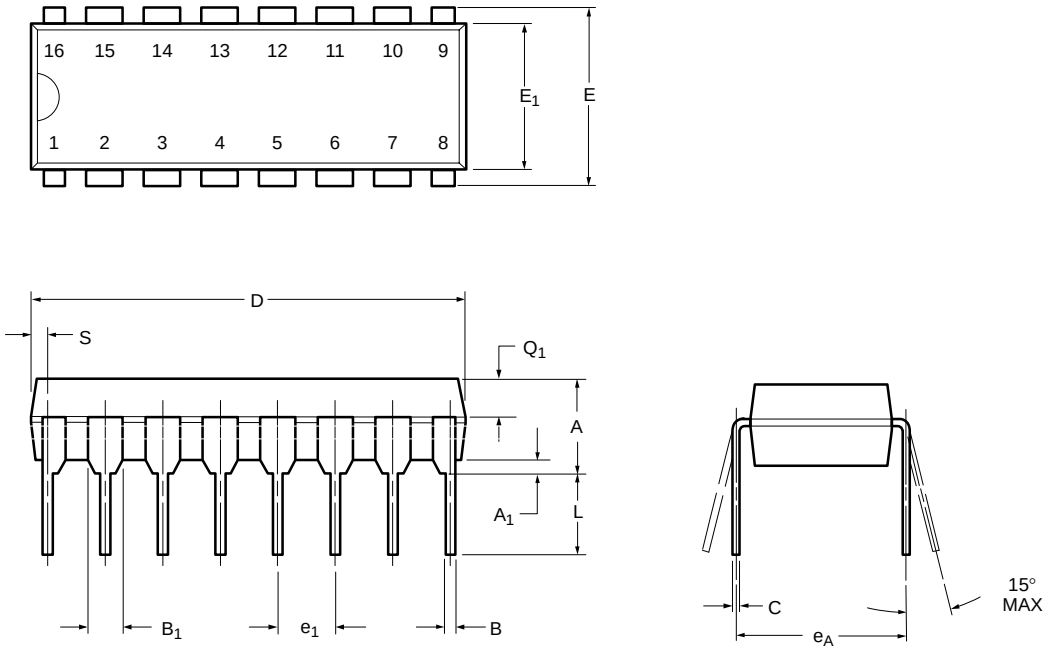
JEDEC Part Number: MS-012

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



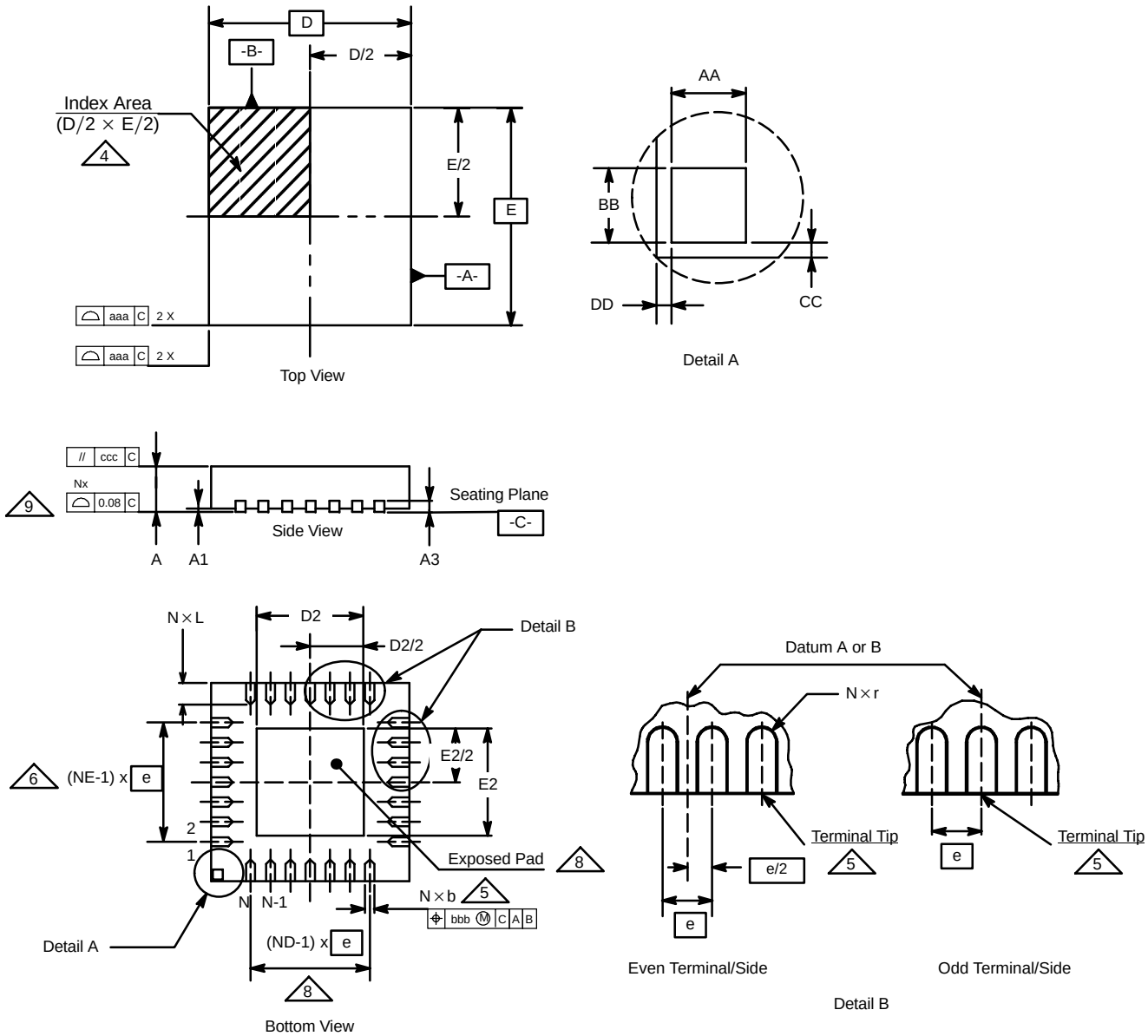
PDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5482				

QFN-16 (4 × 4 mm)

JEDEC Part Number: MO-220



QFN-16 (4 × 4 mm)
JEDEC Part Number: MO-220

Dim	MILLIMETERS*			INCHES			Notes
	Min	Nom	Max	Min	Nom	Max	
A	0.80	0.90	1.00	0.0315	0.0354	0.0394	
A1	0	0.02	0.05	0	0.0008	0.0020	
A3	-	0.20 Ref	-	-	0.0079	-	
AA	-	0.345	-	-	0.0136	-	
aaa	-	0.25	-	-	0.0098	-	
BB	-	0.345	-	-	0.0136	-	
b	0.23	0.30	0.38	0.0091	0.0118	0.0150	5
bbb	-	0.10	-	-	0.0039	-	
CC	-	0.18	-	-	0.0071	-	
ccc	-	0.10	-	-	0.0039	-	
D		4.00 BSC			0.1575 BSC		
D2	2.00	2.15	2.25	0.0787	0.0846	0.0886	
DD	-	0.18	-	-	0.0071	-	
E		4.00 BSC			0.1575 BSC		
E2	2.00	2.15	2.25	0.0787	0.0846	0.0886	
e		0.65 BSC			0.0256 BSC		
L	0.45	0.55	0.65	0.0177	0.0217	0.0256	
N		16			16		3, 7
ND	-	4	-	-	4	-	6
NE	-	4	-	-	4	-	6
r	b(min)/2	-	-	b(min)/2	-	-	

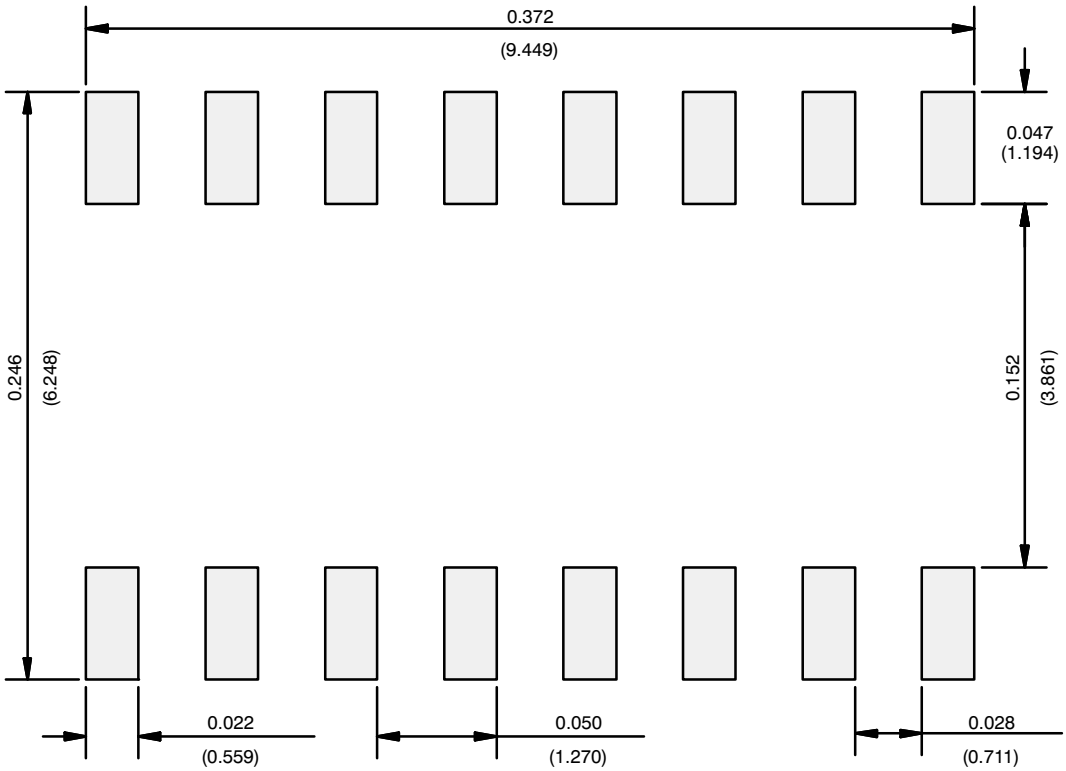
* Use millimeters as the primary measurement.

ECN: S-21437—Rev. A, 19-Aug-02
DWG: 5890

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. All angels are in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a molded or marked feature. The X and Y dimension will vary according to lead counts.
5. Dimension b applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip.
6. ND and NE refer to the number of terminals on the D and E side respectively.
7. Depopulation is possible in a symmetrical fashion.
8. Variation HHD is shown for illustration only.
9. Coplanarity applies to the exposed heat sink slug as well as the terminals.

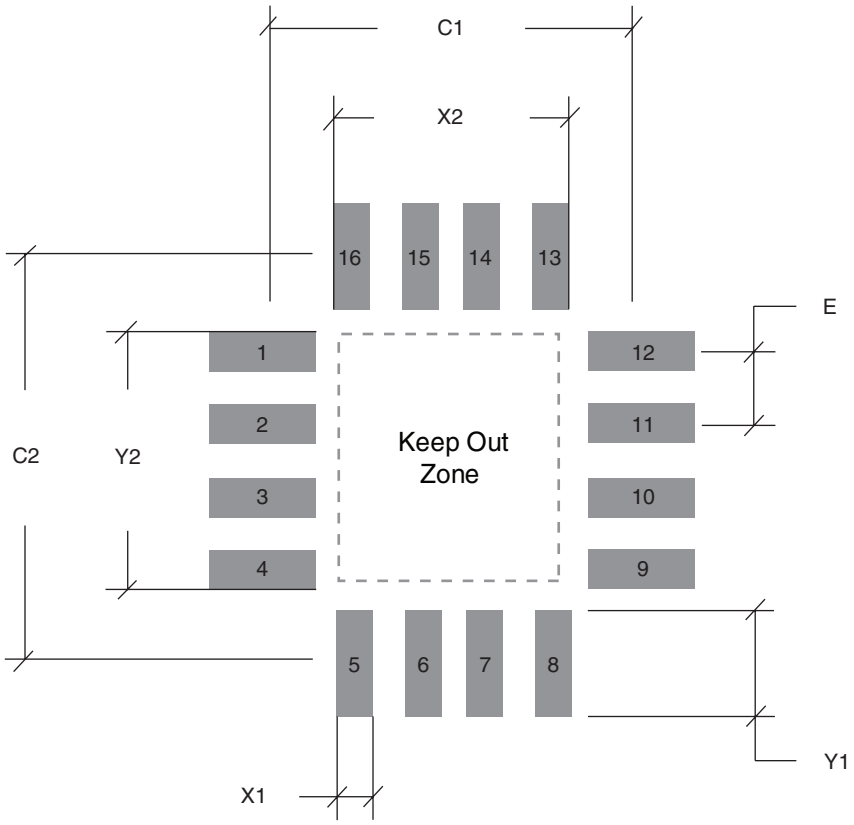
RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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RECOMMENDED MINIMUM PADS FOR QFN-16 (4 x 4 MM BODY)



	Inches	Millimeters
C1	0.142	3.60
C2	0.142	3.60
E	0.026	0.65
X1	0.014	0.35
X2	0.089	2.25
Y1	0.037	0.95
Y2	0.089	2.25

Note:
QFN-16 (4 x 4) has an exposed center pad that must not come into contact with any metalized structure on the PCB. This area is considered a Keep Out Zone.

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