

Single Chip PAL Luminance/Chroma Processor

May 1997

NOT RECOMMENDED FOR NEW DESIGNS

Features

- All PAL Luminance and Chrominance Processing Circuitry on a Single Chip in a 24-Lead Plastic Package
- Phase-Locked Subcarrier Regeneration Utilizing Sample-and-Hold
- DC Controls for Brightness, Contrast, and Color Saturation Functions
- Input for Average Beam-Current Limiting
- Contrast Control Having Excellent Tracking of Luma and Chroma Channels
- Low-Impedance RGB Outputs with Excellent Tracking for Direct Coupling to Video Driver Circuitry

Description

The Harris CA3194E is a silicon monolithic integrated circuit designed to perform all of the signal processing functions for both the chroma and luminance signals of PAL color television receivers.

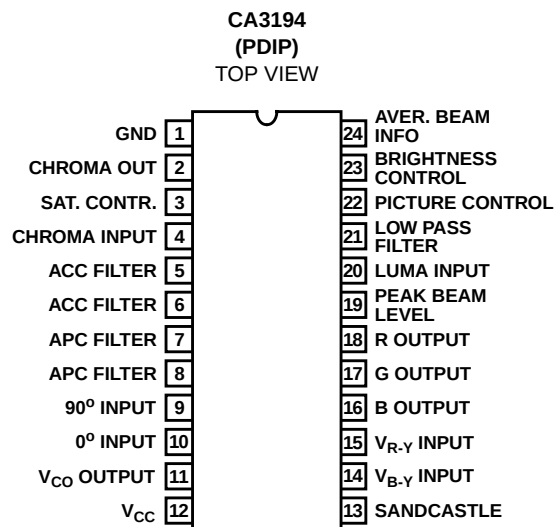
This circuit performs all the functions needed between the video detector and the video RGB output stages. DC contrast, brightness, and saturation controls and average beam limiting functions are included. The RGB buffer stages are capable of delivering 5mA of current into the video output stages.

NOTE: Formerly Dev. No. TA10313.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3194E	-40°C to +85°C	24 Lead PDIP

Pinout



TERMINAL VOLTAGE AND CURRENT RATINGS

TERMINAL	VOLTAGE (NOTE 1) -V		CURRENT - mA	
	MIN	MAX	I _{IN}	I _{OUT}
1	-	-	-	-
2	0	13	0	30
3	0	8	10	-
4	0	5	-	-
5	0	Note	-	-
6	-	-	0.1	0.5
7	0	Note	-	-
8	0	Note	-	-
9	0	8	-	-
10	0	8	-	0.7
11	0	13	-	10
12	0	13	-	-
13	0	12	-	-
14	0	5	-	1.5
15	0	5	-	1.5
16	0	13	-	10
17	0	13	-	10
18	0	13	-	10
19	0	Note	-	-
20	0	5	-	-
21	0	Note	-	-
22	0	8	-	-
23	0	5	-	-
24	0	12	-	-

NOTE:

1. The maximum should not exceed the V_{CC} voltage. Voltage with respect to Terminal 1 for V_{CC} (Terminal 12) of 12V ±10%.

Specifications CA3194

Absolute Maximum Ratings

Supply Voltage and Current
 Pin 12 Voltage Range 11V (Min) to 13V (Max)
 Pin 12 Current Range 44mA (Typ) to 60mA (Max)
 Power Dissipation
 Up to $T_A = +25^{\circ}\text{C}$ 825mW
 Above $T_A = +25^{\circ}\text{C}$ Derate Linearly 8.7mW/ $^{\circ}\text{C}$
 Junction Temperature (Plastic Package) $+150^{\circ}\text{C}$
 Storage Temperature Range -65°C to $+150^{\circ}\text{C}$
 Lead Temperature (Soldering 10s) $+300^{\circ}\text{C}$

Operating Conditions

Operating Temperature Range -40°C to $+85^{\circ}\text{C}$
 Thermal Package Characteristics ($^{\circ}\text{C}/\text{W}$)
 PDIP Package 115

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_A = +25^{\circ}\text{C}$, $V_{CC} = 12\text{V}$, $V_S = 2.85\text{V}$, $V_C = 2.85\text{V}$, $V_{AB} = V_{PB} = V_{CC}$, V_B adjusted for $V_{18} = 6.3\text{V}$, C_X adjusted for $F_{OSC} = 4.43361875\text{MHz}$, Sandcastle: $V_{BG} = 8.0\text{V}$, $V_{BLANK} = 3.5\text{V}$ - Burst Gate centered on Burst.
 These conditions exist except as otherwise noted. See Figure 19 for test circuit

PARAMETER	TEST CONDITIONS	TYPICAL VALUE	UNITS
LUMINANCE SECTION			
Input Impedance (Terminal 20)		6	k Ω
		5	pF
Luminance Channel Input Voltage	Luma Input Signal = 30% Sync.	0.5	V_{P-P}
Bandwidth of Luminance Channel	Luma Input Signal: $0.5V_{P-P}$ (30% Sync) modulated CW Adj. modulation frequency for -3dB at color outputs.	8	MHz
Brightness Control Range (Terminal 23)	For Control Characteristics, See Figures 1 and 2.	0 - 3.5	V_{DC}
Output Black Level Range Offset	Luma Input Signal: $0.5V_{P-P}$ (30% Sync) V_B 0V - 5V, Measured at Pin 18 black level. See Figures 1 and 2.	5.9-9.7	V_{DC}
		0.6 Max.	V_{DC}
Contrast Control Range (Terminal 22)	Luminance Input: $0.5V_{P-P}$ (30% Sync), for Control Characteristics. See Figure 3	0 - 5	V_{DC}
Luminance Gain Control Range	Luminance Input: $0.5V_{P-P}$ (30% Sync), $V_C = 0.5\text{V}$ - 5V measure Pin 18 black level to maximum white level. See Figure 4.	32	dB
RGB Output Swing	Luminance Input: $0.5V_{P-P}$ (30% Sync), $V_C = 5\text{V}$, read black level to peak white. See Figures 5 and 6.	4	V_{P-P}
CHROMINANCE SECTION			
Input Impedance (Terminal 4)	See Figures 7 and 8.	4.5	k Ω
		5	pF
Chroma Channel Input Voltage	Chroma	220	mV $_{P-P}$
	Burst	100	mV $_{P-P}$
ACC Range		+6 - (-20)	dB
Input Burst Level for Kill (Note 1)	Adjust chroma input Pin 4 until Pin 2 $\leq 25\text{mV}_{P-P}$. Measure Burst level at Pin 4.	10	mV $_{P-P}$
Contrast Control Chroma/Luma Tracking	Chroma Input: Burst = 100mV_{P-P} , Chroma = 220mV_{P-P} . Luminance Input: $0.35V_{P-P}$, V_S adjusted for Chroma at Pin 18 = $2V_{P-P}$. V_C is adjusted for luminance at Pin 18 = $2V_{P-P}$. V_C is again adjusted for luminance of +6 and -9dB. Then read chroma percentage difference. See Figure 9.	± 5	%

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PARAMETER	TEST CONDITIONS	TYPICAL VALUE	UNITS
Saturation Control Range (Terminal 3)	For control characteristic, see Figure 10.	0 - 5	V_{DC}
Maximum Chroma Output Voltage (Terminal 2)	Chroma Input: Burst = 100mV_{P-P} , Chroma = 220mV_{P-P} . Adjust V_C and V_S for maximum Pin 2 output.	2.5	V_{P-P}
OSCILLATOR SECTION			
Pull-In Range	Chroma Input: Burst = 100mV_{P-P} , Chroma = 220mV_{P-P} . Adjust C_X for HI/LO f_{OSC} without Chroma signal. Apply signal to lock.	± 500	Hz
Static Phase Error		2	Deg./100Hz
DEMODULATOR SECTION			
R-Y Demodulator Conversion Gain	Chroma Input: Burst = 100mV , Chroma = 220mV_{P-P} , $V_{\emptyset}$. Adjust V_C for $V_{18} = 1\text{V}$. Read V_{15} . Calculate V_{18}/V_{15} .	10	Ratio
B-Y Demodulator Conversion Gain	Chroma Input: Burst = 100mV_{P-P} , $V_{\emptyset}$. Read V_{16} and V_{14} . Calculate V_{16}/V_{14} . V_C remains as for R-Y gain.	18	Ratio
G-Y/B-Y Matrix Ratio	Chroma Input: Burst = 100mV_{P-P} , Chroma = 220mV_{P-P} , $V_{\emptyset}$ read V_{17} and V_{16} , Calculate V_{17}/V_{16} . V_C remains as above.	0.2	Ratio
G-Y/R-Y Matrix Ratio	Chroma Input: Burst = 100mV_{P-P} , Chroma = 220mV_{P-P} , $V_{\emptyset}$. Read V_{17} and V_{18} . Calculate V_{17}/V_{18} . V_C remains as above.	0.5	Ratio
Sub-Carrier and Harmonic Content at Outputs	No Chroma or Luma Input. Read residual carrier at outputs.	30	mV_{P-P}
SANDCASTLE PULSE			
Horizontal and Vertical Blanking Pedestal		2 - 5	V
Burst Gate Pulse		$6.5 - V_{CC}$	V

NOTES:

1. If a different value is desired, see the Threshold Adjustment Circuit of Figure 17.
2. Use of the circuit of Figure 18 is suggested to prevent increased color saturation at low level RF signals.
3. The reference voltage can be adjusted by changing the values of the voltage divider.

Circuit Description (See Block Diagram and Figure 20)

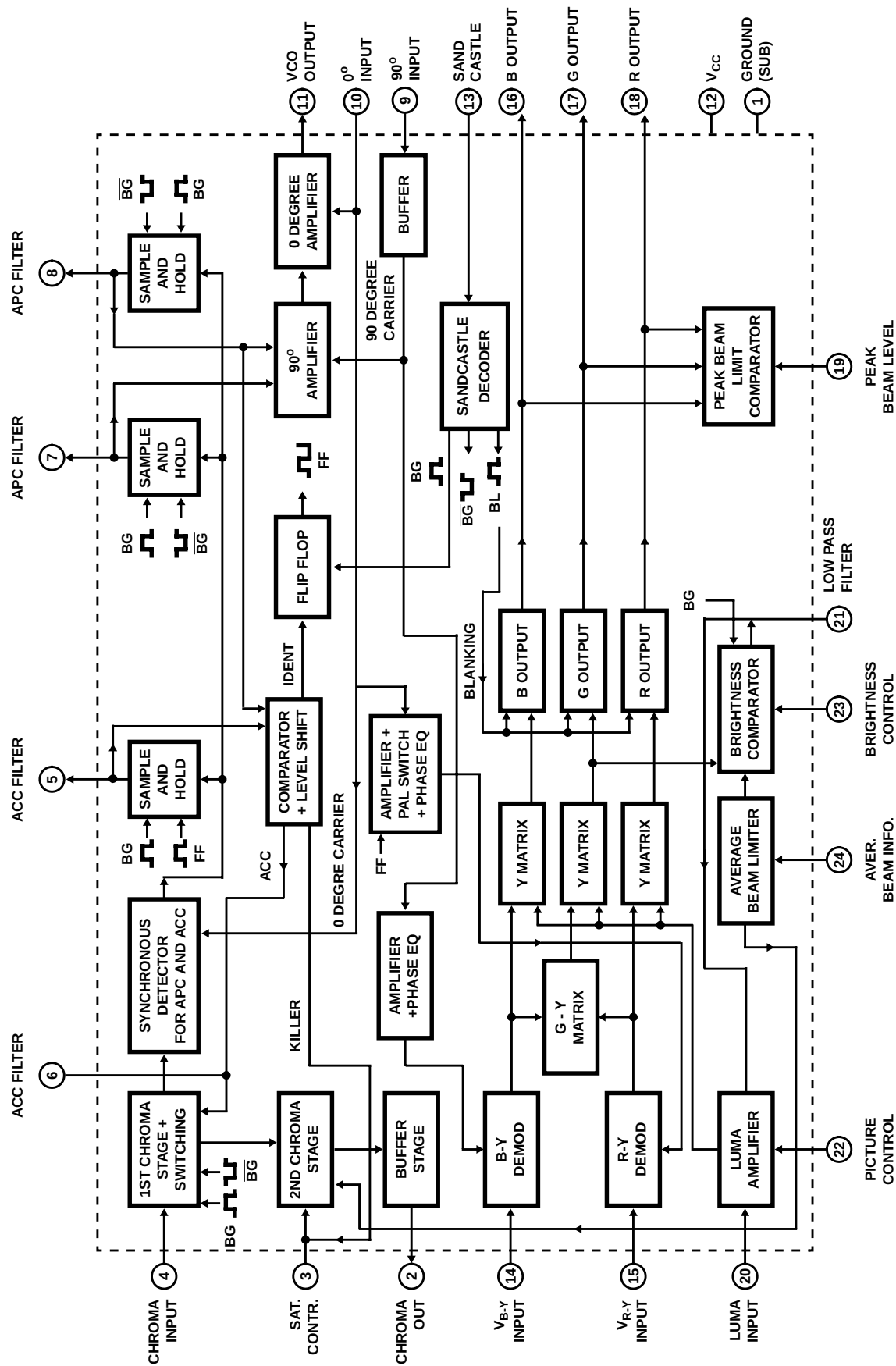
The chroma signal is externally separated from the video signal by means of a bandpass or high-pass filter and applied to pin 4. The burst is separated in the first chroma stage and applied to the synchronous detector which provides information to sample-and-hold circuits for APC (phase-locked loop), ACC (automatic chroma gain control) and identification and killing. The 4.43MHz crystal oscillator is phase-locked to the burst and provides 0 degrees and 90 degrees (via an external phase shifter) carriers to the chroma demodulators. The burst and chroma amplitude at the output of the first chroma amplifier is kept constant by the automatic gain control.

The second chroma stage provides saturation control (pin 3) which tracks the contrast control in the luminance channel. This stage is also used for color killing.

A buffer stage drives the external PAL delay line. The separated U and V signals are applied to pins 14 and 15, respectively, and demodulated. A standard G-Y matrix is included on the chip.

The luminance signal passes through the subcarrier trap and through the luminance delay line and enters the chip at pin 20. Contrast and brightness control is provided before the luminance signal is combined with the color difference signals in the Y matrix. Average and peak beam limiting circuits are controlled from pins 24 and 19.

Block Diagram



Typical Performance Curves

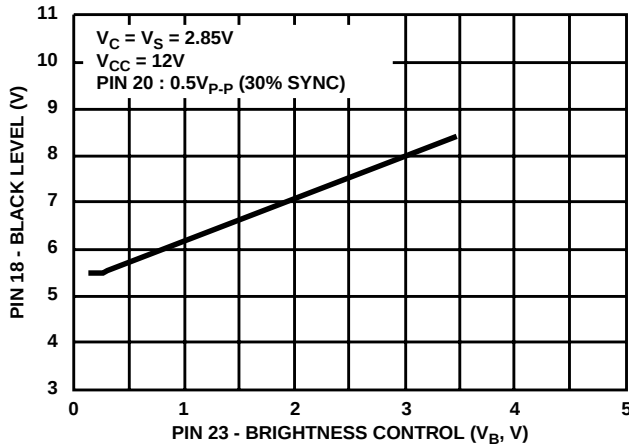


FIGURE 1. BRIGHTNESS CONTROL (V_B) MEASURED AT PIN 18 OUTPUT TERMINAL

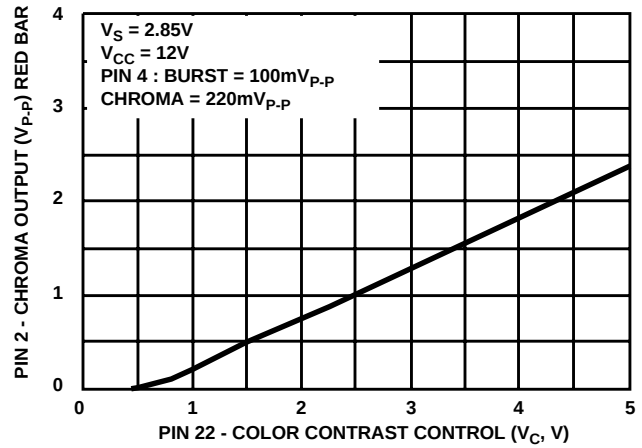


FIGURE 2. CONTRAST CONTROL (V_C) MEASURED AT 2ND CHROMA AMPLIFIER OUTPUT TERMINAL

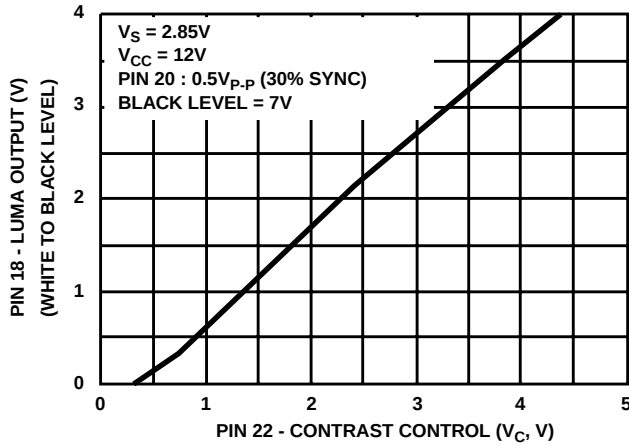


FIGURE 3. CONTRAST CONTROL (V_C) MEASURED AT PIN 18 OUTPUT TERMINAL

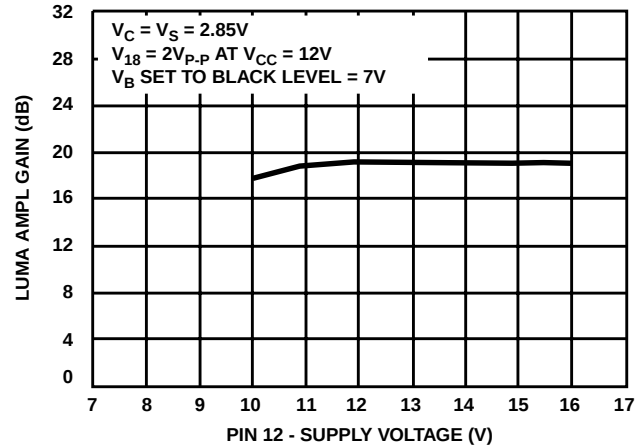


FIGURE 4. LUMA GAIN vs SUPPLY VOLTAGE (V_{CC}) MEASURED AT LUMA AMPLIFIER OUTPUT TERMINAL

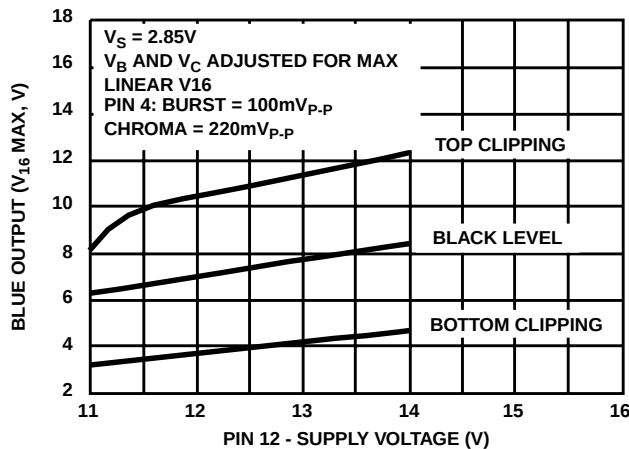


FIGURE 5. LINEAR OPERATING RANGE AS A FUNCTION OF V_{CC} MEASURED AT PIN 16 OUTPUT TERMINAL (BEST OPERATING RANGE IS 11-13V V_{CC})

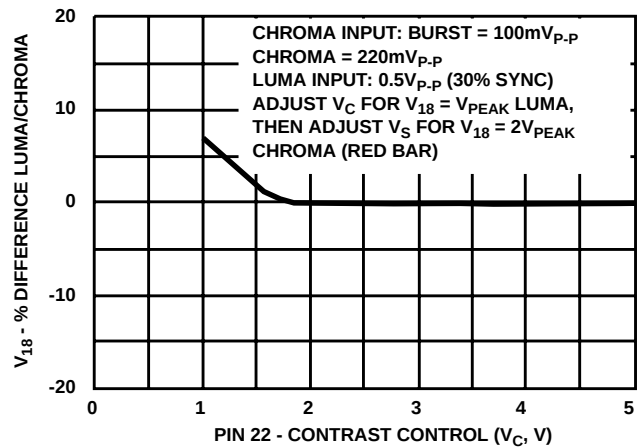


FIGURE 6. LUMA/CHROMA TRACKING AS A FUNCTION OF V_C MEASURED AT PIN 18 OUTPUT TERMINAL

Typical Performance Curves (Continued)

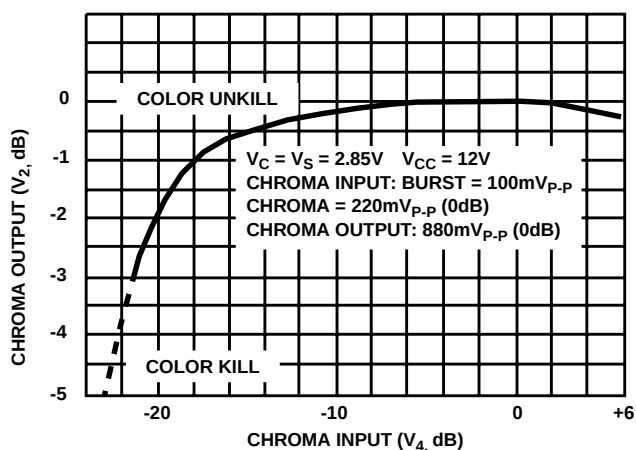


FIGURE 7. ACC CHARACTERISTICS MEASURED AT PIN 2 OUTPUT TERMINAL

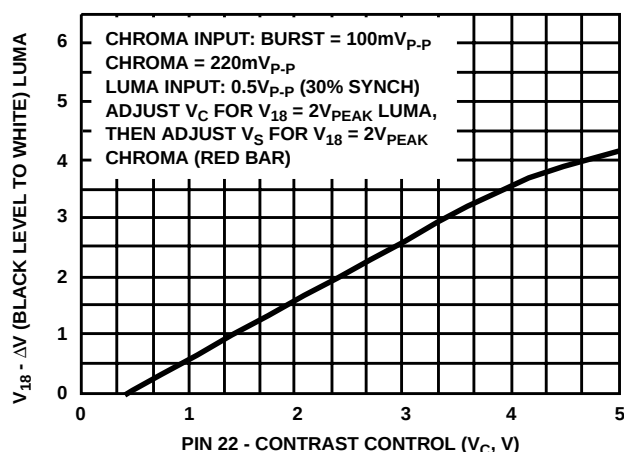


FIGURE 8. LUMA/CHROMA TRACKING vs CONTRAST CONTROL MEASURED AT PIN 18 OUTPUT TERMINAL

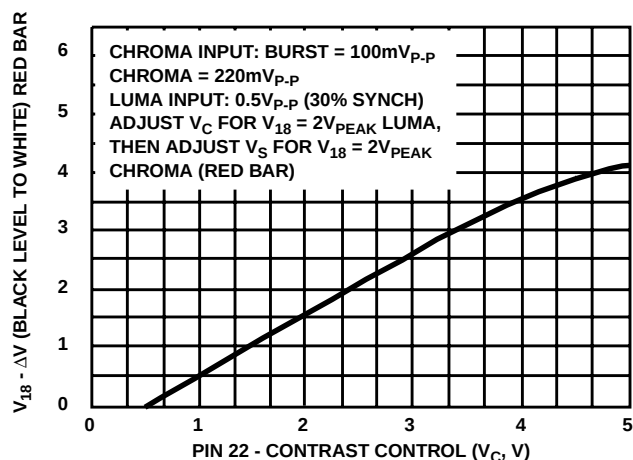


FIGURE 9. LUMA/CHROMA TRACKING WITH CONTRAST CONTROL MEASURED AT PIN 18 OUTPUT TERMINAL

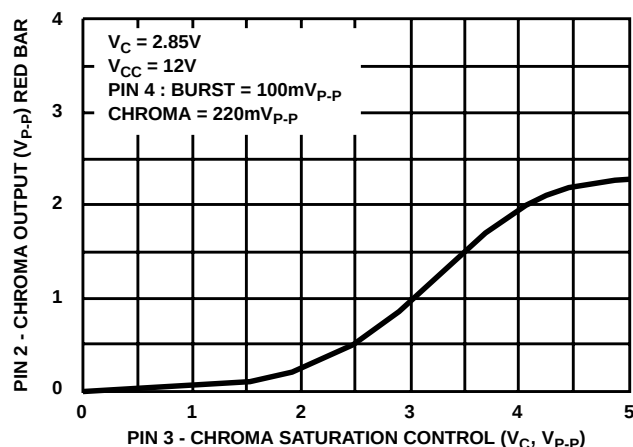
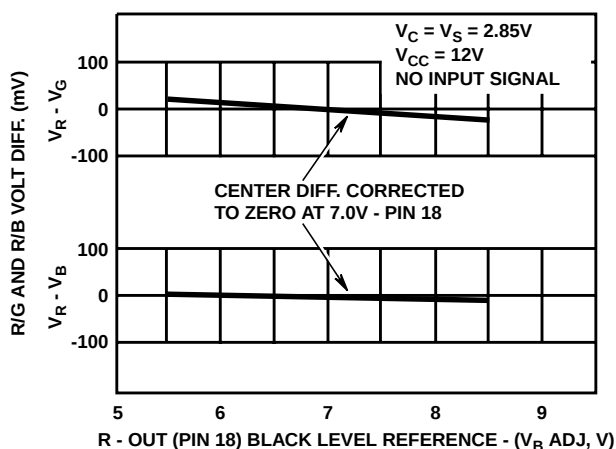
FIGURE 10. SATURATION CONTROL (V_S) MEASURED AT CHROMA AMPLIFIER OUTPUT TERMINAL PIN 2

FIGURE 11. DIFFERENTIAL BLACK-LEVEL TRACKING MEASURED AT RGB OUTPUT TERMINALS

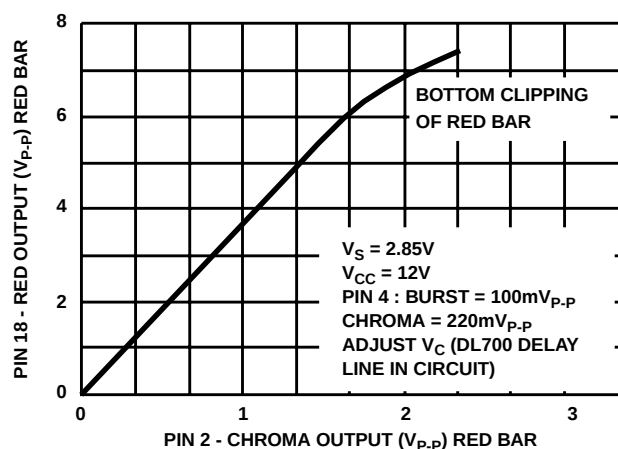


FIGURE 12. PIN 18 OUTPUT vs PIN 2 VOLTAGE MEASURED AT CHROMA OUTPUT TERMINALS AND R OUTPUT

Typical Performance Curves (Continued)

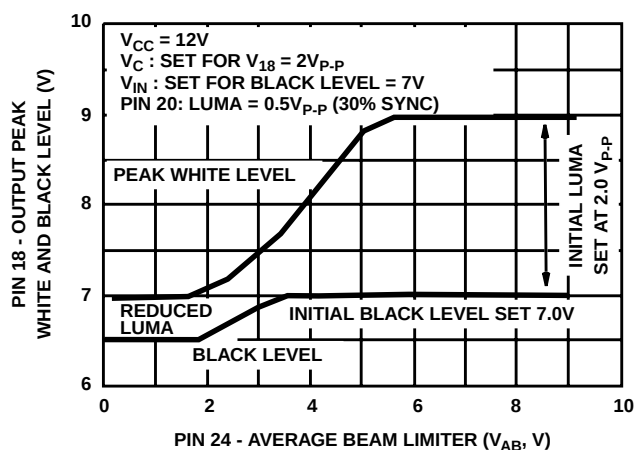
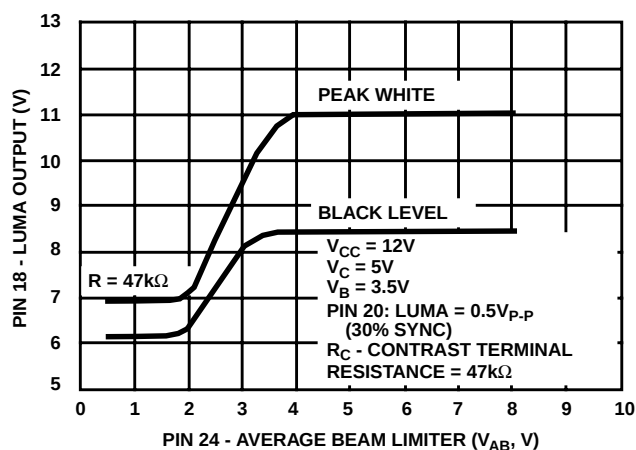
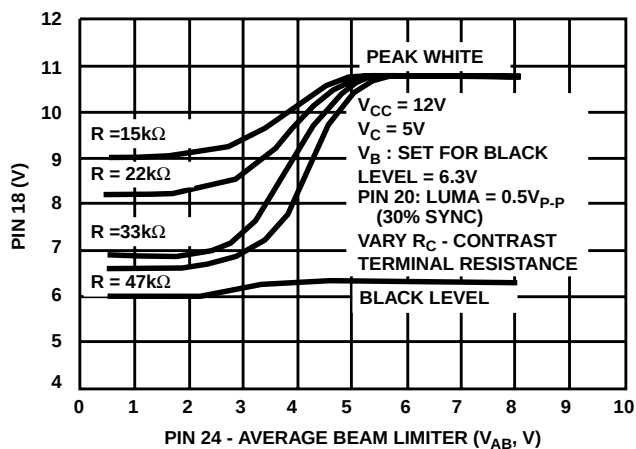
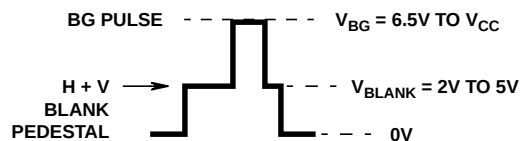
FIGURE 13. AVERAGE BEAM LIMITER (V_{AB}) MEASURED AT PIN 18 OUTPUTFIGURE 14. AVERAGE BEAM LIMITER (V_{AB}) MEASURED AT PIN 18 OUTPUTFIGURE 15. AVERAGE BEAM LIMITER (V_{AB}) MEASURED AT PIN 18 OUTPUT

FIGURE 16. SANDCASTLE INPUT WAVEFORM

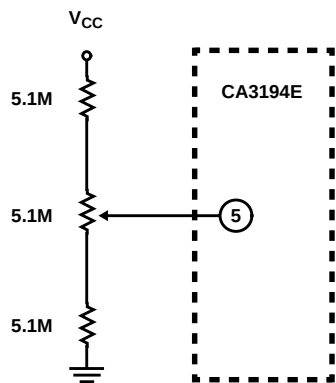
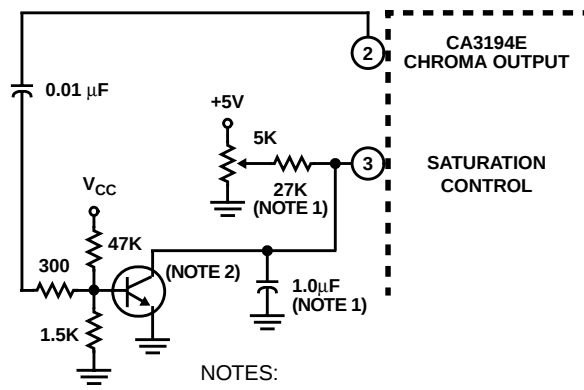


FIGURE 17. KILLER-THRESHOLD LEVEL CONTROL



NOTES:

1. Nominal values used in NTSC system.
2. Small signal n-p-n.

FIGURE 18. EXTERNAL OVERLOAD DETECTOR

Test Circuit

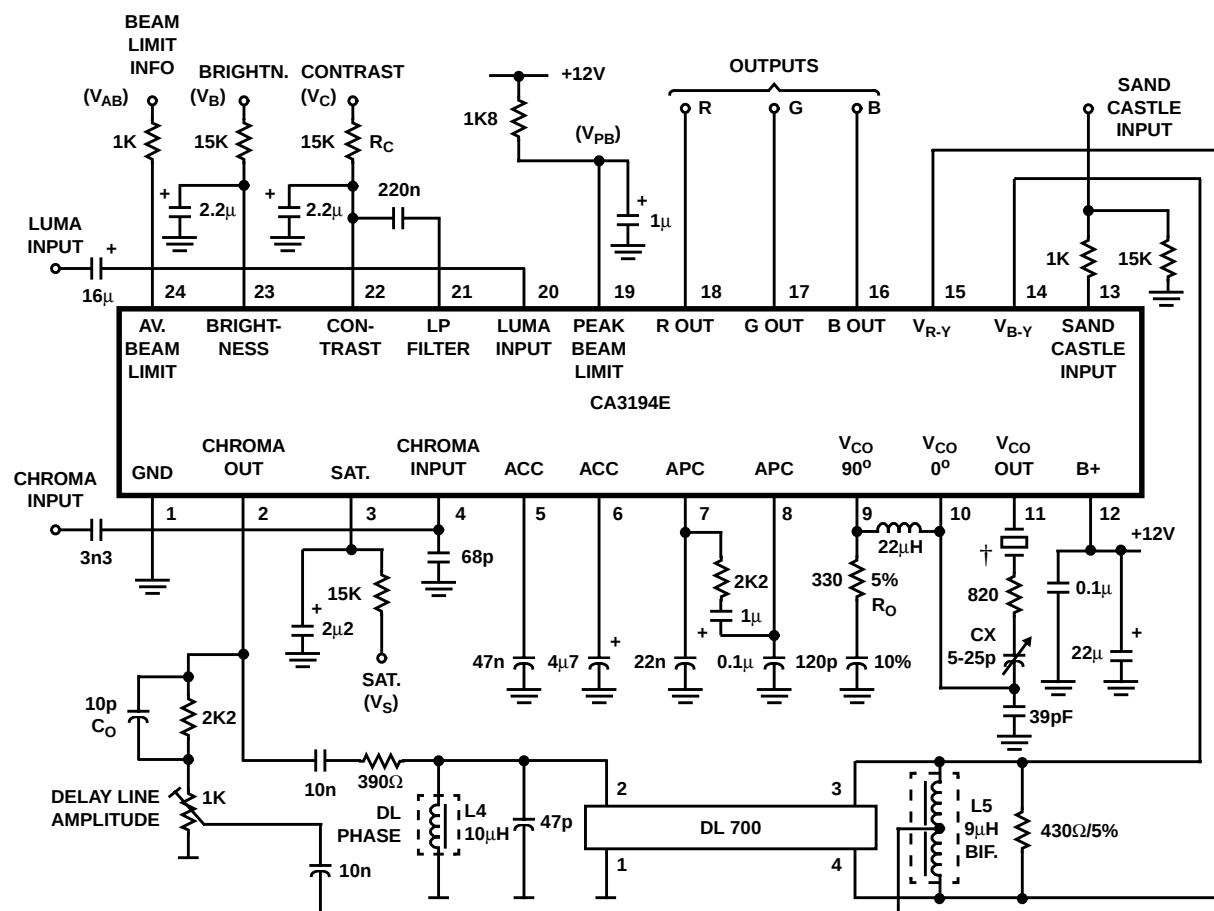


FIGURE 19. TEST CIRCUIT

NOTES:

† 4.43361875MHz

Trim C_O for zero phase; Trim R_O for quad phase.

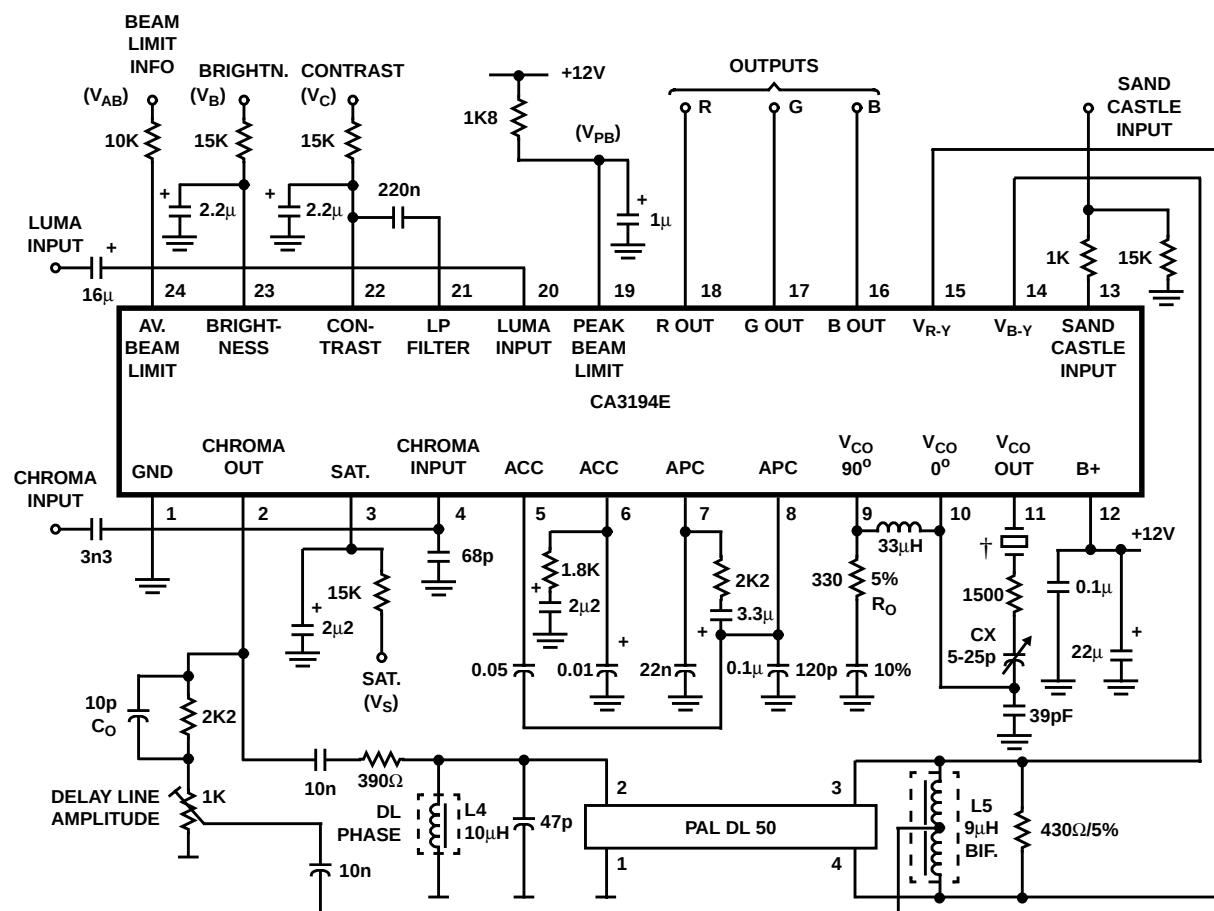
Test Circuit (Continued)

FIGURE 20. APPLICATION CIRCUIT FOR PAL M

NOTE:

† 3.575611MHz