2.5V, 3.3V LVCMOS 1:9 Clock Fanout Buffer
AK8180B

Features

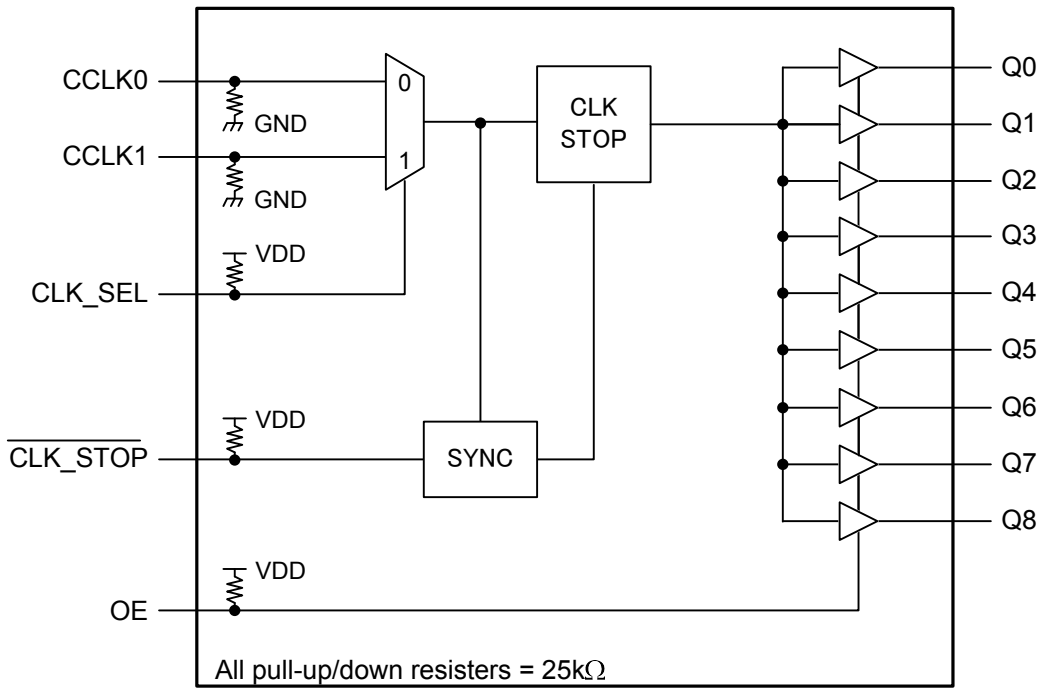
- 9 LVCMOS outputs
- Selectable LVCMOS inputs
- 2.5V or 3.3V power supply
- Clock frequency up to 350MHz
- Output-to-output skew : 150ps max
- Synchronous output stop in logic state
- High-impedance output control
- Drive up to 18 series terminated clock lines
- Operating Temperature Range: -40 to +85°C
- Package: 32-pin LQFP (Pb free)
- Pin compatible with MPC9447

Description

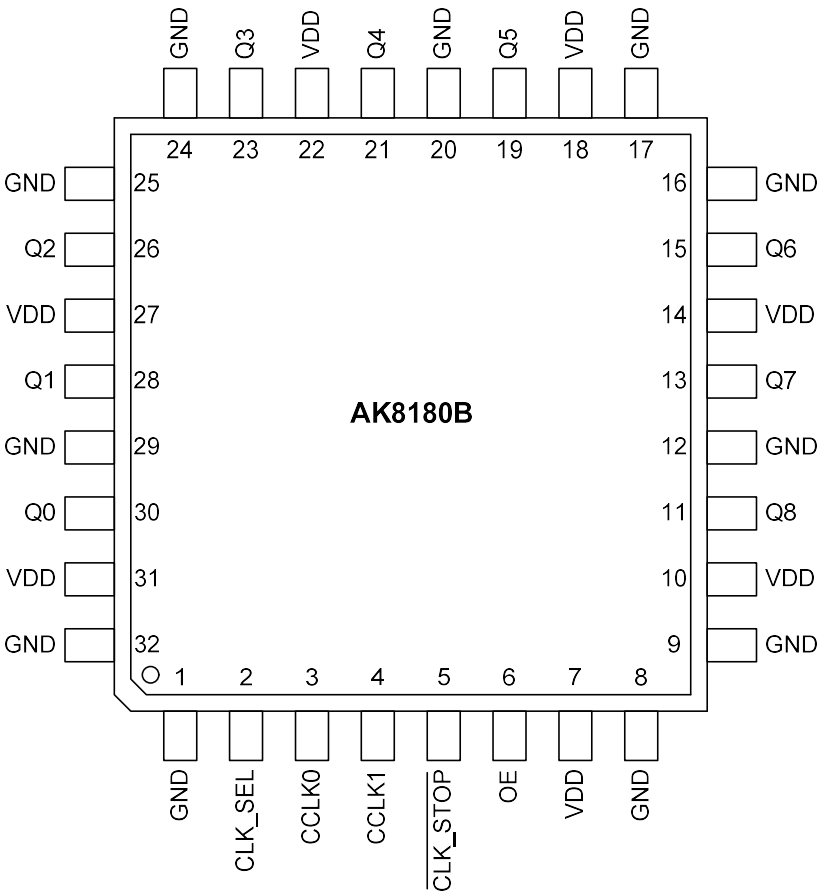
The AK8180B is a member of AKM's LVCMOS clock fanout buffer family designed for telecom, networking and computer applications, requiring a range of clocks with high performance and low skew. The AK8180B distributes 9 buffered clocks up to 350MHz. The 9 outputs can drive terminated 50 Ω clock lines. The $\overline{\text{CLK\_STOP}}$ control allows the output signal to start and stop only in a logic low state. The OE control sets the outputs to high-impedance mode.

AK8180B are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low skew. The AK8180B is available in a 7mm x 7mm 32-pin LQFP package.

Block Diagram



Pin Descriptions



Package: 32-Pin LQFP(Top View)

Pin No.	Pin Name	Pin Type	Pullup /down	Description
1	GND	--	--	Ground
2	CLK_SEL	IN	PU	Clock Input Select
3	CCLK0	IN	PD	Clock Input (LVCMOS)
4	CCLK1	IN	PD	Clock Input (LVCMOS)
5	$\overline{\text{CLK\_STOP}}$	IN	PU	Clock Output Disable (Active low)
6	OE	IN	PU	Clock Output Enable (Disable=High impedance)
7	VDD	--	--	Power supply
8,	GND	--	--	Ground
9	GND	--	--	Ground
10	VDD	--	--	Power supply
11	Q8	OUT	--	Clock output
12	GND	--	--	Ground

PU: Pull up PD: Pull down

(continued on next page)

Pin No.	Pin Name	Pin Type	Pullup /down	Description
13	Q7	OUT	--	Clock output
14	VDD	--	--	Power supply
15	Q6	OUT	--	Clock output
16	GND	--	--	Ground
17	GND	--	--	Ground
18	VDD	--	--	Power supply
19	Q5	OUT	--	Clock output
20	GND	--	--	Ground
21	Q4	OUT	--	Clock output
22	VDD	--	--	Power supply
23	Q3	OUT	--	Clock output
24	GND	--	--	Ground
25	GND	--	--	Ground
26	Q2	OUT	--	Clock output
27	VDD	--	--	Power supply
28	Q1	OUT	--	Clock output
29	GND	--	--	Ground
30	Q0	OUT	--	Clock output
31	VDD	--	--	Power supply
32	GND	--	--	Ground

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8180B	AK8180B	Tape and Reel	32-pin LQFP	-40 to 85 ℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	GND-0.3 to VDD+0.3	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-40		85	°C
Supply voltage (1)	VDD	VDD±5%	2.375	2.5	2.625	V
			3.135	3.3	3.465	

(1) Power of 2.5V or 3.3V requires to be supplied from a single source. A decoupling capacitor of 0.01μF for power supply line should be located close to each VDD pin.

General Specification

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Termination Voltage	VTT			VDD/2		V
ESD Protection 1	MM	Machine model	200			V
ESD Protection 2	HBM	Human Body Model	2000			V
Latch-Up Immunity	LU		200			mA
Power Dissipation Capacitance		Per output		10		pF
Input Capacitance				4.0		pF

Power Supply Current <3.3V>

VDD= 3.3V±5%, Ta: -40 to +85℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Full operation (1)	IDD1	CCLK0=350MHz CLK_SEL=L		120	140	mA
Quiescent state (1)(2)	IDD2			1.0	2.0	mA

(1) The outputs have no loads. (2) All inputs are in default state by the internal pull up/down resisters.

DC Characteristics <3.3V>

All specifications at VDD= 3.3V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	LVCMOS	2.0		VDD+0.3	V
Low Level Input Voltage	V_{IL}	LVCMOS	-0.3		0.8	V
Input Current (1)	I_L1	Vin=GND or VDD	-300		+300	μA
High Level Output Voltage	V_{OH}	I_{OH}= -24mA (2)	2.4			V
Low Level Output Voltage	V_{OL}	I_{OL}= +24mA I_{OL}= +12mA			0.55 0.30	V
Output Impedance				17		Ω

(1) Input pull-up / pull down resistors influence input current.

(2) The AK8180B is capable of driving 50 Ω transmission lines of the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of VTT. Alternatively, the device drives up to two 50 Ω series terminated transmission lines(for VDD=3.3V) or one 50 Ω series terminated transmission line(for VDD=2.5V).

AC Characteristics <3.3V> (1)

All specifications at VDD= 3.3V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Frequency	f_{IN}	Pin: CCLK	0		350	MHz
Input Pulse Width	t_{pwIN}	Pin: CCLK	1.4			ns
Input Rise/Fall time (3)	t_{rIN},t_{fOUT}	Pin: CCLK 0.8 to 2.0V			1.0	ns
Output Frequency	f_{OUT}	Pin: Q0-8	0		350	MHz
Propagation Delay	t_{PLH}, t_{PHL}	CCLK to any Q	0.8	1.6	2.8	ns
Output Disable Time	t_{PLZ},t_{PHZ}				11	ns
Output Enable Time	t_{PZL},t_{PZH}				11	ns
Setup Time	t_S	CCLK to $\overline{\text{CLK\_STOP}}$	0.0			ns
Hold Time	t_H	CCLK to $\overline{\text{CLK\_STOP}}$	1.0			ns
Output-to-Output Skew	t_{skPP}				150	ps
Device-to-Device Skew	t_{skD}				2.0	ns
Output Pulse Skew (4)	t_{skO}	CCLK			300	ps
Output Duty Cycle	DC_{OUT}	f_{OUT} < 170MHz DC_{REF} =50%	45	50	55	%
Output Rise/Fall Time	t_r, t_f	0.55 to 2.4V	0.1		1.0	ns
Cycle-to-Cycle Jitter	t_{JITCC}	1 σ		6		ps

(1) AC characteristics apply for parallel output termination of 50 Ω to VTT.

(2) Vcmr(AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the Vcmr range and the input swing lies within the Vpp(AC) specification. Violation of Vcmr or Vpp impacts $t_{PLH/PHL}$ and t_{skD}.

(3) Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, input pulse width, output duty cycle and maximum frequency specifications.

(4) Output pulse skew t_{skO} is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

Power Supply Current <2.5V>

VDD= 2.5V±5%, Ta: -40 to +85℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Full operation (1)	IDD1	CCLK0=350MHz CLK_SEL=L		95	115	mA
Quiescent state (1)(2)	IDD2			0.7	1.3	mA

(1) The outputs have no loads. (2) All inputs are in default state by the internal pull up/down resisters.

DC Characteristics <2.5V>

All specifications at VDD= 2.5V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	LVCMOS	1.7		VDD+0.3	V
Low Level Input Voltage	V_{IL}	LVCMOS	-0.3		0.7	V
Input Current (1)	I_L1	Vin=GND or VDD	-300		+300	μA
High Level Output Voltage	V_{OH}	I_{OH}= -15mA (2)	1.8			V
Low Level Output Voltage	V_{OL}	I_{OL}= +15mA			0.6	V
Output Impedance				19		Ω

(1) Input pull-up / pull down resistors influence input current.

(2) The AK8180B is capable of driving 50 Ω transmission lines of the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of VTT. Alternatively, the device drives up to two 50 Ω series terminated transmission lines(for VDD=3.3V) or one 50 Ω series terminated transmission lines(for VDD=2.5V).

AC Characteristics <2.5V> (1)

All specifications at VDD= 2.5V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Frequency	f_{IN}	Pin: CCLK	0		350	MHz
Input Pulse Width	t_{pwIN}	Pin: CCLK	1.4			ns
Input Rise/Fall time (3)	t_{rIN},t_{fOUT}	Pin: CCLK 0.8 to 2.0V			1.0	ns
Output Frequency	f_{OUT}	Pin: Q0-8	0		350	MHz
Propagation Delay	t_{PLH}, t_{PHL}	CCLK to any Q	0.9	1.8	3.6	ns
Output Disable Time	t_{PLZ},t_{PHZ}				11	ns
Output Enable Time	t_{PZL},t_{PZH}				11	ns
Setup Time	t_S	CCLK to $\overline{\text{CLK\_STOP}}$	0.0			ns
Hold Time	t_H	CCLK to $\overline{\text{CLK\_STOP}}$	1.0			ns
Output-to-Output Skew	t_{skPP}				150	ps
Device-to-Device Skew	t_{skD}				2.7	ns
Output Pulse Skew (4)	t_{skO}	CCLK			200	ps
Output Duty Cycle	DC_{OUT}	DC_{REF} =50%	45	50	55	%
Output Rise/Fall Time	t_r, t_f	0.6 to 1.8V	0.1		1.0	ns
Cycle-to-Cycle Jitter	t_{JITCC}	1 σ		10		ps

(1) AC characteristics apply for parallel output termination of 50 Ω to VTT.

(2) Vcmr(AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the Vcmr range and the input swing lies within the Vpp(AC) specification. Violation of Vcmr or Vpp impacts $t_{PLH/PHL}$ and t_{skD}.

(3) Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, input pulse width, output duty cycle and maximum frequency specifications.

(4) Output pulse skew t_{skO} is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

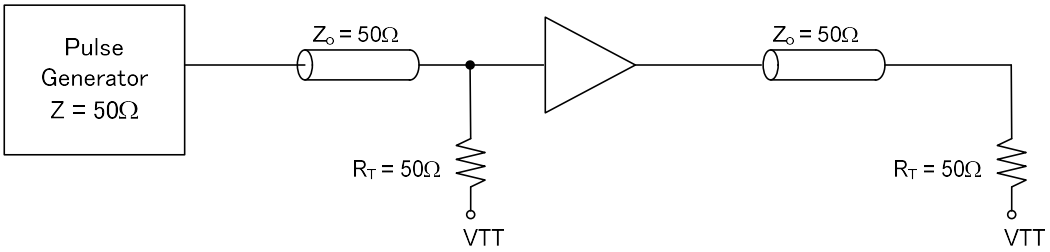


Figure 1 CCLK AC Test Reference

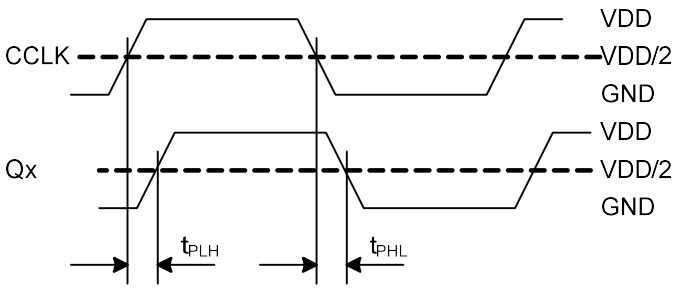


Figure 2 Propagation Delay Test Reference

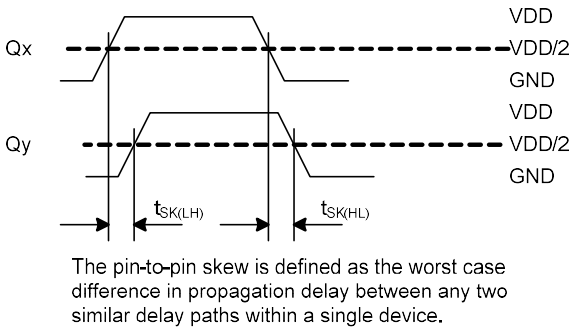


Figure 3 Output-to-Output Skew

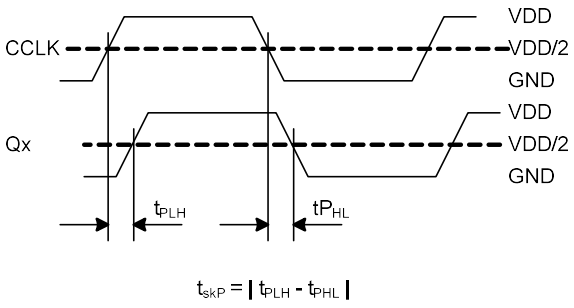
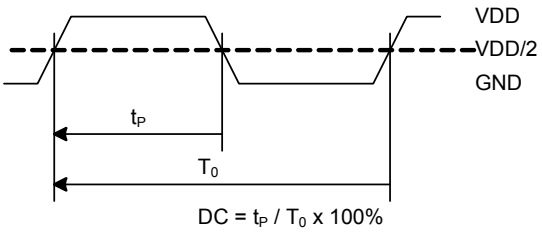
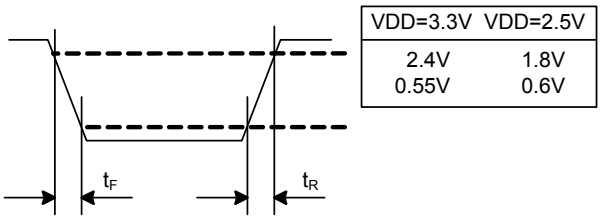


Figure 4 Output Pulse Skew Test Reference



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Figure 5 Output Duty Cycle



VDD=3.3V	VDD=2.5V
2.4V	1.8V
0.55V	0.6V

Figure 6 Output Translation Test Reference

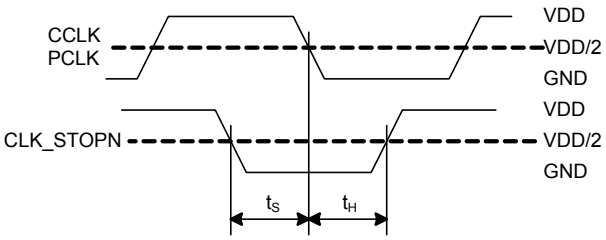
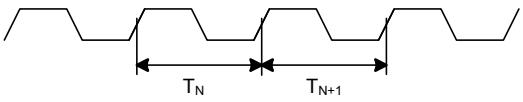


Figure 7 Setup and Hold Time Test Reference



$T_{JIT(CC)} = | T_N - T_{N+1} |$

The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs.

Figure 8 Cycle-to-Cycle Jitter

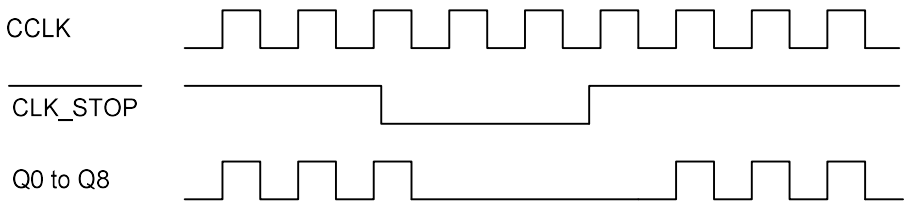
Function Table

The following table shows the inputs/outputs clock state configured through the control pins.

Table 1: Control-Pin-Setting Function Table

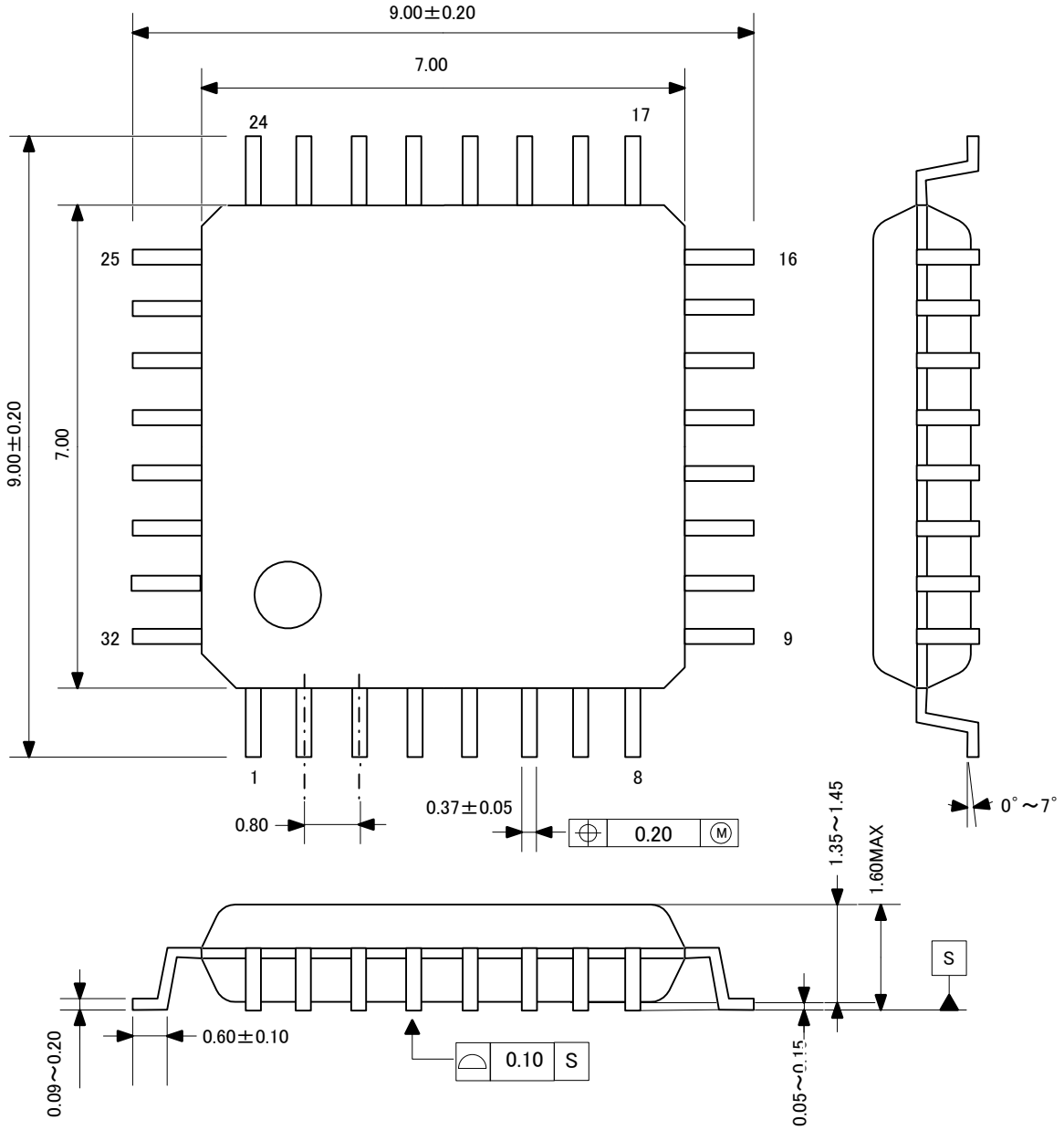
Control Pin	Default	0	1
CLK_SEL	1	CCLK0 input selected	CCLK1 input selected
OE	1	Outputs disabled. (high impedance)	Outputs enabled
$\overline{\text{CLK\_STOP}}$	1	Outputs synchronously stopped in logic low state.	Outputs active

Application example of $\overline{\text{CLK\_STOP}}$



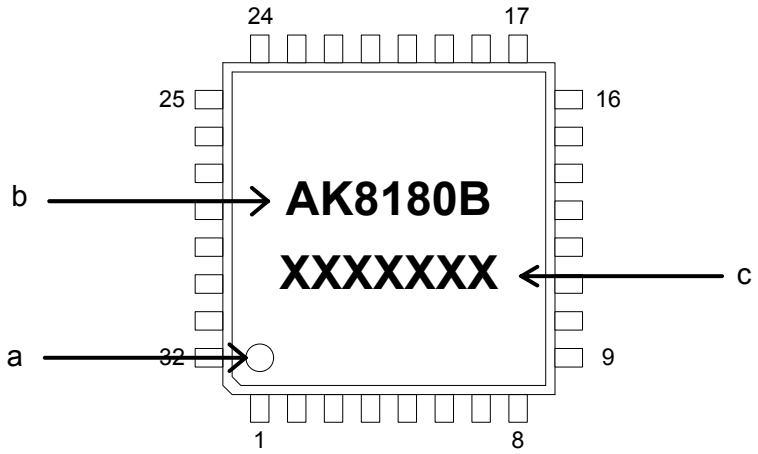
Package Information

- **Mechanical data : 32-lead LQFP**



- **Marking**

a: #1 Pin Index
b: Part number
c: Date code (7 digits)



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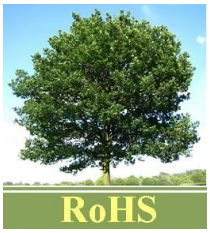
- **RoHS Compliance**



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(*) RoHS compliant products from AKM are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.

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  Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
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