Data Sheet

CADEKA
Amplify the Human Experience

CDK1302

8-bit, 750 MSPS, Flash A/D Converter

FEATURES

- 1:2 Demuxed ECL compatible outputs
- Wide input bandwidth – 900MHz
- Low input capacitance – 15pF
- Metastable errors reduced to 1 LSB
- Monolithic for low cost
- Gray code output

APPLICATIONS

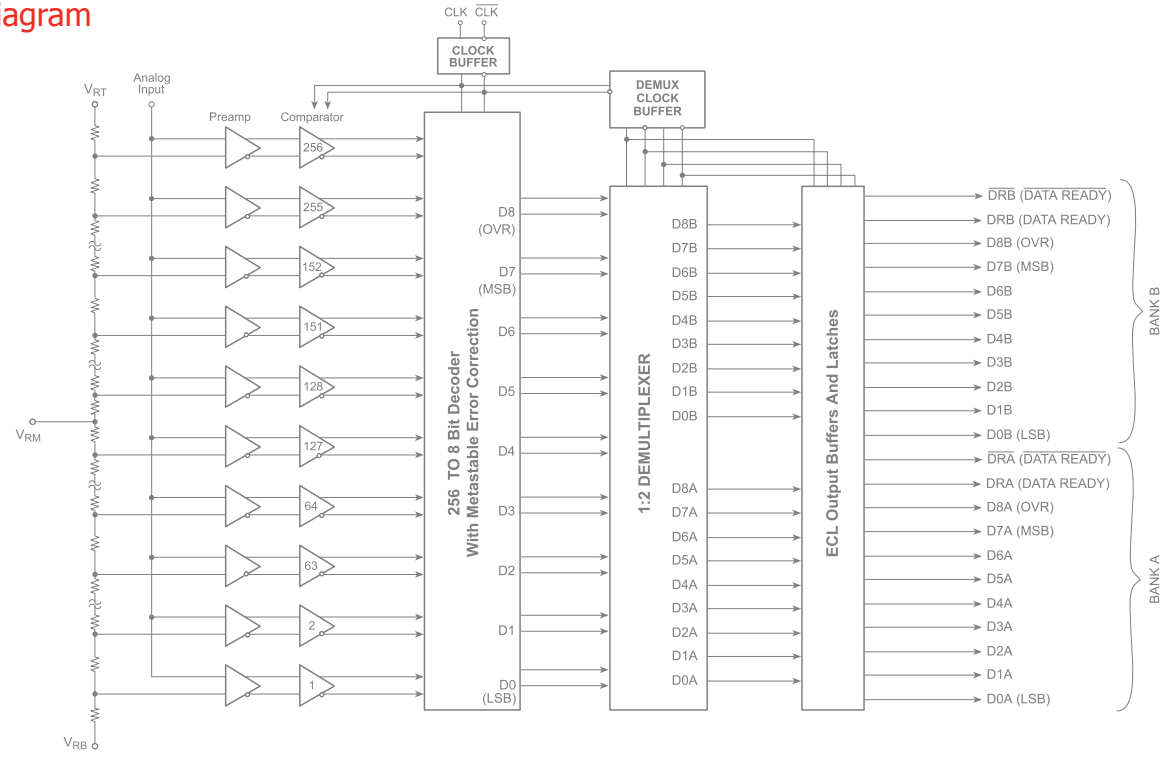
- Digital oscilloscopes
- Transient capture
- Radar, EW, ECM
- Direct RF down-conversion

General Description

The CDK1302 is a full parallel (flash) analog-to-digital converter capable of digitizing full scale (0 to -2V) inputs into eight-bit digital words at an update rate of 750 MSPS. The ECL-compatible outputs are demultiplexed into two separate output banks, each with differential data ready outputs to ease the task of data capture. The CDK1302's wide input bandwidth and low capacitance eliminate the need for external track-and-hold amplifiers for most applications. A proprietary decoding scheme reduces metastable errors to the 1 LSB level. The CDK1302 operates from a single – 5.2V supply, with a nominal power dissipation of 5.5W.

The CDK1302 is available in an 80-lead surface-mount MQuad package over the industrial temperature range (-25°C to +85°C).

Block Diagram



Ordering Information

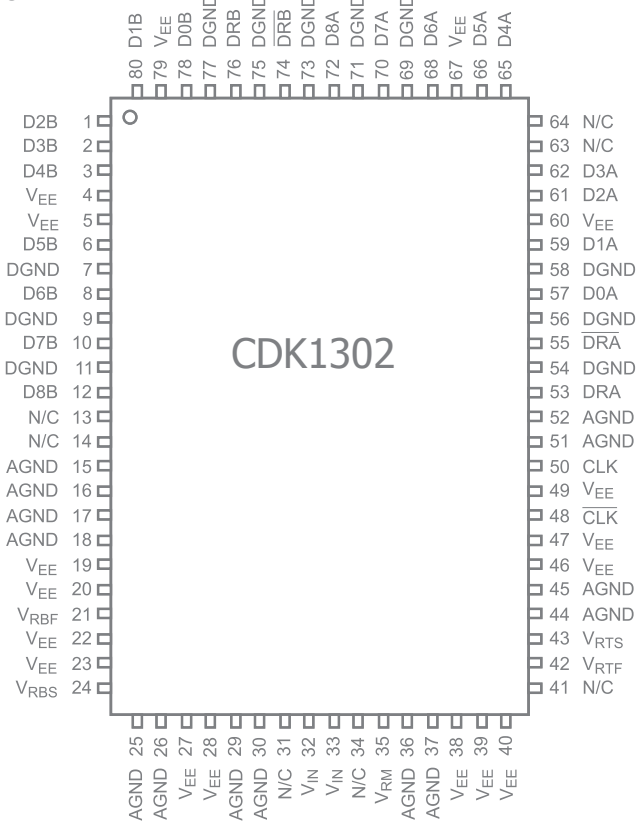
Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CDK1302AEMQ80	MQUAD-80	Yes	Yes	-25°C to +85°C	Rail
CDK1302AEMQ80_Q	MQUAD-80	No	No	-25°C to +85°C	Rail
CDK1302BEMQ80	MQUAD-80	Yes	Yes	-25°C to +85°C	Rail
CDK1302BEMQ80_Q	MQUAD-80	No	No	-25°C to +85°C	Rail

Moisture sensitivity level for all parts is MSL-1.

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Pin Configuration

MQUAD-80



Pin Assignments

Pin Name	Description
V_{EE}	Negative Supply Nominally -5.2V
AGND	Analog Ground
V_{RTF}	Reference Voltage Force Top, Nominally 0V
V_{RTS}	Reference Voltage Sense Top
V_{RM}	Reference Voltage Middle, Nominally -1V
V_{RBF}	Reference Voltage Force Bottom, Nominally -2V
V_{RBS}	Reference Voltage Sense Bottom
V_{IN}	Analog Input Voltage, Can Be Either Voltage or Sense
DGND	Digital Ground
D0-D7A	Data Output Bank A
D0-D7B	Data Output Bank B
DRA	Data Ready Bank A
$\overline{DRA}$	Not Data Ready Bank A
DRB	Data Ready Bank B
$\overline{DRB}$	Not Data Ready Bank B
D8A	Overrange Output Bank A
D8B	Overrange Output Bank B
CLK	Clock Input
$\overline{CLK}$	Clock Input

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Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltages			
Negative Supply Voltage (V_{EE} to GND)	-7.0	+0.5	V
Ground Voltage Differential	-0.5	+0.5	V
Input Voltages			
Analog Input	+0.5	V_{EE} +0.5	V
Reference Input	+0.5	V_{EE} +0.5	V
Digital Input	+0.5	V_{EE} +0.5	V
Reference Current Input (V_{RT} to V_{RB})		35	mA
Output Voltages			
Digital Output Current	0	-28	mA

Reliability Information

Parameter	Min	Typ	Max	Unit
Storage Temperature Range	-65		+150	°C

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range - ambient	-25		+85	°C
Operating Temperature - case			+125	°C
Operating Temperature - junction			+150	°C
Lead Temperature, (soldering 10 seconds)			+300	°C

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Electrical Characteristics

($T_J = T_C = T_A$ = +25°C , V_{EE} = -5.2V, V_{RB} = -2.0V, V_{RM} = -1.0V, V_{RT} = 0.00V, f_{CLK} = 750MHz, Duty Cycle=50%, unless otherwise specified)

			CDK1302A			CDL1302B			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	Resolution			8			8		bits
DC Performance									
DLE	Differential Linearity Error(1)	f_{clk} = 100MHz	-1.0		+1.0	-1.5		+1.5	LSB
ILE	Integral Linearity Error(1)	f_{clk} = 100MHz	-0.85		+0.95	-0.95		+1.5	LSB
	No Missing Codes		Guaranteed			Guaranteed			
Analog Input									
	Input Voltage Range(1)		V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
	Input Bias Current(1)	V_{IN} = 0V		0.75	2.0		0.75	2.0	mA
	Input Resistance			15			15		kΩ
	Input Capacitance	Over Full Input Range		15			15		pF
	Input Bandwidth								
	Small Signal			900			900		MHz
	Large Signal			500			500		MHz
	Offset Error(2)	V_{RT}	-30		+30	-30		+30	mV
	Offset Error(2)	V_{RB}	-30		+30	-30		+30	mV
	Input Slew Rate			5			5		V/ns
	Clock Synchronous Input Currents			2			2		µA
Reference Input									
	Ladder Resistance(1)		60	80		60	80		Ω
	Reference Bandwidth			30			30		MHz
Timing Characteristics									
	Maximum Sample Rate(1)		750			750			MHz
	Aperture Jitter			2			2		ps
	Acquisition Time			250			250		ps
	CLK to Data Delay(2)		0.9	1.4	1.9	0.9	1.4	1.9	ns
	CLK to Data Ready Delay(2)		1.25	1.75	2.25	1.25	1.75	2.25	ns
Dynamic Performance									
SNR	Signal-to-Noise Ratio	f_{IN} = 50MHz(1)	46			44			dB
		f_{IN} = 250MHz(1)	44			42			dB
THD	Total Harmonic Distortion	f_{IN} = 50MHz(1)	-45			-43			dBc
		f_{IN} = 250MHz(1)	-37			-35			dBc
SFDR	Spurious Free Dynamic Range	f_{IN} = 50MHz(1)	48			44			dB
		f_{IN} = 250MHz(1)	40			36			dB
SINAD	Signal-to-Noise and Distortion	f_{IN} = 50MHz(1)	43			41			dB
		f_{IN} = 250MHz(1)	36			34			dB

Notes:

1. 100% production tested at +25°C.
2. Parameter is guaranteed (but not tested) by design and characterization data.
3. Typical Thermal Impedance: θ_{JC} = +4°C/W.

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Electrical Characteristics

($T_J = T_C = T_A = +25°C$, $V_{EE} = -5.2V$, $V_{RB} = -2.0V$, $V_{RM} = -1.0V$, $V_{RT} = 0.00V$, $f_{CLK} = 750MHz$, Duty Cycle=50%, unless otherwise specified)

			CDK1302A			CDK1302B			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Dynamic Inputs									
	Input High Voltage(1)	CLK, $\overline{CLK}$	-1.1	-0.7		-1.1	-0.7		V
	Input Low Voltage(1)	CLK, $\overline{CLK}$		-1.8	-1.5		-1.8	-1.5	V
t_{PWH}	Clock Pulse Width High(1)		0.67	0.5		0.67	0.5		ns
t_{PWL}	Clock Pulse Width Low(1)		0.67	0.5		0.67	0.5		ns
Digital Outputs									
	Logic 1 Voltage(1)		-1.1	-0.9		-1.1	-0.9		V
	Logic 0 Voltage(1)			-1.8	-1.5		-1.8	-1.5	V
	Rise Time	20% to 80%		450			450		ps
	Fall Time	20% to 80%		450			450		ps
Power Supply Requirements									
V_{EE}	Voltage Range(2)		-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
I_{EE}	Current(1)	$V_{IN} = 0V$		1.05	1.2		1.05	1.2	A
	Power Dissipation(1)			5.5	6.25		5.5	6.25	W

Notes:

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2. Parameter is guaranteed (but not tested) by design and characterization data.
3. Typical Thermal Impedance: $\theta_{JC} = +4°C/W$.

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General Description

The CDK1302 is one of the fastest monolithic 8-bit parallel flash A/D converters available today. The nominal conversion rate is 750 MSPS and the analog bandwidth is in excess of 900MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This not only reduces clock transient kickback to the input and reference ladder due to a low AC beta, but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant over different input voltage and frequency ranges and therefore makes the part easier to drive than previous flash converters. The preamplifiers also add a gain of two to the input signal so that each comparator has a wider overdrive or threshold range to "trip" into or out of the active state. This gain reduces metastable states that can cause errors at the output.

The CDK1302 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. The output drive capability of the device can provide full ECL swings into 50Ω loads.

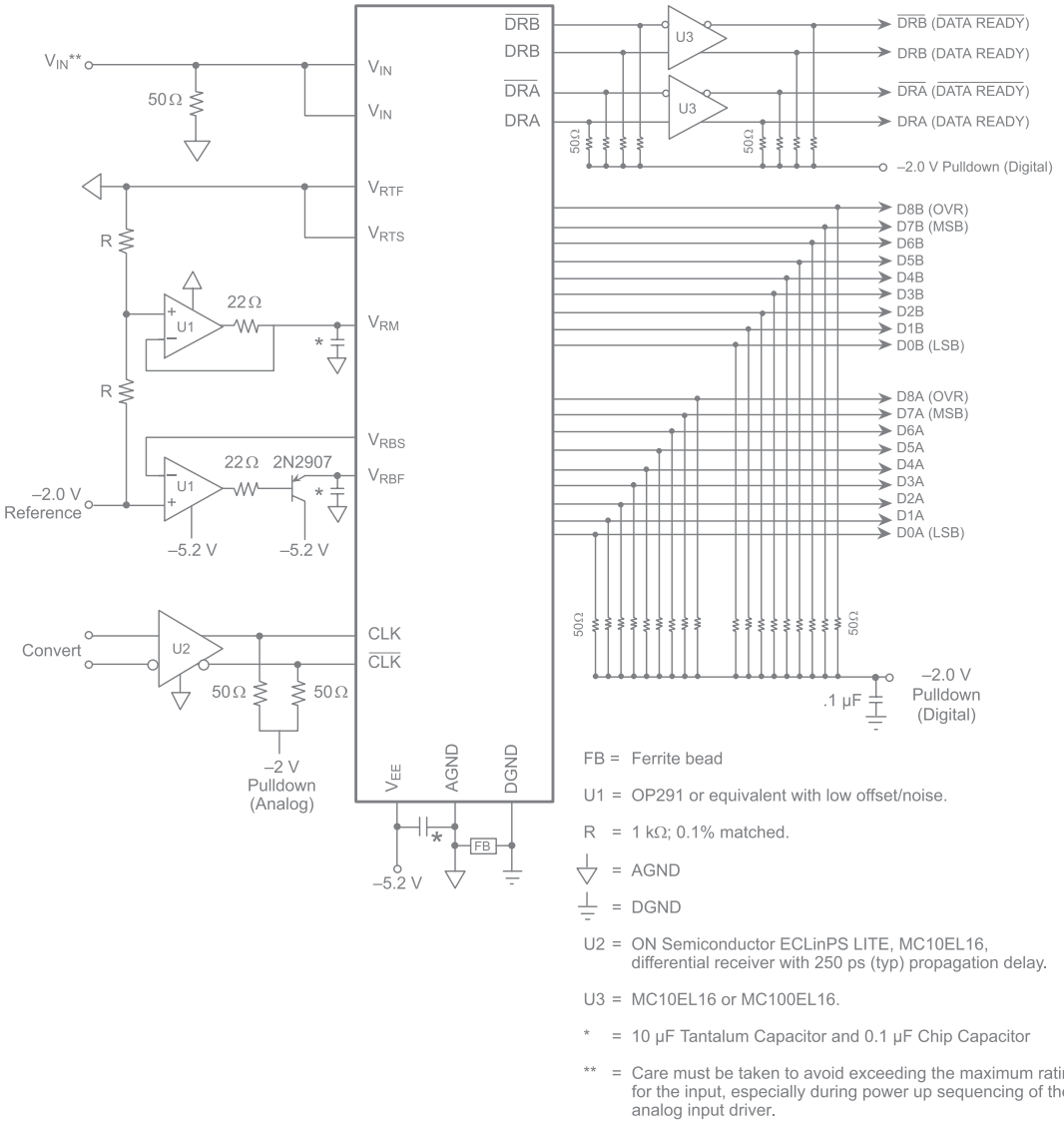


Figure 1. Typical Interface Circuit Diagram

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Typical Interface Circuit

The circuit in Figure 1 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion, and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer, and supply decoupling. Please contact the factory for the CDK1302 evaluation board application note that contains more detailson interfacing the CDK1302. The function of each pinand external connections to other components is as follows:

V_{EE}, AGND, DGND

VEE is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a 0.01µF ceramic capacitor. A 10µF tantalum can also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in Figure 1.

V_{IN} (Analog Input)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input sense and the other for input force. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The CDK1302 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion.

CLK, $\overline{CLK}$ (Clock Inputs)

The clock inputs are designed to be driven differentially with ECL levels. The duty cycle of the clock should be kept at 50% to avoid causing larger second harmonics. If this is not important to the intended application, then duty cycles other than 50% may be used.

D0 To D8, DR, DR, (A and B)

The digital outputs can drive 50Ω to ECL levels when pulled down to -2V. When pulled down to -5.2V, the outputs can drive 130Ω to 1kΩ loads. All digital outputs are grey code with the coding as shown in Table 1. Cadeka recommends using differential receivers on the outputs of the data ready lines to ensure the proper output rise and fall times.

V_{RBF}, V_{RBS}, V_{RTF}, V_{RTS}, V_{RM} (Reference Inputs)

There are two reference inputs and one external reference voltage tap. These are -2V (V_{RB} force and sense), midtap (V_{RM}) and AGND (V_{RT} force and sense). The reference pins and tap can be driven by op amps as shown in Figure 1 or V_{RM} may be bypassed for limited temperature operation. These voltage inputs can be bypassed to AGND for further noise suppression if so desired.

Table 1. Output Coding

V_{IN}	D8	D7–D0
> -0.5 LSB	1	10000000
-0.5 LSB	1 0	10000000 10000000
-1.5 LSB	0 0	10000000 10000001
• • •	• • •	• • •
> -1.0V	0 0	11000000 01000000
• • •	• • •	• • •
-2.0V +0.5 LSB	0 0	00000001 00000000
< (-2.0V +0.5 LSB)	0	00000000

Indicates the transition between the two codes

Thermal Management

The typical thermal impedance is as follows:

Θ_{CA} = +17 °C/W in still air with no heat sink

We highly recommend that a heat sink be used for this device with adequate air flow to ensure rated performance of the device. We have found that a Thermalloy 17846 heat sink with a minimum air flow of 1 meter/second (200 linear feet per minute) provides adequate thermal performance under laboratory tests. Application specific conditions should be taken into account to ensure that the device is properly heat sinked.

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Operation

The CDK1302 has 256 preamp/comparator pairs which are each supplied with the voltage from V_{RT} to V_{RB} divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at V_{IN} is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to V_{RT} (0V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

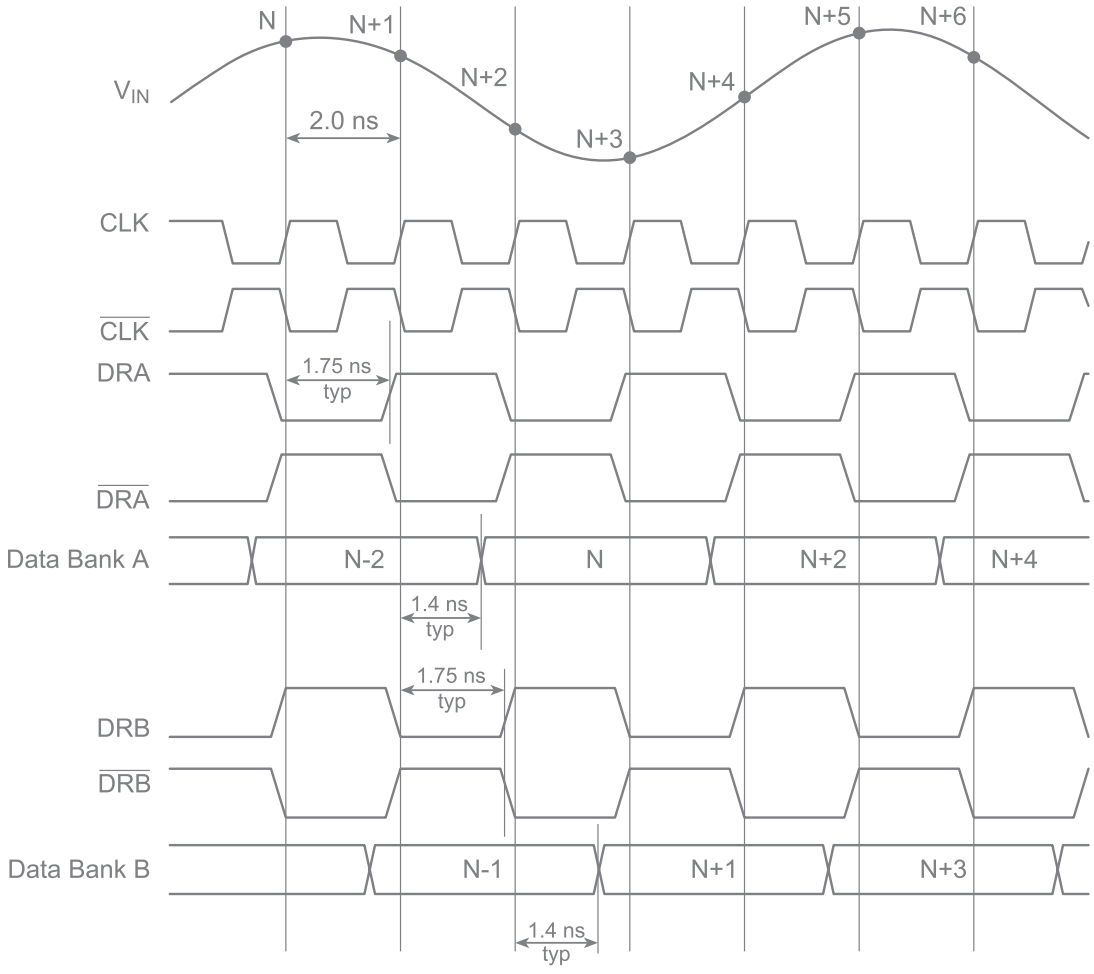
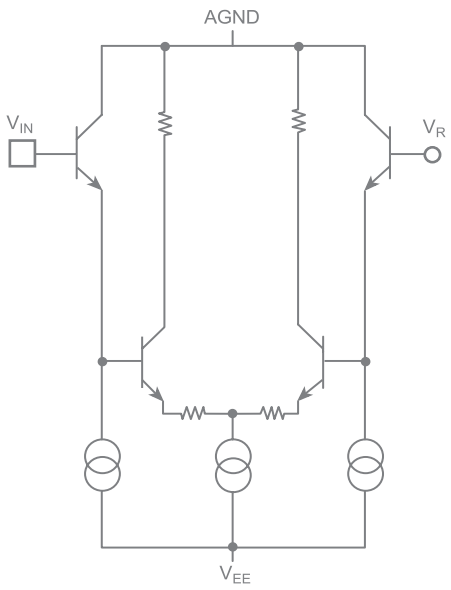


Figure 2. Timing Diagram

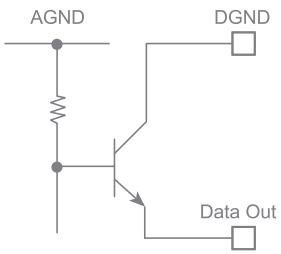
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Schematic Diagrams

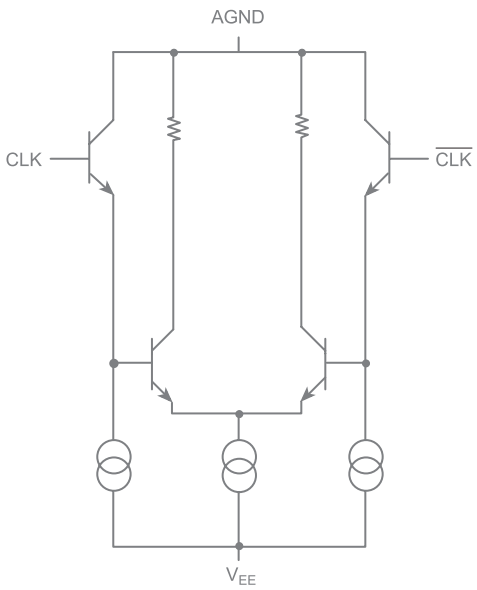
Input Circuit



Output Circuit

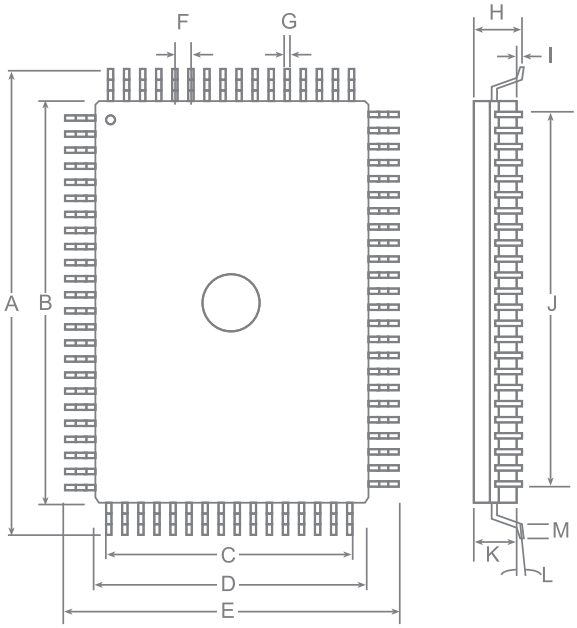


Clock Circuit



Mechanical Dimensions

MQUAD-80 Package



MQUAD-80						
	INCHES			MILLIMETERS		
SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX
A	0.904		0.923	22.95		23.45
B	0.777		0.781	19.74		19.84
C		0.472			12.00	
D	0.541		0.545	13.74		13.84
E	0.667		0.687	16.95		17.45
F		0.031			0.80	
G	0.012		0.018	0.30		0.45
H	0.109		0.134	2.76		3.40
I	0.010		0.024	0.25		0.60
J		0.724			18.40	
K	0.099		0.110	2.51		
L	0°		7°	0°		7°
M	0.029		0.041	0.73		1.03

For additional information regarding our products, please visit CADEKA at: cadeka.com

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