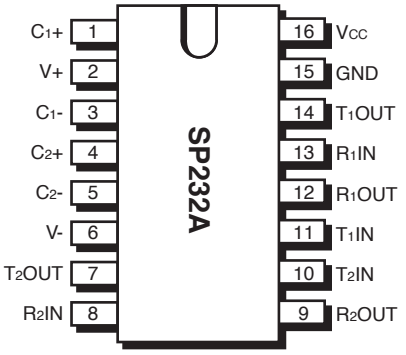
Enhanced RS-232 Line Drivers/Receivers

FEATURES

- Operates from Single +5V Power Supply
- Meets All RS-232F and ITU V.28 Specifications
- Operates with 0.1μF to 1μF Capacitors
- High Data Rate – 120Kbps Under Load
- Low Power CMOS – 3mA Operation (SP232A)
- No External Capacitors Required (SP233A)
- Low Power Shutdown (SP310A,SP312A)
- Enhanced ESD Protection (2kV Human Body Model)



Now Available in Lead Free Packaging

DESCRIPTION

The **SP232A/233A/310A/312A** devices are a family of line driver and receiver pairs that meet the specifications of RS-232 and V.28 serial protocols. These devices are pin-to-pin compatible with popular industry standards. As with the initial versions, the **SP232A/233A/310A/312A** devices feature at least 120Kbps data rate under load, 0.1μF charge pump capacitors, and overall ruggedness for commercial applications. This family also features **Sipex's** BiCMOS design allowing low power operation without sacrificing performance. The series is available in plastic DIP and SOIC packages operating over the commercial and industrial temperature ranges.

SELECTION TABLE

Model	Number of RS232 Drivers	Number of RS232 Receivers	No. of Receivers Active in Shutdown	No. of External 0.1μF Capacitors	Shutdown	WakeUp	TTL Tri–State
SP232A	2	2	N//A	4	No	No	No
SP233A	2	2	N/A	0	No	No	No
SP310A	2	2	0	4	Yes	No	Yes
SP312A	2	2	2	4	Yes	Yes	Yes

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ABSOLUTE MAXIMUM RATINGS

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{cc} ..... +6V
V^+ ..... (Vcc-0.3V) to +11.0V
V^- ..... -11.0V

Input Voltages
T_{IN} ..... -0.3 to (Vcc +0.3V)
R_{IN} ..... ±30V

Output Voltages
T_{OUT} ..... (V+, +0.3V) to (V-, -0.3V)
R_{OUT} ..... -0.3V to (Vcc +0.3V)

Short Circuit Duration
T_{OUT} ..... Continuous
Plastic DIP 375mW
(derate 7mW/°C above +70°C)
Small Outline 375mW
(derate 7mW/°C above +70°C)

ELECTRICAL CHARACTERISTICS

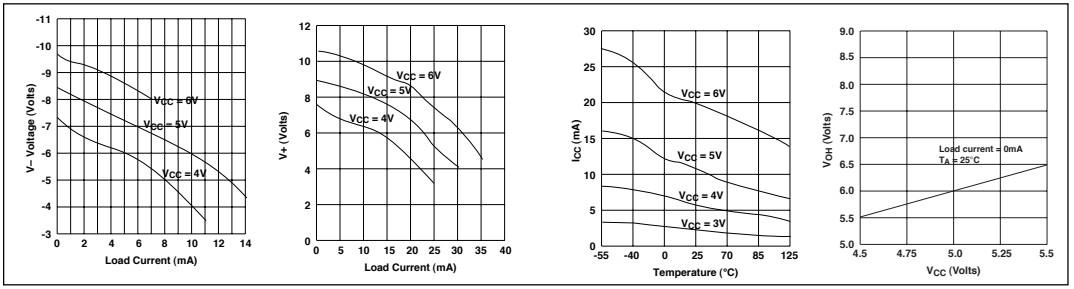
V_{CC}=+5V±10%; 0.1µF charge pump capacitors; T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TTL INPUT					
Logic Threshold					
LOW			0.8	Volts	T_{IN} ; $\overline{EN}$, $\overline{SD}$
HIGH	2.0			Volts	T_{IN} ; $\overline{EN}$, $\overline{SD}$
Logic Pull-Up Current		15	200	µA	T_{IN} = ZeroV
TTL OUTPUT					
TTL/CMOS Output					
Voltage, Low			0.4	Volts	I_{OUT} = 3.2mA; Vcc = +5V
Voltage, High	3.5			Volts	I_{OUT} = -1.0mA
Leakage Current; T_A = +25°		0.05	±10	µA	$\overline{EN}$ = V_{CC}, ZeroV≤V_{OUT} ≤V_{CC} SP310A and SP312A only
RS-232 OUTPUT					
Output Voltage Swing	±5	±6		Volts	All transmitter outputs loaded with 3kΩ to Ground
Output Resistance	300			Ohms	V_{CC} = ZeroV; V_{OUT} = ±2V
Output Short Circuit Current		±18		mA	Infinite duration
Maximum Data Rate	120	240		Kbps	C_L = 2500pF, R_L= 3kΩ
RS-232 INPUT					
Voltage Range	-30		+30	Volts	
Voltage Threshold					
LOW	0.8	1.2		Volts	V_{CC} = 5V, T_A = +25°C
HIGH		1.7	2.4	Volts	V_{CC} = 5V, T_A = +25°C
Hysteresis	0.2	0.5	1.0	Volts	V_{CC} = 5V, T_A = +25°C
Resistance	3	5	7	kΩ	T_A = +25°C, -15V ≤ V_{IN} ≤ +15V
DYNAMIC CHARACTERISTICS					
Driver Propagation Delay		1.5	3.0	µs	TTL to RS-232; C_L = 50pF
Receiver Propagation Delay		0.1	1.0	µs	RS-232 to TTL
Instantaneous Slew Rate			30	V/µs	C_L = 10pF, R_L= 3-7kΩ; T_A =+25°C
Transition Region Slew Rate		10		V/µs	C_L = 2500pF, R_L= 3kΩ; measured from +3V to -3V or -3V to +3V
Output Enable Time		400		ns	SP310A and SP312A only
Output Disable Time		250		ns	SP310A and SP312A only
POWER REQUIREMENTS					
V_{CC} Power Supply Current					
SP232A		3	5	mA	No load, T_A= +25°C; V_{CC} = 5V
SP233A, SP310A, SP312A		10	15	mA	No load, T_A= +25°C; V_{CC} = 5V
V_{CC} Supply Current,Loaded					
SP232A		15		mA	All transmitters R_L = 3kΩ; T_A = +25°C
SP233A, SP310A, SP312A		25		mA	All transmitters R_L = 3kΩ; T_A = +25°C
Shutdown Supply Current					
SP310A,SP312A		1	10	µA	V_{CC} = 5V, T_A = +25°C

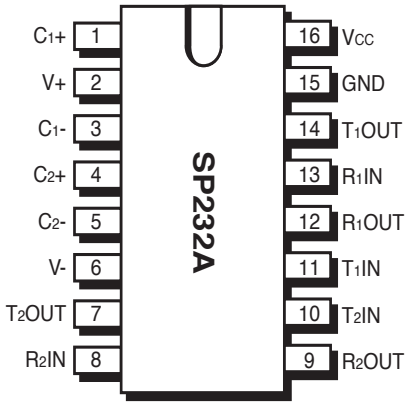
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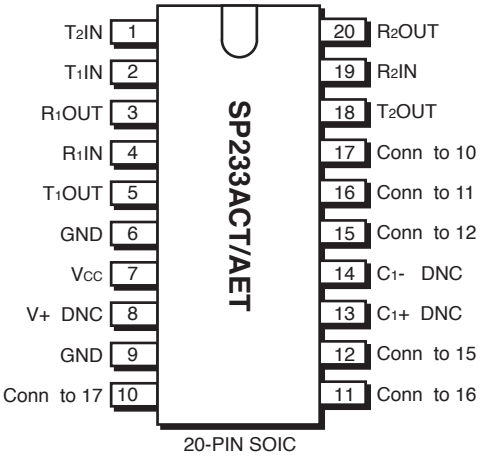
PERFORMANCE CURVES

Not 100% tested.



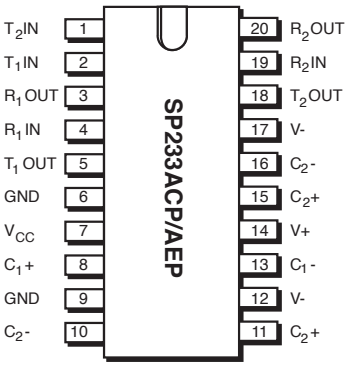
PINOUTS



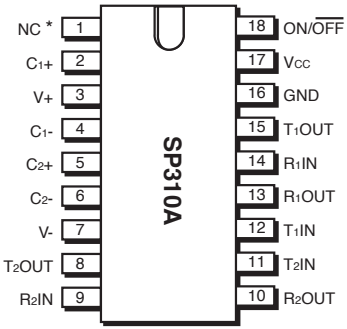


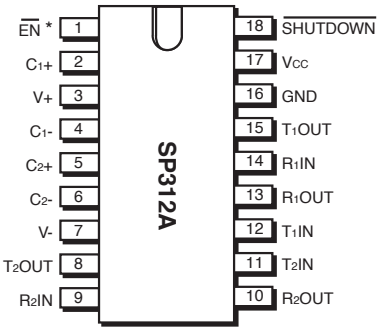
20-PIN SOIC

See Figure 2 for Pin Connections



20-PIN PLASTIC DIP





*** N.C. for SP310E_A, $\overline{EN}$ for SP312E_A**

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FEATURES...

The **SP232A/233A/310A/312A** devices are a family of line driver and receiver pairs that meet the specifications of RS-232 and V.28 serial protocols. The ESD tolerance has been improved on these devices to over ±2KV for the Human Body Model. These devices are pin-to-pin compatible with popular industry standards. The **SP232A/233A/310A/312A** devices feature10V/µs slew rate, 120Kbps data rate under load, 0.1µF charge pump capacitors, overall ruggedness for commercial applications, and increased drive current for longer and more flexible cable configurations. This family also features **Sipex's** BiCMOS design allowing low power operation without sacrificing performance.

The **SP232A/233A/310A/312A** devices have internal charge pump voltage converters which allow them to operate from a single +5V supply. The charge pumps will operate with polarized or non-polarized capacitors ranging from 0.1 to 1µF and will generate the ±6V needed for the RS-232 output levels. Both meet all EIA RS-232F and ITU V.28 specifications.

The **SP310A** provides identical features as the **SP232A** with the addition of a single control line which simultaneously shuts down the internal DC/DC converter and puts all transmitter and receiver outputs into a high impedance state. The **SP312A** is identical to the **SP310A** with separate tri-state and shutdown control lines.

THEORY OF OPERATION

The **SP232A**, **SP233A**, **SP310A** and **SP312A** devices are made up of three basic circuit blocks – 1) a driver/transmitter, 2) a receiver and 3) a charge pump. Each block is described below.

Driver/Transmitter

The drivers are inverting transmitters, which accept TTL or CMOS inputs and output the RS-232 signals with an inverted sense relative to the input logic levels. Typically the RS-232output voltage swing is ±6V. Even under worst case loading conditions of 3kOhms and 2500pF, the output is guaranteed to be ±5V, which is consistent with the RS-232 standard specifications. The transmitter outputs are protected against infinite short-circuits to ground without degradation in reliability.

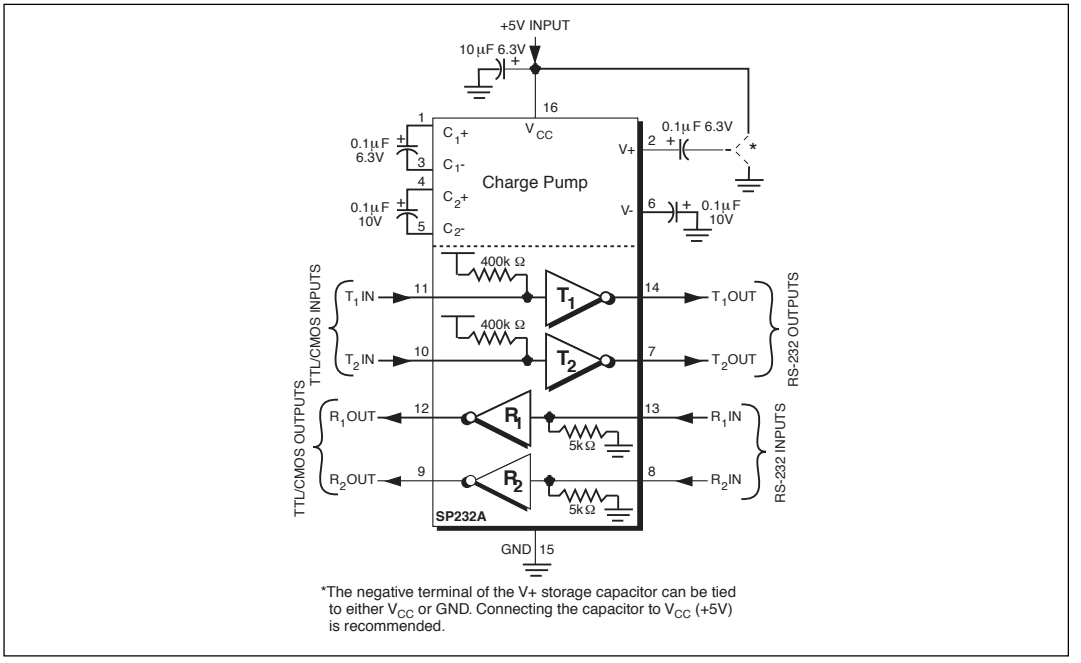


Figure 1. Typical Circuit using the SP232A.

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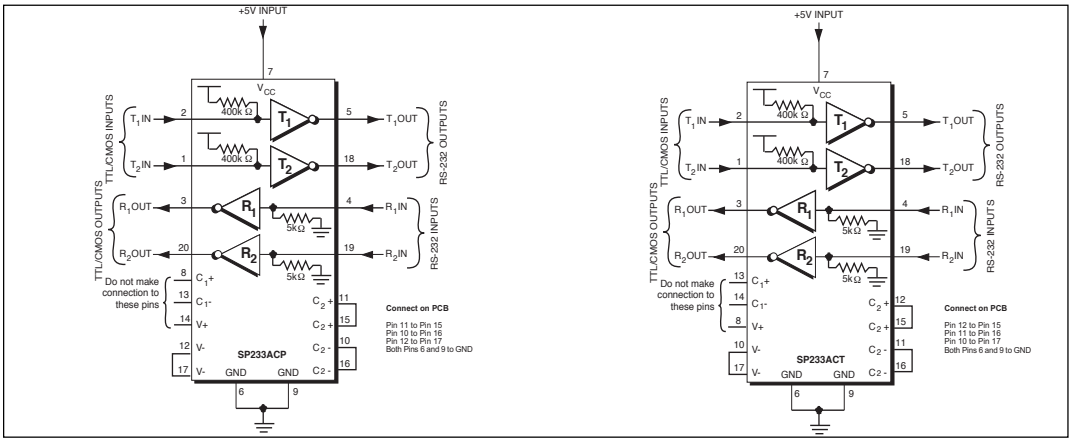


Figure 2. Typical Circuits using the SP233ACP and SP233ACT

The instantaneous slew rate of the transmitter output is internally limited to a maximum of 30V/µs in order to meet the standards [EIA RS-232-F]. The transition region slew rate of these enhanced products is typically 10V/µs. The smooth transition of the loaded output from V_{OL} to V_{OH} clearly meets the monotonicity requirements of the standard [EIA RS-232-F].

Receivers

The receivers convert RS-232 input signals to inverted TTL signals. Since the input is usually from a transmission line, where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is virtually immune to noisy transmission lines.

The input thresholds are 0.8V minimum and 2.4V maximum, again well within the ±3V RS-232 requirements. The receiver inputs are also protected against voltages up to ±25V. Should an input be left unconnected, a 5KΩ pulldown resistor to ground will commit the output of the receiver to a high state.

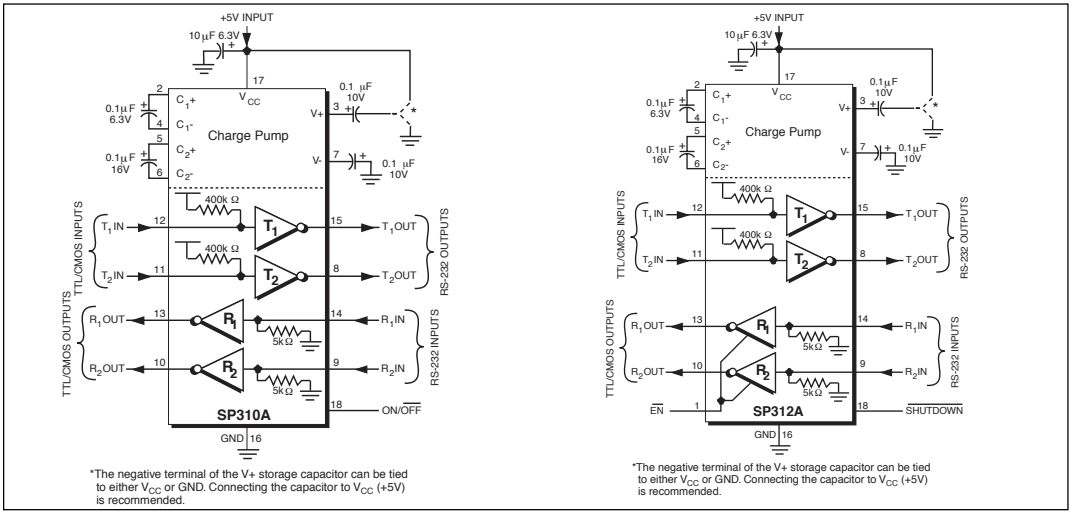


Figure 3. Typical Circuits using the SP310A and SP312A

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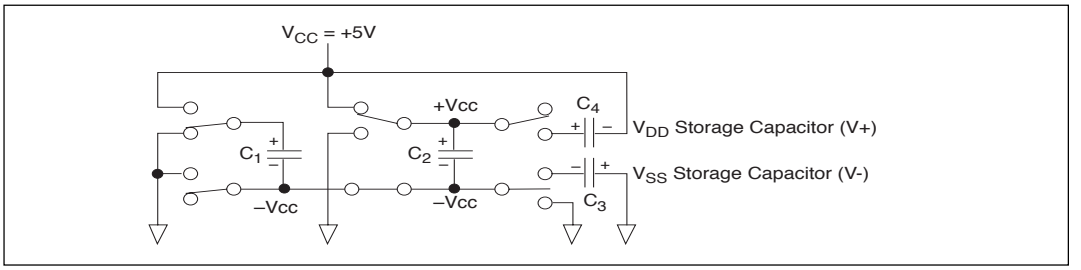


Figure 4. Charge Pump — Phase 1

In actual system applications, it is quite possible for signals to be applied to the receiver inputs before power is applied to the receiver circuitry. This occurs, for example, when a PC user attempts to print, only to realize the printer wasn't turned on. In this case an RS-232 signal from the PC will appear on the receiver input at the printer. When the printer power is turned on, the receiver will operate normally. All of these enhanced devices are fully protected.

Charge Pump

The charge pump is a **Sipex**–patented design (5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical power supplies. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage —During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –l0V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is a maximum of l0V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to ground, and transfers the generated l0V across C_2 to C_4, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V^+ and V^- are separately generated from V_{CC}; in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches

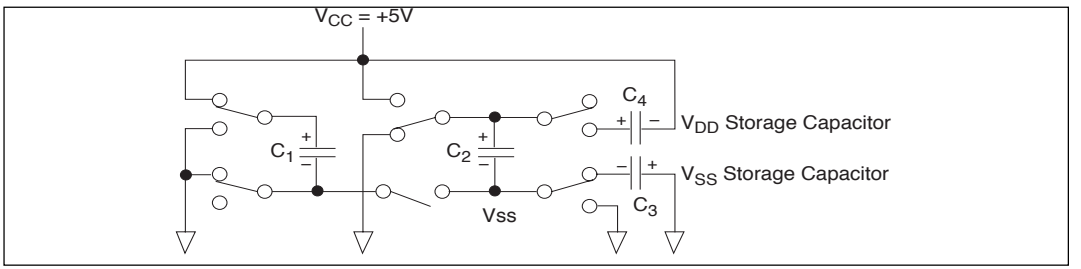


Figure 5. Charge Pump — Phase 2

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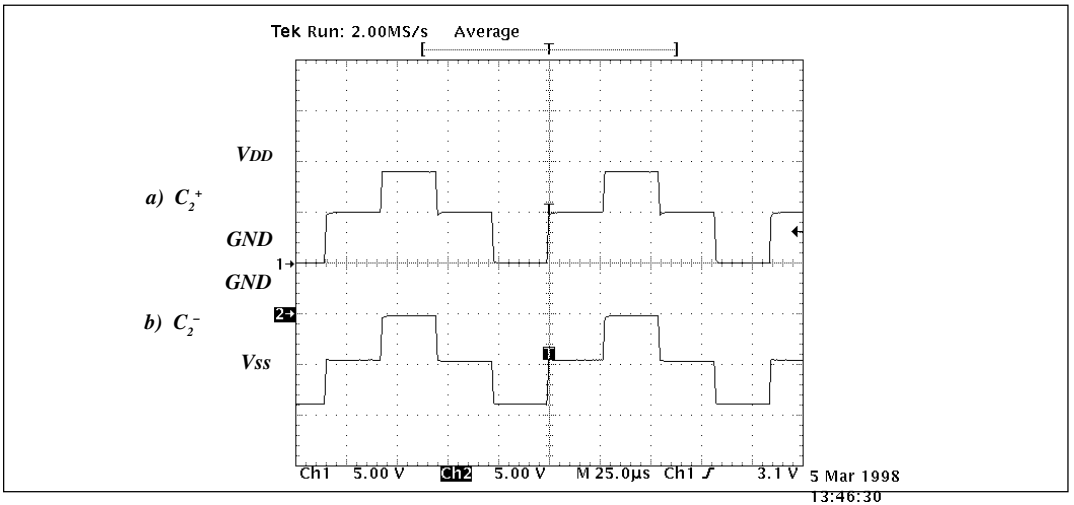


Figure 6. Charge Pump Waveforms

that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at greater than 15kHz. The external capacitors can be as low as 0.1µF with a 10V breakdown voltage rating.

Shutdown (SD) and Enable (EN) for the SP310A and SP312A

Both the **SP310A** and **SP312A** have a shutdown/standby mode to conserve power in battery-powered systems. To activate the shutdown mode, which stops the operation of the charge pump, a logic "0" is applied to the appropriate control line. For the **SP310A**, this control line is ON/OFF (pin 18). Activating the shutdown mode also puts the

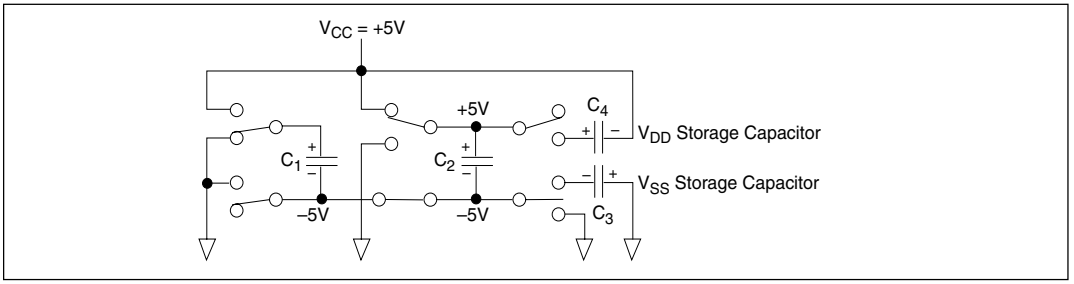


Figure 7. Charge Pump — Phase 3

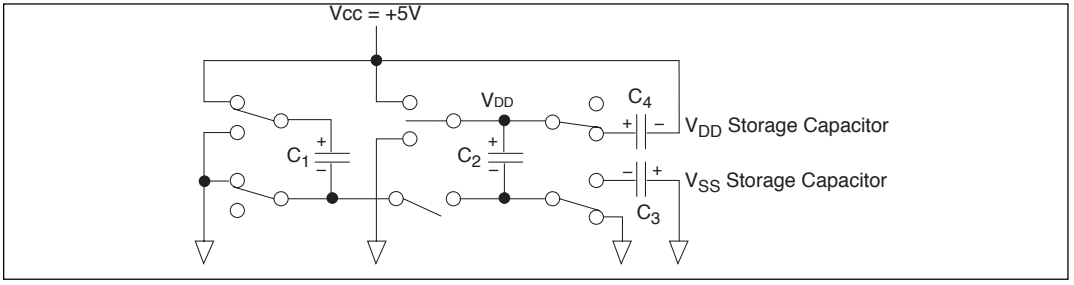


Figure 8. Charge Pump — Phase 4

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SP310A transmitter and receiver outputs in a high impedance condition (tri-stated). The shutdown mode is controlled on the **SP312A** by a logic "0" on the $\overline{\text{SHUTDOWN}}$ control line (pin 18); this also puts the transmitter outputs in a tri–state mode. The receiver outputs can be tri–stated separately during normal operation or shutdown by a logic "1" on the $\overline{\text{ENABLE}}$ line (pin 1).

Wake–Up Feature for the SP312A

The **SP312A** has a wake–up feature that keeps all the receivers in an enabled state when the device is in the shutdown mode. *Table 1* defines the truth table for the wake–up function.

With only the receivers activated, the **SP312A** typically draws less than 5µA supply current. In the case of a modem interfaced to a computer in power down mode, the Ring Indicator (RI) signal from the modem would be used to "wake up" the computer, allowing it to accept data transmission.

After the ring indicator signal has propagated through the **SP312A** receiver, it can be used to trigger the power management circuitry of the computer to power up the microprocessor, and bring the $\overline{\text{SD}}$ pin of the **SP312A** to a logic high, taking it out of the shutdown mode. The receiver propagation delay is typically 1µs. The enable time for V^+ and V^- is typically 2ms. After V^+ and V^- have settled to their final values, a signal can be sent back to the modem on the data terminal ready (DTR) pin signifying that the computer is ready to accept and transmit data.

$\overline{\text{SD}}$	$\overline{\text{EN}}$	Power Up/Down	Receiver Outputs
0	0	Down	Enable
0	1	Down	Tri–state
1	0	Up	Enable
1	1	Up	Tri–state

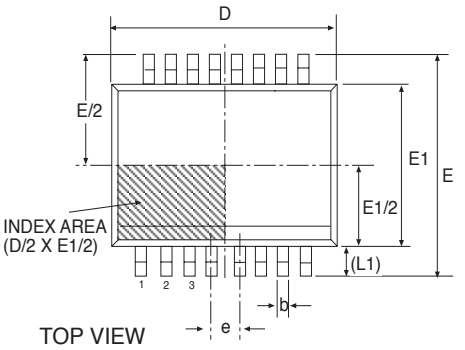
Table 1. Wake-up Function Truth Table.

Pin Strapping for the SP233ACT/ACP

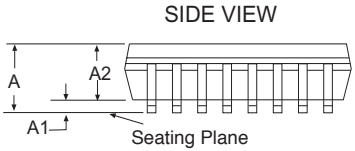
The **SP233A** packaged in the 20–pin SOIC package (**SP233ACT**) has a slightly different pinout than the **SP233A** in PDIP packaging (**SP233ACP**). To operate properly, the following pairs of pins must be externally wired together:

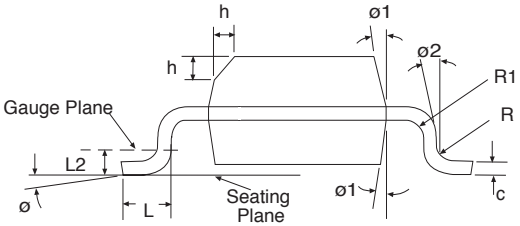
Pins Wired Together	SOIC	PDIP
Two V- Pins	10 & 17	12 & 17
Two C2+ Pins	12 & 15	11 & 15
Two C2- Pins	11 & 16	10 & 16
	No Connections for Pins 8, 13, and 14	
	Connect Pins 6 and 9 to GND	

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TOP VIEW

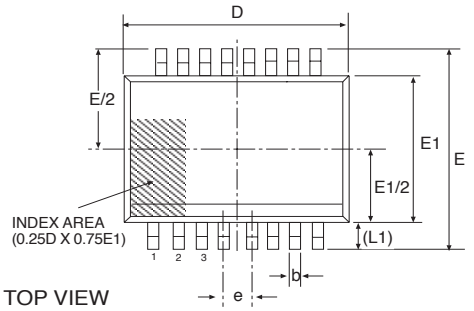


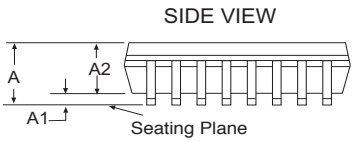


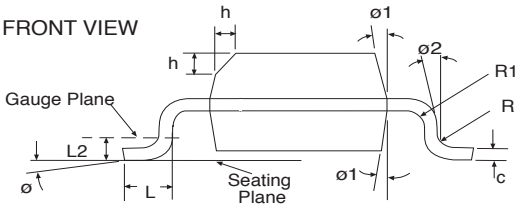
FRONT VIEW

16 Pin NSOIC		JEDEC MS-012		Variation AC		
SYMBOL	Dimensions in Millimeters: Controlling Dimension			Dimensions in Inches Conversion Factor: 1 Inch = 25.40 mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	-	1.75	0.053	-	0.069
A1	0.10	-	0.25	0.004	-	0.010
A2	1.25	-	1.65	0.049	-	0.065
b	0.31	-	0.51	0.012	-	0.020
c	0.17	-	0.25	0.007	-	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25		0.50	0.010	-	0.020
L	0.40	-	1.27	0.016	-	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
ø	0º	-	8º	0º	-	8º
ø1	5º	-	15º	5º	-	15º
ø2	0º	-	-	0º	-	-
D	9.90 BSC			0.390 BSC		
SIPEX Pkg Signoff Date/Rev:			JL Oct12 -05 / Rev A			

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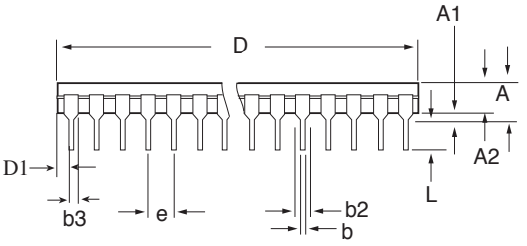


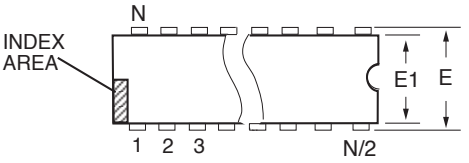


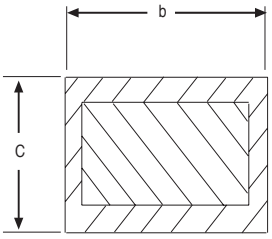


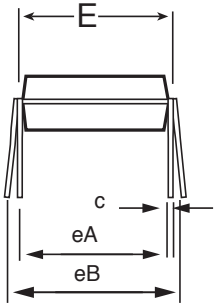
16 PIN WSOIC	JEDEC MS-013			Variation AA		
SYMBOL	Dimensions in Millimeters: Controlling Dimension			Dimensions in Inches Conversion Factor: 1 Inch = 25.40 mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	-	2.65	0.093	-	0.104
A1	0.10	-	0.30	0.004	-	0.012
A2	2.05	-	2.55	0.081	-	0.100
b	0.31	-	0.51	0.012	-	0.020
c	0.20	-	0.33	0.008	-	0.013
E	10.30 BSC			0.406 BSC		
E1	7.50 BSC			0.295 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	-	0.75	0.010	-	0.030
L	0.40	-	1.27	0.016	-	0.050
L1	1.40 REF			0.055 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
ø	0º	-	8º	0º	-	8º
ø1	5º	-	15º	5º	-	15º
ø2	0º	-	-	0º	-	-
D	10.30 REF			0.405 REF		
SIPEX Pkg Signoff Date/Rev:				JL Oct11-05/ Rev A		

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PDIP JEDEC MS-001 Common Dimensions			
Dimensions in Inches. Controlling Dimension.			
SYMBOL	MIN	NOM	MAX
A	-	-	0.21
A1	0.15	-	-
A2	0.115	0.13	0.195
b	0.014	0.018	0.022
b2	0.045	0.06	0.07
b3	0.3	0.039	0.045
c	0.008	0.01	0.014
D1	0.005	-	-
E	0.3	0.31	0.325
E1	0.24	0.25	0.28
e	.100 BSC		
eA	.300 BSC		
eB	-	-	0.43
L	0.115	0.13	0.15
PDIP JEDEC MS-001 VARIATION AB N = 16 Pins			
D	0.78	0.79	0.8
PDIP JEDEC MS-001 VARIATION AC N = 18 Pins			
D	0.88	0.9	0.92
PDIP JEDEC MS-001 VARIATION AD N = 20 Pins			
D	0.98	1.03	1.06

PDIP JEDEC MS-001 Common Dimensions			
Dimensions in Millimeters. Conversion factor: 1 inch = 25.40 mm.			
SYMBOL	MIN	NOM	MAX
A	-	-	5.33
A1	3.81	-	-
A2	2.79	3.30	4.83
b	0.25	0.25	0.51
b2	1.02	1.52	1.78
b3	7.62	0.76	1.02
c	0.00	0.25	0.25
D1	0.00	-	-
E	7.62	7.87	8.13
E1	6.10	6.35	7.11
e	2.54 BSC		
eA	7.62 BSC		
eB	-	-	10.92
L	2.79	3.30	3.81
PDIP JEDEC MS-001 VARIATION AB N = 16 Pins			
D	19.81	20.07	20.32
PDIP JEDEC MS-001 VARIATION AC N = 18 Pins			
D	22.35	22.86	23.37
PDIP JEDEC MS-001 VARIATION AD N = 20 Pins			
D	24.89	26.16	26.92

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ORDERING INFORMATION

Part Number	Temperature Range	Topmark	Package
SP232ACN	0°C to +70°C	SP232ACN	16–pin NSOIC
SP232ACN/TR	0°C to +70°C	SP232ACN	16–pin NSOIC
SP232ACP	0°C to +70°C	SP232ACP	16–pin PDIP
SP232ACT	0°C to +70°C	SP232ACT	16–pin WSOIC
SP232ACT/TR	0°C to +70°C	SP232ACT	16–pin WSOIC
SP232AEN	–40°C to +85°C	SP232AEN	16–pin NSOIC
SP232AEN/TR	–40°C to +85°C	SP232AEN	16–pin NSOIC
SP232AEP	–40°C to +85°C	SP232AEP	16–pin PDIP
SP232AET	–40°C to +85°C	SP232AET	16–pin WSOIC
SP232AET/TR	–40°C to +85°C	SP232AET	16–pin WSOIC
SP233ACP	0°C to +70°C	SP232ACP	20–pin PDIP
SP233ACT	0°C to +70°C	SP233ACT	20–pin WSOIC
SP233ACT/TR	0°C to +70°C	SP233ACT	20–pin WSOIC
SP233AEP	–40°C to +85°C	SP232AEP	20–pin PDIP
SP233AET	–40°C to +85°C	SP233AET	20–pin WSOIC
SP233AET/TR	–40°C to +85°C	SP233AET	20–pin WSOIC
SP310ACP	0°C to +70°C	SP310ACP	18–pin PDIP
SP310ACT	0°C to +70°C	SP310ACT	18–pin WSOIC
SP310ACT/TR	0°C to +70°C	SP310ACT	18–pin WSOIC
SP310AEP	–40°C to +85°C	SP310AEP	18–pin PDIP
SP310AET	–40°C to +85°C	SP310AET	18–pin WSOIC
SP310AET/TR	–40°C to +85°C	SP310AET	18–pin WSOIC
SP312ACP	0°C to +70°C	SP312ACP	18–pin PDIP
SP312ACT	0°C to +70°C	SP312ACT	18–pin WSOIC
SP312ACT/TR	0°C to +70°C	SP312ACT	18–pin WSOIC
SP312AEP	–40°C to +85°C	SP312AEP	18–pin PDIP
SP312AET	–40°C to +85°C	SP312AET	18–pin WSOIC
SP312AET/TR	–40°C to +85°C	SP312AET	18–pin WSOIC

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP312AEA/TR = standard; SP312AEA-L/TR = lead free.

/TR = Tape and Reel

Pack quantity is 1,500 for WSOIC and 2,500 for NSOIC.

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