DATA SHEET

SAA7283
Terrestrial Digital Sound Decoder (TDSD3)

Preliminary specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

Terrestrial Digital Sound Decoder (TDSD3)

SAA7283

FEATURES

- Single-chip solution including FM and vision filters, analog demodulator and audio switching
- Dual standard with automatic selection between PAL system I and BGH including French NICAM L system)
- Single low-radiation crystal oscillator for improved EMC
- Stereo bitstream audio DACs
- Programmable attenuator for matching levels of NICAM and FM audio sources at the output of the device
- Full EBU NICAM 728 specification demodulation and decoding
- Digital Audio Interface conforming with EBU/IEC 958
- Automatic mute function which switches from NICAM to FM sound when NICAM fails
- Compatible with either single-ended or differential DQPSK input signals
- Microcomputer controlled via I^{2}C-bus (up to 400 kHz specification).

APPLICATIONS

- Television receivers
- Video cassette recorders.

GENERAL DESCRIPTION

The SAA7283 is a NICAM receiver solution, developing the well established high quality Terrestrial Digital Sound decoder family from Philips Semiconductors.

This innovative IC with analog front-end, offers more impressive features and flexibility with minimum external circuitry.

The SAA7283 takes, as input, a second IF (intercarrier) Terrestrial TV PAL signal, and performs all the Differential Quadrature Phase Shift Keying (DQPSK) demodulation, digital decoding and digital-to-analog conversion necessary to produce a complete NICAM receiver on a single integrated circuit.

The demodulator function includes integrated baseband filters for pulse shaping and unwanted signal rejection, automatic gain control, a low jitter integrated VCO, digital monostable for precise data sampling points and a multi-standard controller to enable automatic locking to either a PAL system I or PAL system BGH input signal (including French NICAM L system).

The decoder function performs the descrambling, de-interleaving and reformatting operations required to recover the original data words.

The data words are processed through a stereo digital filter, digital de-emphasis network, second order noise shaper and 256 times oversampling Bitstream audio DAC. The SAA7283 then provides a switching output buffer for selecting between FM, NICAM and daisy-chain inputs, and a programmable level attenuation matrix for matching levels of the FM and NICAM audio sources at the output of the device. An additional feature is the inclusion of a Digital Audio Interface (DAI) output IEC 958, which may be disabled if required.

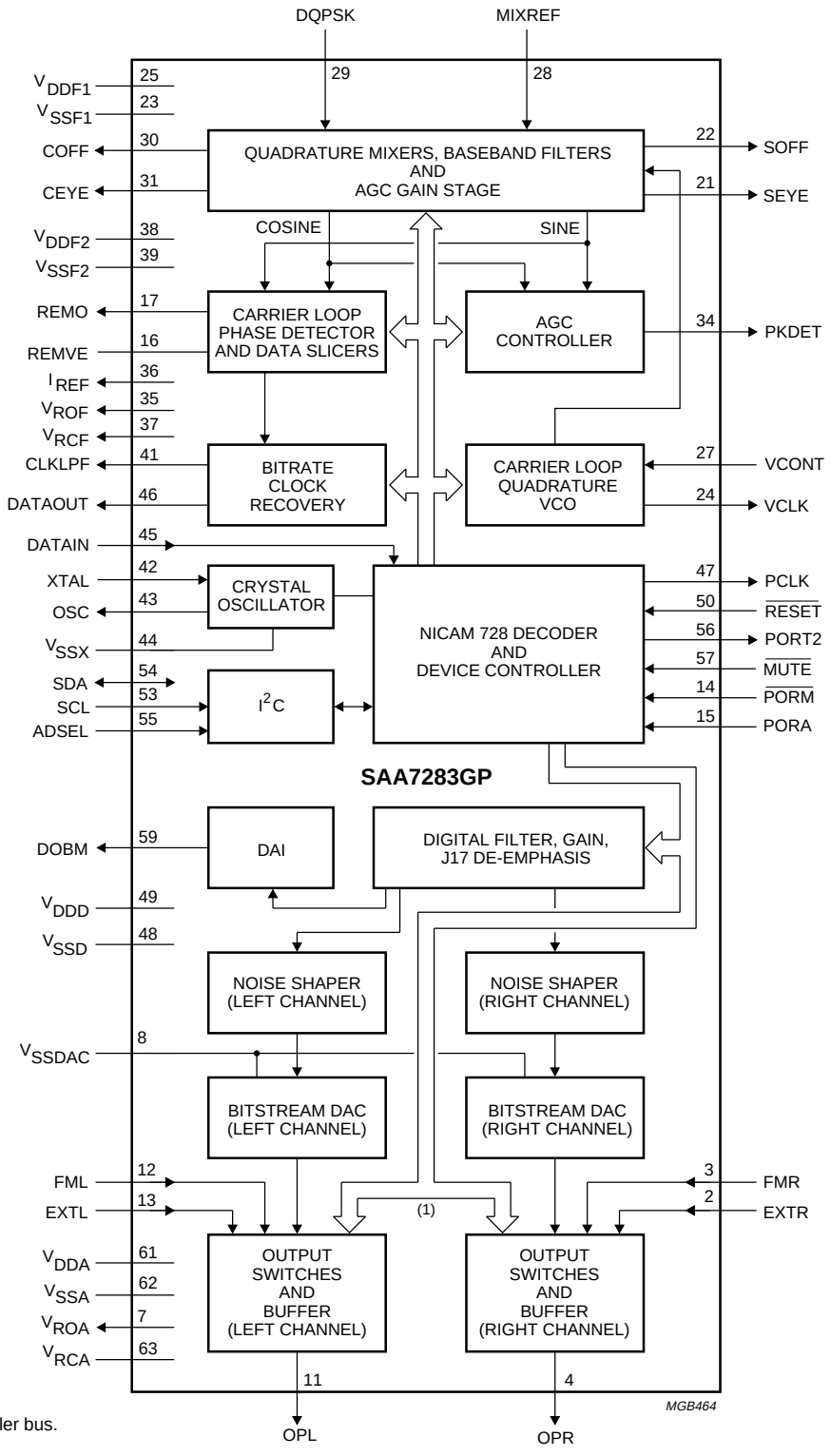
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7283ZP	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1
SAA7283GP	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	205	–	mA
f_{clk}	clock frequency	–	8.192	–	MHz
T_{amb}	operating ambient temperature	–20	+25	+70	°C

BLOCK DIAGRAM



(1) Represents controller bus.

Fig.1 Block diagram (QFP64).

PINNING

SYMBOL	PIN		DESCRIPTION
	SDIP52	QFP64[1]	
$\overline{MUTE}$	1	57	active LOW mute input; function defined by MUTEDEF (control bit in the I^2C-bus register)
DOBM	2	59	digital audio interface output that can be 3-stated via I^2C-bus
V_{DDA}	3	61	analog supply voltage for the audio channels
V_{SSA}	4	62	analog ground connection for the audio channels
V_{RCA}	5	63	internal audio reference voltage buffer (high-impedance node)
EXTR	6	2	external analog input to the right audio channel
FMR	7	3	FM sound input to the right audio channel
OPR	8	4	analog output from the right audio channel
n.c.	9 and 10	9 and 10	not connected; left open-circuit in application
V_{ROA}	11	7	internal audio reference voltage buffer output
V_{SSDAC}	12	8	quiet ground connection to DACs
n.c.	13 and 14	–	not connected; left open-circuit in application
OPL	15	11	analog output from the left audio channel
FML	16	12	FM sound input to the left audio channel
EXTL	17	13	external analog input to the left audio channel
$\overline{PORM}$	18	14	active LOW power-on reset mute input; mute cleared by setting silence bit HIGH in I^2C-bus (internal pull-up)
PORA	19	15	power-on reset audio select input (internal pull-up)
REMVE	20	16	carrier loop-filter connection
REMO	21	17	carrier loop-filter output
SEYE	22	21	sine channel eye pattern output for monitoring
SOFF	23	22	sine channel offset compensator capacitor output
V_{SSF1}	24	23	demodulator ground connection 1
VCLK	25	24	carrier loop VCO clock output for monitoring
V_{DDF1}	26	25	demodulator supply voltage 1
VCONT	27	27	carrier loop VCO control voltage input
MIXREF	28	28	mixer voltage reference or input when using differential DQPSK signal
DQPSK	29	29	DQPSK input signal
COFF	30	30	cosine channel offset compensator capacitor output
CEYE	31	31	cosine channel eye pattern output for monitoring
PKDET	32	34	AGC peak detector storage capacitor output
V_{ROF}	33	35	internal demodulator reference voltage buffered output
I_{REF}	34	36	internal demodulator reference current output
V_{RCF}	35	37	internal demodulator reference voltage unbuffered output
V_{DDF2}	36	38	demodulator supply voltage 2
V_{SSF2}	37	39	demodulator ground connection 2
n.c.	38	40	not connected; left open-circuit in application
CLKLPF	39	41	clock loop-phase comparator output

SYMBOL	PIN		DESCRIPTION
	SDIP52	QFP64[1]	
XTAL	40	42	8.192 MHz crystal oscillator input
OSC	41	43	8.192 MHz crystal oscillator output
V_{SSX}	42	44	crystal oscillator ground connection
DATAIN	43	45	serial data input at 728 kbits/s to decoder
V_{SSD}	44	48	digital ground connection
PCLK	45	47	728 kHz output clock to DQPSK demodulator
V_{DDD}	46	49	digital supply voltage
$\overline{\text{RESET}}$	47	50	active LOW power-on reset input
DATAOUT	48	46	serial data output at 728 kbits/s from DQPSK demodulator
SCL	49	53	serial clock input for I^2C-bus
SDA	50	54	serial data input/output for I^2C-bus
ADSEL	51	55	input that defines I^2C-bus address bit 0 (internal pull-up)
PORT2	52	56	output that is directly controlled from Port 2 bit in I^2C-bus

Note

1. Pins 1, 5, 6, 18, 19, 20, 26, 32, 33, 51, 52, 58, 60 and 64 are not connected; left open-circuit in application.

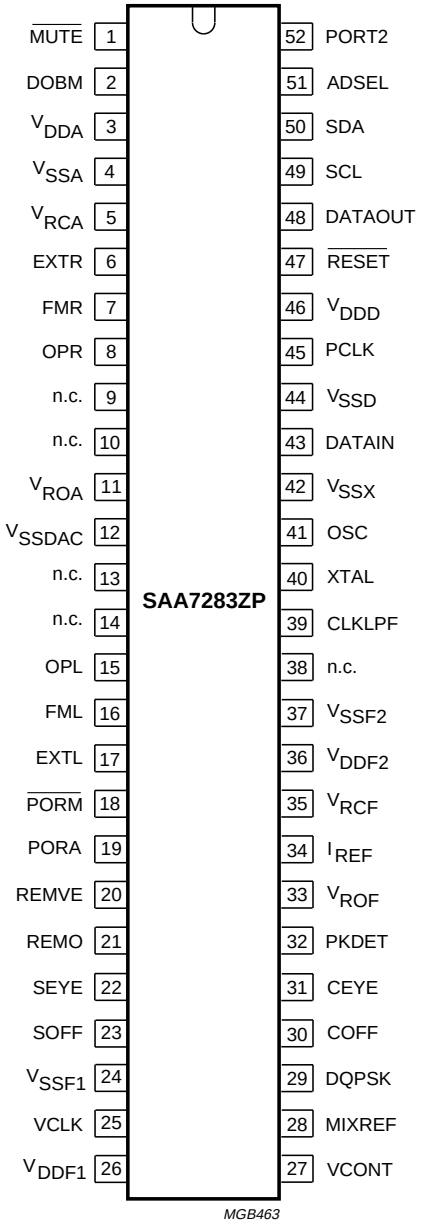


Fig.2 Pin configuration for SOT247.

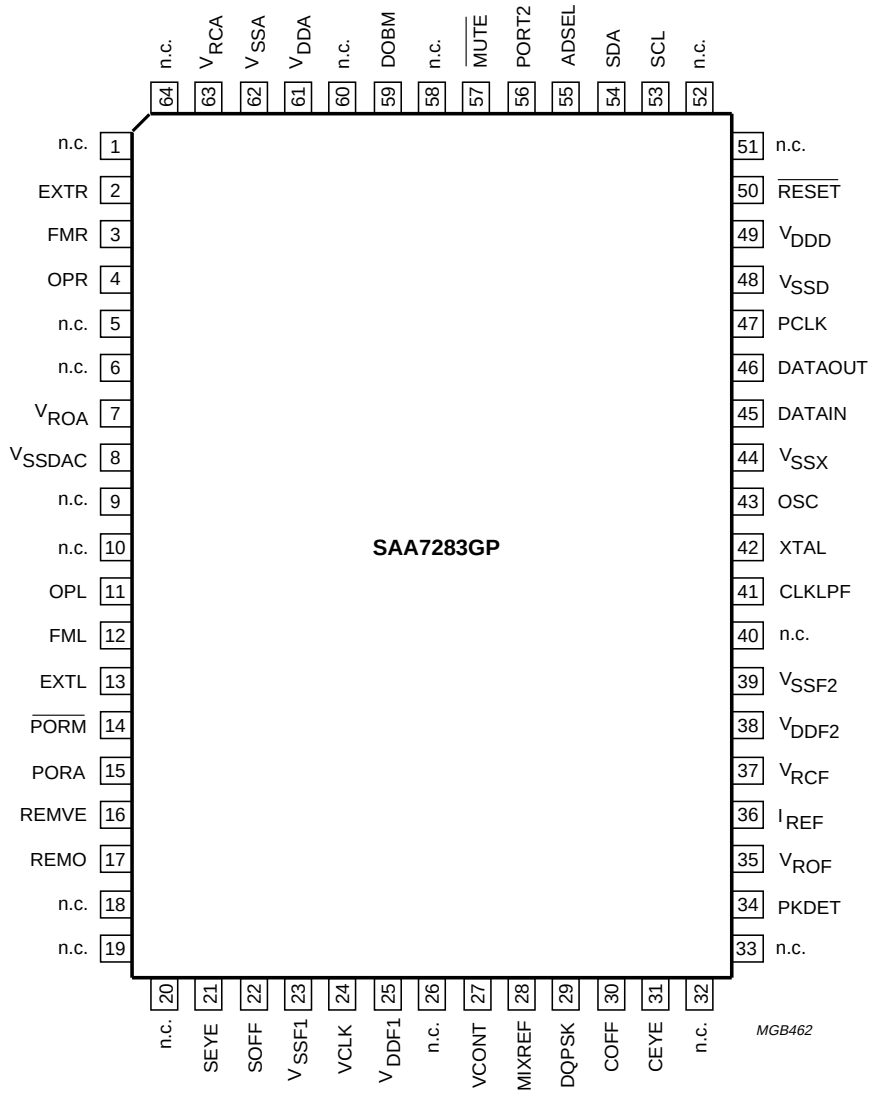


Fig.3 Pin configuration for SOT319.

FUNCTIONAL DESCRIPTION

DQPSK demodulation

QUADRATURE MIXERS, BASEBAND FILTERS AND AUTOMATIC GAIN CONTROL (AGC)

The DQPSK signal is fed into two differential input mixers, where it is mixed with quadrature phases generated by the carrier-loop quadrature VCO. The quadrature signals modulated onto the NICAM carrier are thus recovered.

The mixers can be driven by either a single-ended or differential source. In single-ended mode, the device is driven directly from the sound IF down-converter into the DQPSK input pin, with the MIXREF pin decoupled.
In differential mode, the signal is applied between the DQPSK and MIXREF pins.

The outputs from the mixers are then fed into a pulse-shaping filter, and FM/vision filter stage which filters out all interference components, including AM carrier for French NICAM L system. The signal from the filtering stages is then fed into the AGC, which ensures that the phase comparator gain remains constant, irrespective of the input signal level. This is important to maintain the stability of Costas loop PLL.

AGC CONTROLLER

The AGC controller monitors the I and Q channel signals at the input to the carrier loop-phase comparator and generates a reference voltage to set the AGC output level.

EYE BUFFER

A differential to the single-ended converter provides the baseband signal as an output at the pins CEYE and SEYE for the I and Q channels respectively for eye-height monitoring.

BIT RATE CLOCK RECOVERY

The I and Q channels are processed using edge detectors and monostables, which generate a signal with a coherent component at the data symbol rate. The outputs from the I and Q channel monostables are each compared with the clock derived from PCLK (364 kHz nominal), the resultant output is used to derive a 3-state control signal used to control two current sources at the CLKLPF output.
This error signal is loop filtered and used to control the master clock oscillator. The bit rate clock, PCLK, and symbol clock are derived from the master clock.

NICAM 728 decoding

DECODING FUNCTIONS

The device performs all decoding functions in accordance with the EBU NICAM 728 specification. After locking to the frame alignment word, the data is de-scrambled by application of the defined pseudo random binary sequence, and the device synchronizes to the periodic frame flag bit C0.

The relevant control information and scale factor word is extracted, and with the integrated RAM the data is de-interleaved and the scale factor word is extracted, and expanded to 14 bits. Parity checking on the eleventh bit of each sample word is carried out to reveal any sound sample errors, which if detected are flagged, with the last good sample being held.

Automatic muting

Enable when AMDIS = LOW. The I^2C-bus section has two registers which define an upper and lower limit for the automatic muting function. When the number of errors within a 128 ms period exceeds the number stored in the upper error limit register, then the automatic muting will switch the device output to the FM input, (dependent on the relevant control bits in the I^2C-bus) and mute (set to zero) the data input to the filter (in that order). When the error count in a 128 ms period is less than the value stored in the lower error limit register then the data into the filter is uninterrupted, and the device output is switched back to the DAC (dependent on the value of the relevant control bits in the I^2C-bus). During the muting operation the open-drain pin $\overline{\text{MUTE}}$ is pulled LOW and the AM bit in the status-byte is set HIGH. Figure 4 shows the dependency of the automatic muting function on error_count, RSSF, $\overline{\text{C4OV}}$, output state and application mode. The automatic muting function, if enabled, will override user mute via the $\overline{\text{MUTE}}$ pin/bit.

When the transmission is DATA format or currently undefined format (C3 = logic 1) the device will automatically switch to the FM inputs regardless of RSSF/$\overline{\text{C4OV}}$ states, and whether the automatic muting function AMDIS is enabled or disabled.

User mute

The error counter is an 8-bit counter which locks at count 255. The counter is reset and its output sent to the I²C-bus every 128 ms. This enables the user to interrogate the number of errors occurring within a 128 ms period. The user can then mute the device by pulling pin $\overline{\text{MUTE}}$ LOW (this function is also provided by the $\overline{\text{MUTE}}$ bit in the I²C-bus) or setting SILENCE bit LOW in I²C-bus to switch input of audio switching buffers to analog ground.

Switching buffers

The analog switches select between the output of the DACs, the FM input and an external input (EXT). Switching is controlled by bits in the I²C-bus and internal switching function. The external analog inputs should be ≤1.1 V (RMS) at the input pin, and the output buffers have a voltage drive of 1 V (RMS).

NICAM/FM audio level matching

Differing audio headroom and alignment levels occur between systems I and BGH, due to the differing systems and broadcast standards. In order to match the NICAM and FM audio output levels without requiring application changes, the device will automatically switch in 4.6 dB attenuation network in the NICAM path for system BGH (this can be disabled by setting the NICLEV bit LOW in I²C-bus). A programmable attenuation network in the FM path only, controlled by bits in I²C-bus, provides additional flexibility for user to match FM and NICAM audio levels (see Table 9).

Power-on reset state

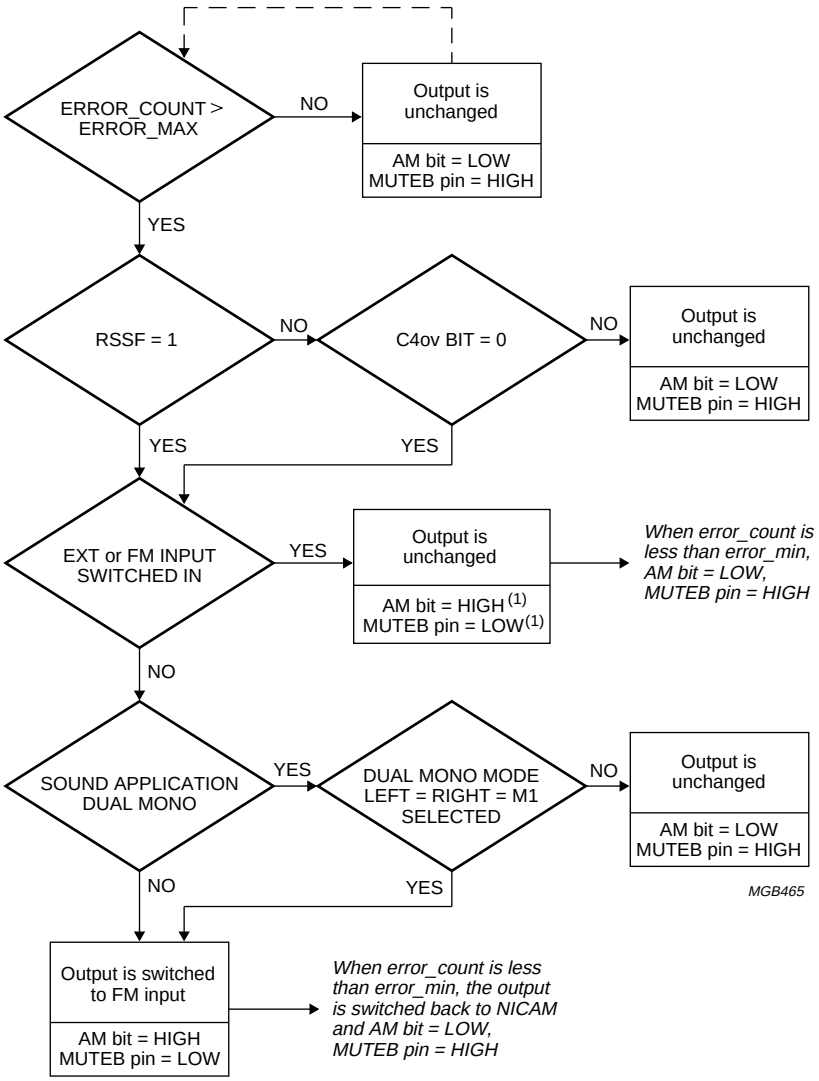
Two pins control the initial set-up of the device during power-on reset.

PORA (Power-On Reset Audio)

When pulled LOW the device will be configured with a 12 dB gain in the oversampling filter and the $\overline{\text{C4OV}}$ bit in the I²C-bus will be set HIGH. This pin when HIGH will configure the device with a 6 dB gain in the oversampling filter and will set $\overline{\text{C4OV}}$ bit in the I²C-bus LOW.

$\overline{\text{PORM}}$ (Power-On Reset Mute)

This pin when LOW will mute the output of the device at power-on by setting the SILENCE bit in the I²C-bus LOW. To put the device back into a normal mode of operation the SILENCE bit in the I²C-bus must be set HIGH.



(1) Indicating that a mute may occur when user returns to NICAM source.

Fig.4 Flow diagram showing SAA7283 automatic muting function.

I²C-BUS FORMATS

The SAA7283 contains an I²C-bus slave transceiver (up to 400 kHz) permitting a master device to:

- Read decoder status information derived from the transmitted digital audio signal
- Read an error count byte to determine the bit error rate for user mute purposes and to indicate quality of NICAM signal
- Write control codes to select PAL I or PAL BGH configurations
- Write control codes to select the available analog switching configurations
- Write upper and lower error count limits for automatic muting function
- Read additional transmitted data bits. Their purpose has yet to be defined but accessibility is provided to allow future services to be implemented in receiver software.

I²C-bus slave address

An address select pin (ADSEL) is provided to allow selection of one of two different slave addresses. The logic state of the ADSEL pin is reflected in the least significant bit of the I²C-bus slave address.

Slave address = 101101X (R/$\overline{W}$) [ADSEL = 1, address = B6 (R/$\overline{W}$) ADSEL = 0, address = B4 (R/$\overline{W}$)].

Table 1 SAA7283 slave address

BITS							
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
1	0	1	1	0	1	selected by ADSEL	read/write

The SAA7283 does not acknowledge the I²C-bus general call address.

Slave receiver format

The slave receiver format is shown in Table 2.

Table 2 Slave receiver format

START	slave_addr	ACK	sub_addr	ACK	data_byte	ACK	n-bytes	data_byte	ACK	STOP

Table 3 Explanation of Table 2

ITEM	DESCRIPTION
START	I²C-bus start condition
Slave_addr	101101XW
X	logic 0 when ADSEL = 0; logic 1 when ADSEL = 1
W	logic 0, I²C-bus write to slave receiver
ACK	I²C-bus acknowledge condition generated by slave receiver
Sub_addr	sub-address range 00 to 04 (HEX)
Data_byte	data byte transmitted to slave receiver
STOP	I²C-bus stop condition

The sub-address is auto-incremented by the SAA7283, for each data byte received. When the sub-address is equal to 04 (HEX), on reception of the next data byte, the sub-address will reset to 00 (HEX).

I²C-bus slave receiver register map

Table 4 Slave receiver data byte

SUB-ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
000	M1/$\overline{M2}$	DMSEL	SSWIT3	SSWIT2	SSWIT1	PORT2	MUTEDEF	AMDIS
001	EMAX7	EMAX6	EMAX5	EMAX4	EMAX3	EMAX2	EMAX1	EMAX0
010	EMIN7	EMIN6	EMIN5	EMIN4	EMIN3	EMIN2	EMIN1	EMIN0
011	$\overline{C4OV}$	$\overline{MUTE}$	SILENCE	DAIE	FM3	FM2	FM1	FM0
100	ASYS	BG/$\overline{I}$	NICLEV	STLOCK	–	–	–	–

M1/$\overline{M2}$

This bit selects either mono channel M1 or M2 to be the output on the left and right channel dependent on the transmitted control bits C1 and C2 indicating a mono transmission and the value of bit DMSEL (see Table 5). Power-on resets to logic 1.

DMSEL

DMSEL is the dual mono selection bit, for transmissions consisting of two independent mono signals. Selection is in conjunction with M1/$\overline{M2}$ (see Table 5). Power on resets to logic 0.

SSWIT1, SSWIT2 AND SSWIT3

These bits control the analog switching, selecting between the FM, external, and NICAM signals. With the NICAM source the signals select whether the de-emphasis is performed and what gain is applied after the filtering and de-emphasis stage. The signal states and their meaning are listed in Table 7. Power-on resets to 010 with PORA pin HIGH, and to 011 with PORA pin LOW.

PORT2

PORT2 controls a bit out, providing direct access to a dedicated output pin (PORT2) via the I²C-bus. See Table 6. Power-on resets to logic 0.

MUTEDEF

This defines the operation of the user definable $\overline{MUTE}$ pin or $\overline{MUTE}$ I²C-bus bit when it is pulled LOW externally or set LOW in the I²C-bus respectively.

When this bit is HIGH, pulling the $\overline{MUTE}$ pin/I²C-bus bit LOW will mute (set to zero) the digital data and switch the output to the FM input, depending on relevant control bits (see Table 8). When this bit is LOW, pulling the $\overline{MUTE}$ pin/I²C-bus bit LOW will only mute the digital data under the same conditions. Power-on resets to LOW.

AMDIS

This bit enables and disables the automatic mute function. Power-on resets to enabled = LOW.

EMAX7 TO EMAX0

This is the upper error limit register which defines the number of errors in 128 ms period which will cause automatic mute to switch IN. User definable, but power-on resets to 50 (HEX).

EMIN7 TO EMIN0

This is the lower error limit register which defines the number of errors in 128 ms period which will cause automatic mute to switch OUT. User definable, but power-on resets to 14 (HEX).

$\overline{C4OV}$

When set LOW this bit overrides the status of the transmitted C4-bit when muting. When this bit is HIGH muting takes place in accordance with EBU specification. Power-on resets to HIGH when the PORA pin is held LOW during power-up, and power-on resets to LOW when PORA is HIGH.

$\overline{MUTE}$

This reflects the function of the MUTEB pin. When this bit is set LOW the external MUTEB pin is pulled LOW and the action is dependent on the MUTEDEF bit (see Table 8). Power-on resets to HIGH.

SILENCE

When set LOW this bit silences the outputs of the device by switching the input of the audio switching buffers to analog ground. When the $\overline{PORM}$ pin is held LOW at power-on reset the silence bit is initialized to zero. With PORM bit HIGH the silence bit is initialized HIGH.

DAIE

When set HIGH this bit switches in the Digital Audio Interface output to the DOBM pin. When set LOW the DOBM output is 3-stated. Power-on resets to HIGH.

FM3 TO FM0

These bits set the level of attenuation of the FM audio signal (see Table 9). Power-on resets 0000 = 0 dB attenuation.

ASYS

When this bit is HIGH it activates the automatic standard switch mode. When set LOW, the standard must be set by the BG/$\bar{I}$ bit. Power-on resets to HIGH.

BG/$\bar{I}$

When this bit is HIGH it switches the DQPSK demodulator to system BGH and attenuates the digital audio level by 4.6 dB (if NICLEV is set HIGH). When LOW, the DQPSK demodulator switches to system I (with no 4.6 dB attenuation). Power-on resets to HIGH.

NICLEV

When this bit is set LOW it overrides the 4.6 dB NICAM audio level compensation, irrespective of whether the device is in automatic or manual system mode. When set HIGH the 4.6 dB compensation level is applied in system BGH. Power-on resets to HIGH.

STLOCK

When STLOCK is set HIGH it will stop the automatic system switch after the device has achieved an INSYNC condition, should the demodulator lose lock at any time. This minimizes the re-acquisition time. When set LOW the device will be permitted to change system after an INSYNC condition has been reached. Power-on resets to LOW.

Table 5 Output as a function of M1/$\overline{M2}$ and DMSEL

DMSEL	M1/$\overline{M2}$	FUNCTION
0	0	selects DIGITAL; L = M2, R = M2
0	1	selects DIGITAL; L = M1, R = M1
1	0	selects DIGITAL; L = M2, R = M1
1	1	selects DIGITAL; L = M1, R = M2

Table 6 Port 2 control

PORT2	PIN OUTPUT STATE
0	LOW
1	HIGH

Table 7 SSWIT signal states and function

SSWIT3	SSWIT2	SSWIT1	FUNCTION
0	0	0	NICAM source de-emphasis switched out, no gain
0	0	1	NICAM source de-emphasis switched in, no gain
0	1	0	NICAM source de-emphasis switched in, +6 dB gain; power-on reset when PORA = HIGH
0	1	1	NICAM source de-emphasis switched in, +12 dB gain; power-on reset when PORA = LOW
1	X[1]	0	external inputs switched in, no change to previous de-emphasis/gain setting
1	X	1	FM inputs switched in, no change to previous de-emphasis/gain setting

Note

1. Where X = don’t care.

Table 8 Action of pulling $\overline{\text{MUTE}}$ pin/I²C-bus bit LOW

TRANSMITTED C4 BIT (RSSF)	$\overline{\text{C4OV}}$	TRANSMISSION MODE	OUTPUT ACTION(1)	
			MUTEDEF = 1	MUTEDEF = 0
1	1 or 0	stereo/mono/dual mono with L and R = M1	mute digital data and switch to FM	mute digital data only
1	1 or 0	dual mono with M2 selected in either L or R	no action	no action
0	1	all modes	no action	no action
0	0	all modes	mute digital data and switch to FM	mute digital data only

Note

1. With $\overline{\text{MUTE}}$ pin/i²C-bus bit pulled LOW. If user has manually selected FM or NICAM inputs, no switching will occur.

Table 9 FM attenuation control

FM ATTENUATION (dB)	FM3	FM2	FM1	FM0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
Not defined	1	1	0	1
Not defined	1	1	1	0
Not defined	1	1	1	1

Slave transmitter format

The slave transmitter format is shown in Table 10.

Table 10 Slave transmitter format

START	slave_addr	ACK	data_byte	ACK	n-bytes	data_byte	$\overline{\text{ACK}}$	STOP

Table 11 Explanation of Table 10

ITEM	DESCRIPTION
START	I^2C-bus start condition
Slave_addr	101101XR
X	logic 0 when ADSEL = 0; logic 1 when ADSEL = 1
R	logic 1, I^2C-bus read from slave transmitter
ACK	I^2C-bus acknowledge condition generated by slave receiver
Data_byte	data byte transmitted from slave receiver
$\overline{ACK}$	master device negative acknowledge to indicate last byte
STOP	I^2C-bus stop condition

I^2C slave transmitter register map

The bus master can perform single-byte, two-byte, three-byte, four-byte or five-byte read in the order shown in Table 12.

Table 12 Slave transmitter data byte

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
STATUS BYTE 1	PONRES	S/$\overline{M}$	D/$\overline{S}$	VDSP	RSSF	O$\overline{S}$	AM	$\overline{CFC}$
ERROR BYTE	ERR7	ERR6	ERR5	ERR4	ERR3	ERR2	ERR1	ERR0
AD BYTE 0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
AD BYTE 1	OVW	SAD	0	CI1	CI2	AD10	AD9	AD8
STATUS BYTE 2	C1	C2	C3	BG/$\overline{I}$	0	0	0	0

PONRES

When set HIGH this bit indicates that a power-on reset has occurred. It is cleared after the status byte has been read.

S/$\overline{M}$

This bit gives the stereo or mono broadcast indication. Set HIGH indicates stereo transmission.

D/$\overline{S}$

When HIGH this bit indicates a dual mono broadcast.

VDSP

When this bit is HIGH, it indicates that the digital data transmission is a sound source. When LOW the transmission is either data or undefined format.

RSSF

This bit reflects the state of the C4 bit in the NICAM transmission. When set LOW, the FM sound content does not match the digital transmission, and switching to FM by automatic mute or setting $\overline{MUTE}$ LOW is prevented (if $\overline{C4OV}$ = HIGH).

O$\overline{S}$

When HIGH this bit indicates that the device has both frame and C0 (16 frame) synchronization.

AM

When HIGH this bit indicates that the automatic mute function has switched from NICAM to FM. When LOW the automatic mute function has not activated a switch.

$\overline{CFC}$

When LOW this bit indicates a configuration change at the C0 (16 frame) boundary. it is reset after reading the status byte.

ERR7 TO ERR0

These bits indicate the number of errors occurring in the previous 128 ms period.

AD7 TO AD0

These bits contain the eight least significant additional data bits.

OVW

This bit is set when new additional data bits are written to the I^2C-bus without the previous bits being read.

SAD

This bit is set HIGH when new additional data is written into the I^2C-bus, and cleared by the action of reading the data.

CI1 AND CI2

These are the CI bits decoded by majority logic from the parity checks of the last ten samples in a frame.

AD10, AD9 AND AD8

These are the three most significant additional data bits.

C1, C2 AND C3

These are the transmitted control bits, see Table 13.

BG/$\overline{I}$

When set HIGH this bit indicates that the DQPSK demodulator is switched to system BGH. When LOW, indicates that DQPSK demodulator is switched to system I.

Indicator bits

Table 13 is the truth table for the indicator bits.

Table 13 Indicator bits functional truth table

TRANSMISSION	C1	C2	C3	S/$\overline{M}$	D/$\overline{S}$	VDSP	$\overline{OS}$
Stereo	0	0	0	1	0	1	1
M1 + M2	0	1	0	0	1	1	1
M1 + data	1	0	0	0	0	1	1
Transparent data	1	1	0	0	0	0	1
Any currently undefined combination of C1, C2 and C3				0	0	0	1
Decoder unsynchronized ($\overline{OS}$ = logic 0)				0	0	0	0

DIGITAL AUDIO INTERFACE IEC/EBU 958

Block structure

The output is grouped into a block of 192 consecutive frames providing, for each channel the 192 channel status data bits. The start of a block is designated by a special sub-frame preamble.

Frame structure

Each frame is uniquely composed of two sub-frames. The rate of transmission of frames corresponds exactly to the source sampling frequency. In the 2-channel operation, samples taken from both channels are transmitted by time multiplexing in consecutive sub-frames. Sub-frames related to Channel 1 (left or 'A' channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However the preamble is changed to preamble B once every 192 frames. This defines the block structure used to organize the channel status information. Sub-frames of Channel 2 (right or 'B' channel in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

Sub-frame structure

Each frame is divided into 32 time-slots numbered 0 to 31.

Time-slots 0 to 3 carry one of three permitted preambles. These are used to affect synchronization of sub-frames, frames and blocks.

Time-slots 4 to 27 carry the audio sample word in linear two's complement representation. The most significant bit is carried by time-slot 27.

Time-slot 28 carries the validity flag associated with the audio sample word. This flag is set to logic 0 if the audio sample is reliable. If set to logic 1 then the sample is unreliable.

Time-slot 29 carries one bit of the user data channel. In this application this is not used and so is set to logic 0.

Time-slot 30 carries one bit of the channel status word associated with the audio channel transmitted in the same sub-frame.

Time-slot 31 carries a parity bit such that time-slots 4 to 31 inclusive will carry an even number of ones and an even number of zeros.

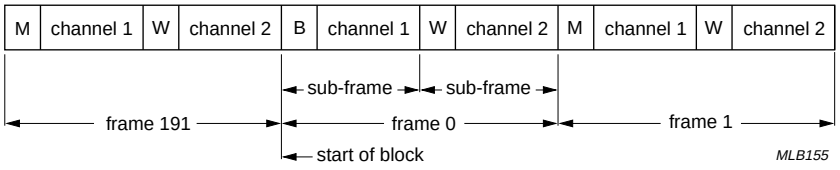


Fig.5 Frame format.

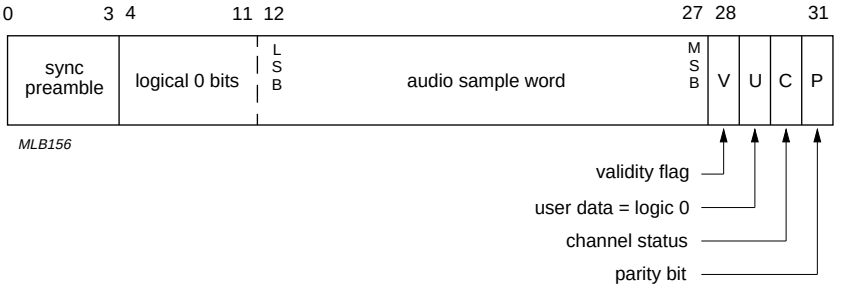


Fig.6 Sub-frame structure.

Channel coding

Time-slots are encoded as biphase mark data. Each bit transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit being transmitted is logic 0, however it is different if the bit is logic 1 (see Table 14).

Table 14 Channel coding

PRECEDING STATE	0	1
TRANSMITTED BIT	CHANNEL CODING	
0	11	00
1	10	01

Preambles

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks.

A set of three preambles is used. These preambles are transmitted in the time allocated to four time-slots and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol. Depending on this state the preambles are as shown in Table 15.

Table 15 Preambles

PRECEDING STATE	0	1
PREAMBLE	CHANNEL CODING	
B	11101000	00010111
M	11100010	00011101
W	11100100	00011011

The preambles preceding each digital audio sample are used to indicate the beginning of a sample as follows:

- **Preamble B** indicates the start of Channel A data and the beginning of a block
- **Preamble M** indicates the start of Channel A data but not the beginning of a block
- **Preamble W** indicates the start of Channel B data.

Channel status

The channel status information is organized in 192-bit words. The first bit of each word is carried in the frame with Preamble B. The 192-bit word is organized into sections as shown in Table 16.

Table 16 Channel status codes

BIT	CODE	DESCRIPTION
0	0	consumer
1	0	sound data
2	1	digital copy permitted
3 and 4	00	indicates digital de-emphasis switched in
	11	indicates digital de-emphasis switched out
5	0	–
6 and 7	00	–
8 to 5	00110001	category code
16 to 19	0000	source code (don't care)
20 to 23	0000	channel number (don't care)
24 to 27	1100	sampling frequency (32 kHz)
28 and 29	00	clock accuracy (level II)
30 to 191	all 0s	–

LIMITING VALUES

In accordance with the Absolute Maximum Rating Systems (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDF1}, V_{DDF2}, V_{DDA}	supply voltage (all supplies)	note 1	–0.3	+6.5	V
V_{SSF1}, V_{SSF2}, V_{SSA}	ground supply voltage		V_{SSD} – 0.5	V_{SSD} + 0.5	V
$V_{I(max)}$	maximum input voltage (any input)		0	V_{DD}	V
$V_{O(max)}$	maximum output voltage		0	V_{DD}	V
I_{IOK}	DC input or output diode current		–	±20	mA
$I_{O(max)}$	output current (each output)		–	±10	mA
T_{amb}	ambient operating temperature		–20	+70	°C
T_{stg}	storage temperature		–55	+125	°C
	electrostatic handling				
$V_{stat(HBM)}$	Human Body Model	note 2	–2 000	+2 000	V
$V_{stat(MM)}$	Machine Model	note 3	–200	+200	V

Notes

1. All V_{DD} and V_{SS} connections must be made externally to the same power supply.
2. Electrostatic handling is equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a 15 ns rise time.
3. Electrostatic handling is equivalent to discharging a 200 pF capacitor via a 0 Ω series resistor with a 15 ns rise time.

QUALITY AND RELIABILITY

This device will meet Philips Semiconductors General Quality Specification for Business group *"Consumer Integrated Circuits SNW-FQ-611-Part E"*.

SYSTEM PERFORMANCE

Bit Error Rate (BER)

Table 17 shows input signal conditions which typically produce bit error rates of less than 10^{-3}. Signal levels given in dB are related to the picture carrier reference level (0 dB) and based on the output level of the Philips range of sound IF down-converter ICs. All measurements at 2nd IF (intercarrier) frequencies (NICAM and FM only) using Philips Semiconductors TDSD3 Applications Board.

Table 17 System performance

INPUT SIGNAL CONDITIONS	SYSTEM I	SYSTEM BG	UNIT
FM overmodulation [NICAM = –20 dB, FM = –10 dB (I)/–13 dB (B/G)]	170	105	kHz
NICAM level with respect to picture carrier (FM deviation = ±50 kHz) FM = –10 dB (I)/–13 dB (B/G)	–44	–43	dB
NICAM carrier-to-noise ratio (NICAM = –20 dB, FM deviation = ±50 kHz) FM = –10 dB (I)/–13 dB (B/G)	9	10.5	dB

Acquisition time

Maximum acquisition time = 1 s, measured from power-on reset to in-sync condition achieved.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = –20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital supplies (note 1)						
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
V_{SSD}	digital ground supply voltage		–	0	–	V
I_{DDD}	digital supply current		–	15	–	mA
Audio supplies (note 1)						
V_{DDA}	audio supply voltage		4.5	5.0	5.5	V
V_{SSA}	audio ground supply voltage		–	0	–	V
V_{SSDAC}	DAC ground supply voltage		–	0	–	V
I_{DDA}	audio supply current		–	19	–	mA
Demodulator supplies (note 1)						
V_{DDF1}	1st front-end supply voltage		4.5	5.0	5.5	V
V_{SSF1}	1st front-end ground supply voltage		–	0	–	V
I_{DDF1}	1st front-end supply current		–	46	–	mA
V_{DDF2}	2nd front-end supply voltage		4.5	5.0	5.5	V
V_{SSF2}	2nd front-end ground supply voltage		–	0	–	V
I_{DDF2}	2nd front-end supply current		–	125	–	mA
Digital inputs						
DATAIN (TTL/CMOS COMPATIBLE INPUT LEVELS)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
I_{LI}	input leakage current		–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
ADSEL, $\overline{\text{PORM}}$ AND PORA (TTL/CMOS COMPATIBLE INPUT LEVELS WITH INTERNAL PULL-UP)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
$R_{i(pu)}$	input pull-up resistance		–	50	–	kΩ
C_i	input capacitance		–	–	10	pF
$\overline{\text{RESET}}$ AND SCL (CMOS/I^{2}C-BUS INPUT LEVELS WITH SCHMITT TRIGGER)						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}	V
V_{hys}	hysteresis		–	$0.05V_{DD}$	–	V
I_{LI}	input leakage current		–10	–	+10	µA
C_i	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input/output						
SDA (I^2C-BUS LEVELS WITH SCHMITT TRIGGER/OPEN-DRAIN OUTPUT)						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}	V
V_{hys}	hysteresis		$0.05V_{DD}$	–	–	V
I_{LI}	input leakage current		–10	–	+10	μA
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = +3 mA	0	–	0.4	V
C_L	load capacitance					
	active pull-up		–	–	400	pF
	passive pull-up		–	–	200	pF
$\overline{\text{MUTE}}$ (TTL/CMOS COMPATIBLE INPUT LEVELS/OPEN-DRAIN OUTPUT WITH INTERNAL PULL-UP)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = +3 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –3 mA	2.4	–	V_{DD}	V
C_i	load capacitance with active pull-up		–	–	50	pF
Z_i	input impedance		–	50	–	kΩ
Digital outputs						
PORT2, PCLK AND DATAOUT (PUSH-PULL OUTPUT)						
V_{OL}	LOW level output voltage	I_{OL} = +2 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
DOBM (3-STATE PUSH-PULL OUTPUT)						
V_{OL}	LOW level output voltage	I_{OL} = +2 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	–10	–	+10	μA
ANALOG SECTION (measured at V_{DD} = 5 V; T_{amb} = 25 °C)						
Demodulator analog references						
V_{RCF} OUTPUT						
V_o	output signal voltage	supply dependent	–	$0.5V_{DDF2}$	–	V
C_i	input capacitance		–	–	10	pF
V_{ROF} OUTPUT						
V_o	output signal voltage	defined by V_{RCF}	–	$0.5V_{DDF2}$	–	V
C_i	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{REF} OUTPUT						
V_o	output signal voltage	defined by V_{RCF}	–	$0.5V_{DDF2}$	–	V
C_i	input capacitance		–	–	10	pF
I_{sink}	output sink current	with external 10 kΩ resistor from pin to V_{SSF2}	–	250	–	μA
Signal path analog inputs						
DQPSK AND MIXREF						
R_i	input resistance		–	12.5	–	kΩ
$V_{iDQPSK(rms)}$	NICAM input signal voltage V_{nom} (RMS value)		–	43	–	mV
V_{iDR}	AGC range	with respect to V_{iDQPSK}	+8.5	+10	–	dB
			–25	–30	–	dB
$V_{iCUM(rms)}$	cumulative input signal voltage (RMS value)	note 2	–	–	464	mV
C_i	input capacitance		–	–	10	pF
Baseband outputs						
CEYE AND SEYE						
$V_{o(p-p)}$	eye pattern output signal voltage (peak-to-peak value)	in-lock; note 3; system I	–	1.25	–	V
		in-lock; note 3; system B/G	–	1.79	–	V
$V_{I/Q}$	channel matching	$20\log_{10}(V_{CEYE}/V_{SEYE})$	–2	0	+2	dB
COFF AND SOFF						
V_O	offset compensator DC output voltage	defined by V_{RCF}	–	$0.5V_{DDF2}$	–	V
Baseband filters						
SYSTEM I						
Af_o	pass band cut-off attenuation	f_i = 6552 MHz + 182 kHz	1.9	3.1	4.6	dB
FMr	FM rejection	f_i = 6.0 MHz ± 50 kHz	–	65	–	dB
FMomr	FM rejection (overmodulated FM)	f_i = 6.0 MHz ± 80 kHz	45	50	–	dB
CCr	colour-carrier rejection	f_i = 4.43 MHz	–	78	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SYSTEM BGH						
Af_o	pass band cut-off attenuation	f_i = 5850 MHz + 182 kHz	1.7	3.1	4.5	dB
FMr	FM rejection	f_i = 5.5 MHz ± 50 kHz	–	50	–	dB
AMr (SECAM)	AM rejection (for SECAM L system)	f_i = 6.5 MHz	–	56	–	dB
FMomr	FM rejection (overmodulated FM)	f_i = 5.5 MHz ± 80 kHz	25	30	–	dB
CCr	colour-carrier rejection	f_i = 4.43 MHz	–	73	–	dB
Baseband demodulator output						
REMO						
V_o	output voltage limits		0.2	–	V_{DD} – 0.5	V
K_p	carrier loop-phase detector gain	system I	–	1.2	–	V/rad
		system B/G	–	0.9	–	V/rad
f_p	carrier loop pull-in frequency		4	–	–	kHz
Φ_{offset}	carrier loop-phase detector offset	phase shift = 45°	–4	0	+4	deg
f_n	carrier loop bandwidth (natural frequency)		2	–	5	kHz
Baseband remodulator filter feedback						
REMVE						
V_o	carrier loop filter virtual earth voltage	defined by V_{RCF}	–	$0.5V_{DDF2}$	–	V
Fine frequency calibration current (on to REMVE node)						
I_{source}	output source current		–	15	–	µA
I_{sink}	output sink current		–	15	–	µA
I_{LI}	3-state leakage current		–0.25	0	+0.25	µA
f_{fstep}	fine frequency calibration step		0.8	2	8	kHz
Voltage controlled oscillator						
VCONT						
V_i	input signal voltage		0.5	–	V_{DD} – 0.5	V
C_i	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VCO (MEASURED AT V_{CLK} PIN)						
f_{VCO}	VCO frequency after DAC calibration	f_{SYS} = 6552 MHz (system I) or f_{SYS} = 5.85 MHz (system BGH)	f_{SYS} – 75	–	f_{SYS} + 75	kHz
	VCO frequency after fine frequency calibration		f_{SYS} – 4	–	f_{SYS} + 4	kHz
K_{VCO}	VCO slope	system I	–139	–186	–232	kHz/V
		system B/G	–191	–255	–319	kHz/V
DAC_{STEP}	VCO calibrating DAC step size		–50	+30	+50	kHz
ItoQ	in-phase to quadrature phase accuracy		–	90	–	deg
φ_j	VCO phase jitter	note 4	–	–	8.1	ns
Clock recovery loop and crystal oscillator						
XTAL						
C_i	input capacitance		–	–	10	pF
V_{bias}	DC bias voltage		–	3.63	–	V
OSC						
$V_{osc(p-p)}$	oscillator voltage amplitude (peak to peak value)		–	1.4	–	V
V_{bias}	DC bias voltage		–	2.33	–	V
G_v	small signal voltage gain		–	1.0	–	V/V
C_o	output capacitance		–	–	10	pF
CRYSTAL SPECIFICATION (FUNDAMENTAL MODE)						
f_i	crystal input frequency		–	8.192	–	MHz
C_L	load capacitance		–	15	–	pF
C1	series capacitance		21	–	–	fF
C0	parallel capacitance		–	–	5	pF
S	pulling sensitivity	determined by C_L, C1 and C0	–26.25	–	–	10^{-6}/pF
R_r	resonance resistance		–	–	40	Ω
R_{DLD}	resonance resistance; drive level dependency		–	–	120	Ω
X_a	ageing		–	–	±5	10^{-6}/year
T_{range}	temperature range		–20	+25	+70	°C
X_j	adjustment tolerance		–	–	±30	10^{-6}
X_d	drift	across T_{range}	–	–	±30	10^{-6}
CLOCK RECOVERY LOOP CURRENT SOURCE (CLKLPF)						
I_{LI}	3-state leakage current at ½ phase shift	$0.5 \leq V_{CLKLPF} \leq V_{DD} - 0.5$; note 5	–5	0	+5	µA
φ_{gm}	phase comparator transconductance	$0.5 \leq V_{CLKLPF} \leq V_{DD} - 0.5$; note 5	57	63.5	70	µA/rad

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog references						
V_{RCA} OUTPUT						
V_o	output signal voltage	supply dependent	–	$0.5V_{DDA}$	–	V
C_i	input capacitance		–	–	10	pF
V_{ROA} OUTPUT						
V_o	output signal voltage	defined by V_{RCA}	–	$0.5V_{DDA}$	–	V
C_i	input capacitance		–	–	10	pF
Digital filter						
f_s	output sample frequency		–	128	–	kHz
PR	pass band ripple	at 0 Hz to 15 kHz	–	–	±0.01	dB
SBA	stop band attenuation	at f ≥ 17 kHz	30	–	–	dB
Digital de-emphasis						
DEV	deviation from ideal		–	–	±0.09	dB
FM audio inputs						
FML AND FMR (SELECTED VIA I^2C-BUS CONTROL)						
Z_i	input impedance	0 dB FM attenuation set	–	40	–	kΩ
		–12 dB FM attenuation set	–	160	–	kΩ
G	output gain	programmable in 1 dB steps	–	0 to 12	–	dB
G_a	output gain accuracy		–0.5	0	+0.5	dB
$V_{ain(rms)}$	input voltage level (RMS value)		–	–	1.1	V
S/N	signal-to-noise ratio		90	95	–	dB
THD	total harmonic distortion		–	–85	–70	dB
EXT audio input						
EXTL AND EXTR (SELECTED VIA I^2C-BUS CONTROL)						
Z_i	input impedance		–	40	–	kΩ
G	output gain		–	0	–	dB
G_a	output gain accuracy		–	0	–	dB
$V_{ain(rms)}$	input voltage level (RMS value)		–	–	1.1	V
S/N	signal-to-noise ratio		90	95	–	dB
THD	total harmonic distortion		–	–85	–70	dB
NICAM internal DAC (selected via I^2C-bus control)						
$V_{o(rms)}$	NICAM output voltage level (RMS value)	0 dB; V_{ROA} = 2.5 V	0.94	1	1.06	V
THD+N	total harmonic distortion plus noise	notes 6 and 7	–	–80	–75	dB
DIGS	digital silence level	$\overline{\text{MUTE}}$ on	–	–80	–	dB
AUDIOS	audio silence level	SILENCE on = 0	–80	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio outputs						
OPL AND OPR						
C_L	output load capacitance		–	–	300	pF
R_L	output load resistance		3	–	–	kΩ
CHM	channel matching	0 dB, 1 kHz	–0.5	0	+0.5	dB
PSRR	power supply rejection ratio		–	40	–	dB
Timing (all timing values refer to V_{IH} and V_{IL} levels)						
DATAIN WITH RESPECT TO PCLK (see Fig.9)						
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		250	–	–	ns
SDA WITH RESPECT TO SCL(see Fig.10)						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{BUF}	bus free time		1300	–	–	ns
$t_{HD;STA}$	START code hold time		600	–	–	ns
t_{LOW}	SCL clock LOW time		1300	–	–	ns
t_{HIGH}	SCL clock HIGH time		600	–	–	ns
$t_{SU;STA}$	START code set-up time		600	–	–	ns
$t_{HD;DAT}$	data hold time	note 8	0	–	–	ns
$t_{SU;DAT}$	data set-up time	note 9	100	–	–	ns
t_r	SDA and SCL rise time		50	–	300	ns
t_f	SDA and SCL fall time		50	–	300	ns
$t_{SU;STO}$	STOP code set-up time		600	–	–	ns

Notes

1. It is assumed that all supplies are externally connected at the same source, and consequently that maximum and minimum values apply simultaneously to each supply.
2. Cumulative input level based on FM at 0 dB and NICAM at –10 dB with respect to picture carrier.
3. The signal amplitude present at the SEYE and CEYE pins depends on whether the demodulator is in or out-of-lock. When out-of-lock, the signal at the pins is $\sqrt{2}$ times the in-lock situation.
4. VCO jitter is measured in System I over 100 cycles of the VCO clock.
5. With 10 kΩ resistor from I_{REF} to V_{SSF2}.
6. Audio performance is limited by the dynamic range of the NICAM 728 system. Due to compansion, the quantization noise is never lower than –62 dB with respect to the input level.
7. Measured with a –30 dB, 1 kHz NICAM 728 input signal.
8. Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.
9. If a fast I²C-bus device is used in an up to 100 kbit/s I²C-bus system, then the requirement $t_{SU;DAT} \geq 250$ ns is always fulfilled if this device cannot stretch the LOW level of the SCL signal. If a device stretches the LOW level of the SCL signal, then data to SDA must be asserted ($t_{RD(max)} + t_{SU;DAT}$) = 1000 + 250 = 1250 ns before the SCL signal is released to be compatible with the up to 100 kbit/s I²C-bus specification.

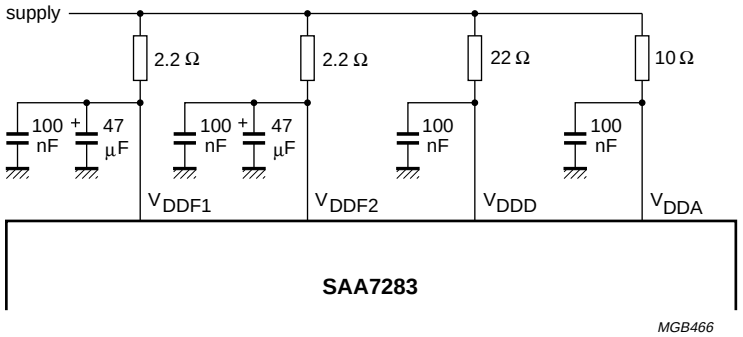


Fig.7 V_{DD} external circuitry.

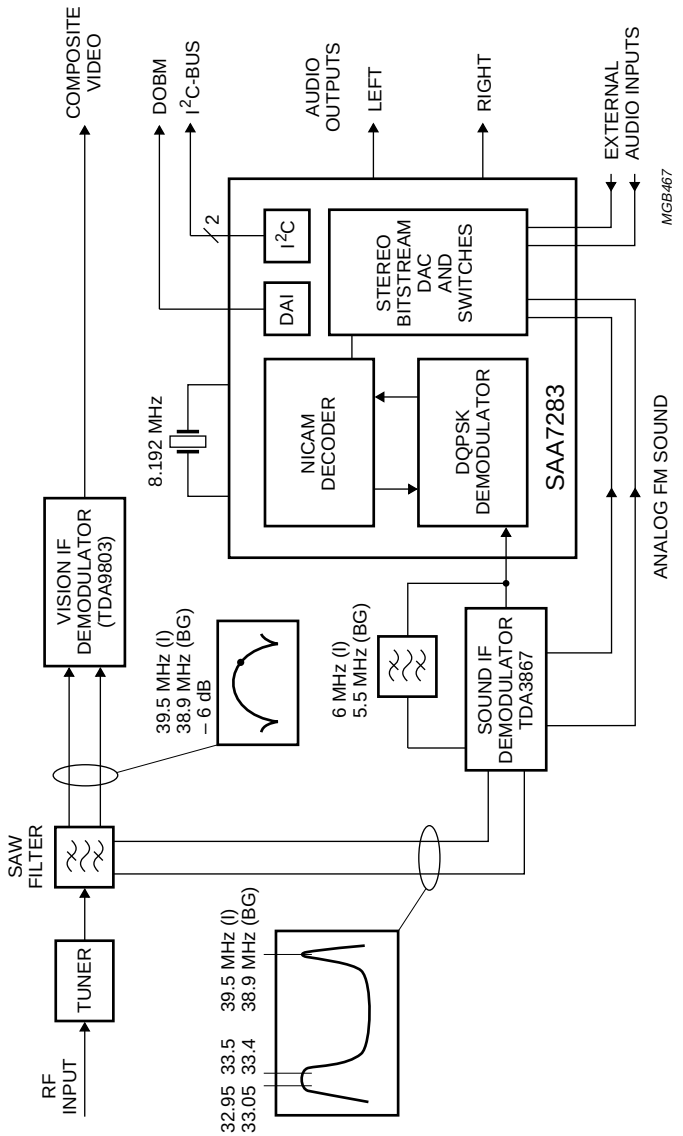


Fig.8 System block diagram showing SAA7283.

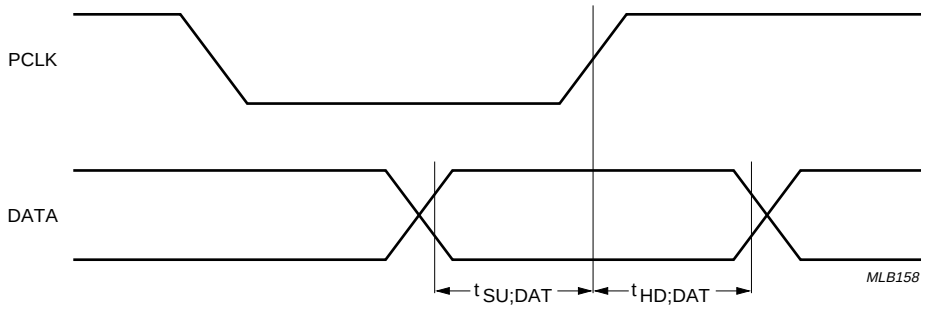


Fig.9 Data output timing.

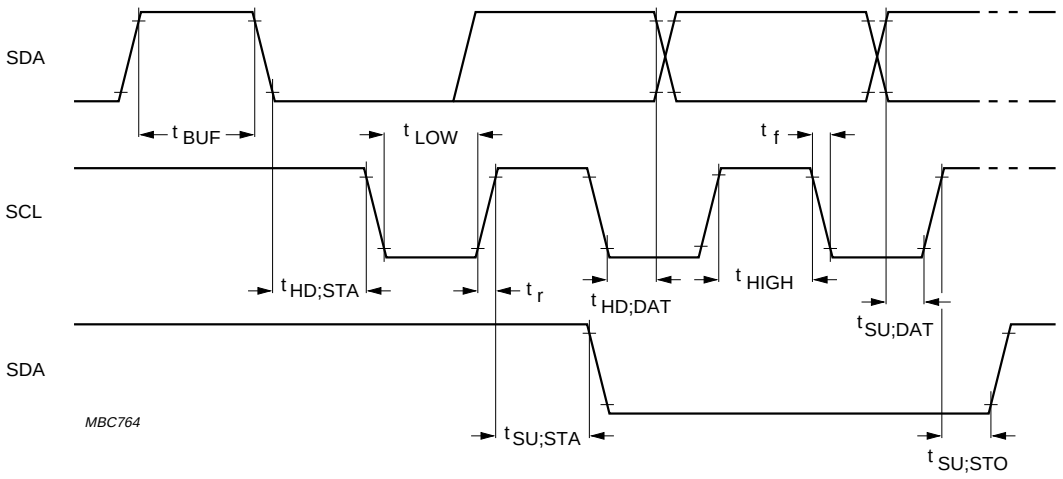


Fig.10 I^2C-bus timing.

APPLICATION INFORMATION

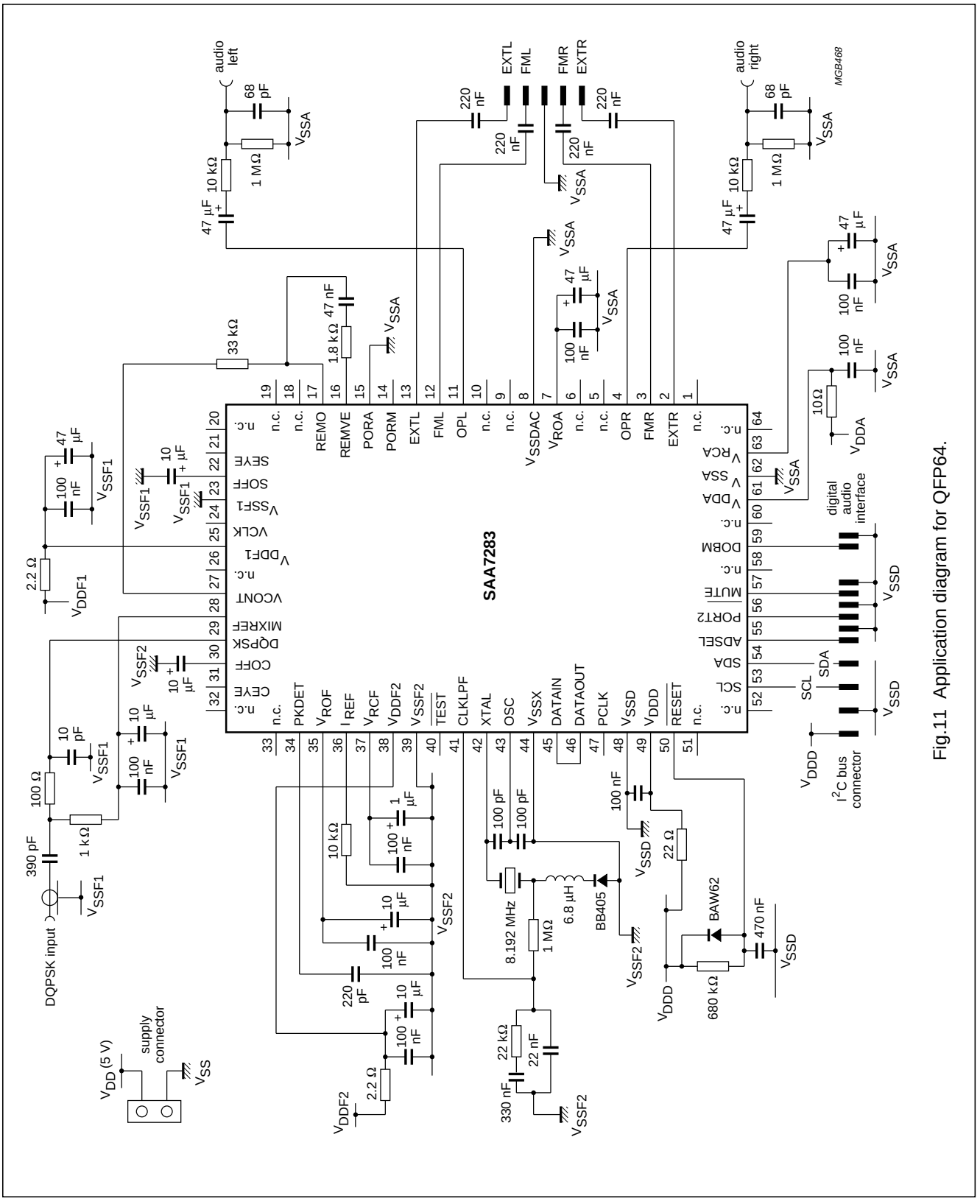
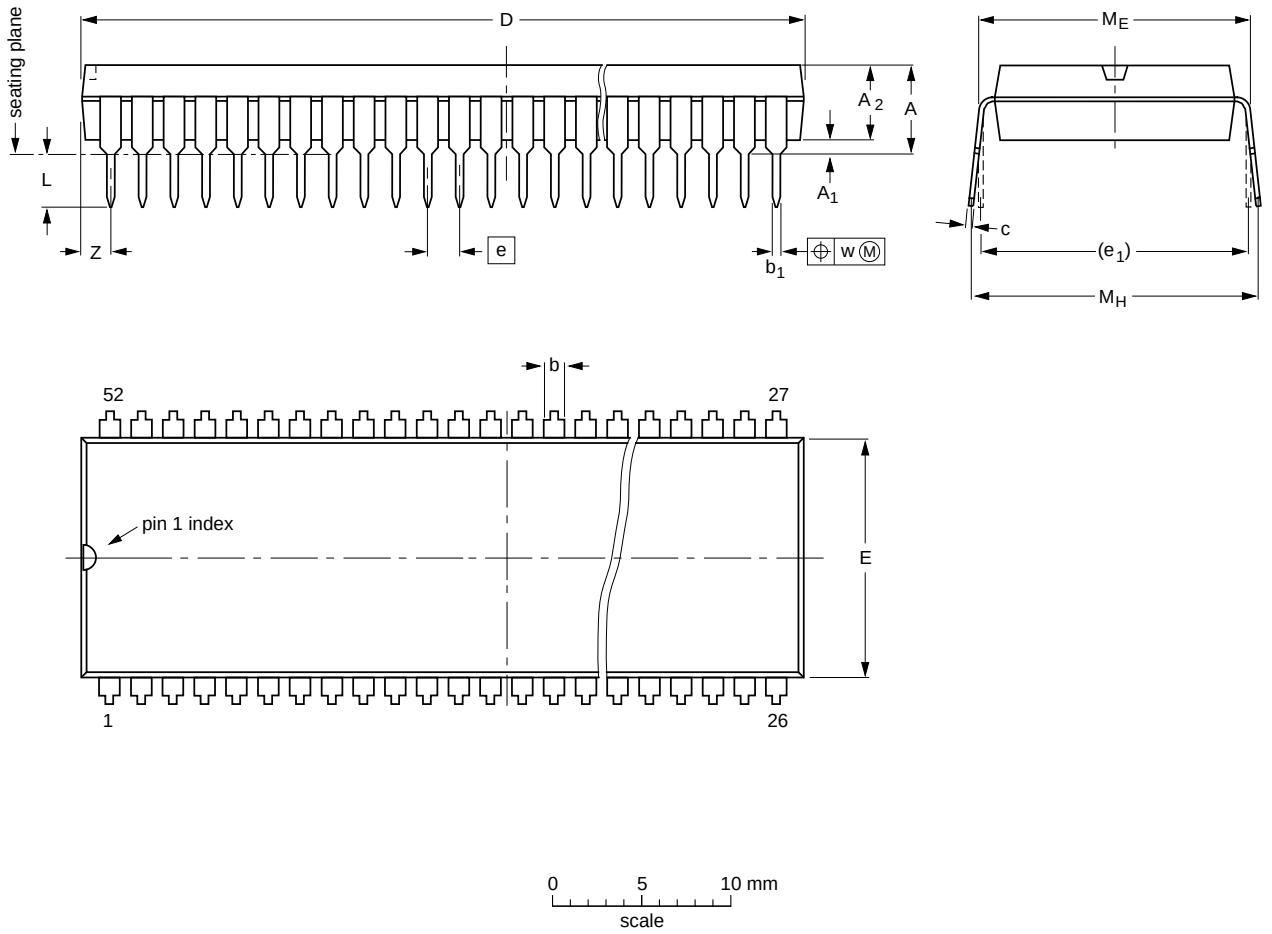


Fig.11 Application diagram for QFP64.

PACKAGE OUTLINES

SDIP52: plastic shrink dual in-line package; 52 leads (600 mil) **SOT247-1**



DIMENSIONS (mm are the original dimensions)

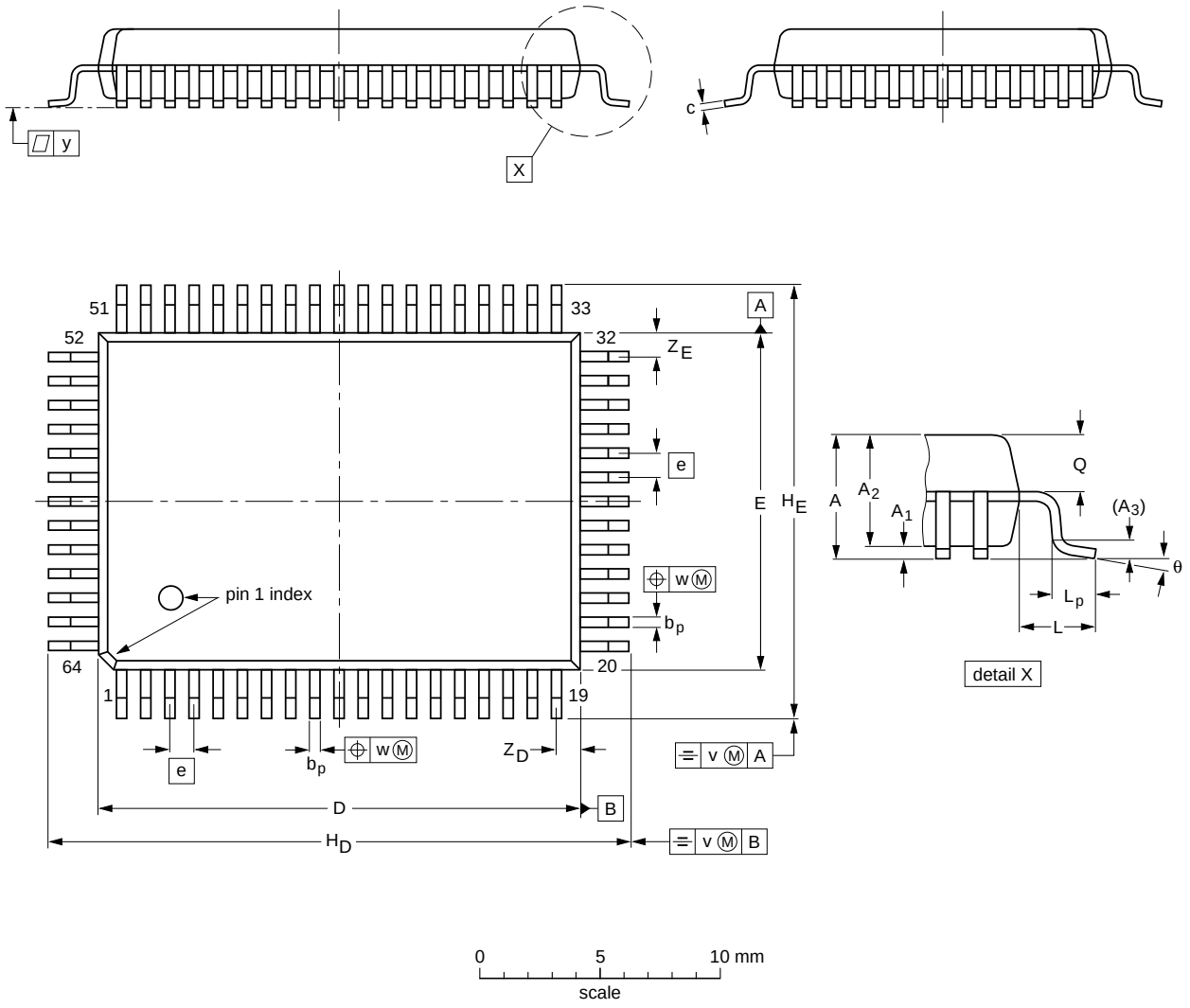
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	47.9 47.1	14.0 13.7	1.778	15.24	3.2 2.8	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT247-1						~~90-01-22~~ 95-03-11

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT319-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

SDIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

QFP

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary from 50 to 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheat for 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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