CSD16570Q5B 25V N 通道 NexFET™功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 极低电阻
- 低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- SON 5mm × 6mm 塑料封装

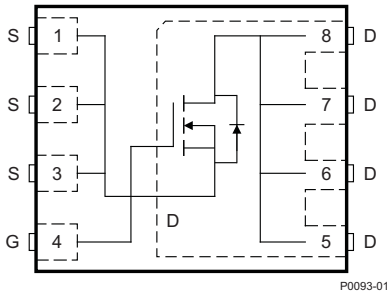
2 应用范围

- ORing 和热插拔 应用

3 说明

这款 25V，0.49mΩ，SON 5mm × 6mm NexFET™功率 MOSFET 旨在最大限度地减小 ORing 和热拔插应用的 电阻， 不适用于开关 应用。

顶部图标



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	25		V
Q_g	栅极电荷总量 (4.5V)	95		nC
Q_{gd}	栅极电荷（栅极到漏极）	31		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V	0.68	mΩ
		V_{GS} = 10V	0.49	mΩ
$V_{GS(th)}$	阈值电压	1.5		V

订购信息(1)

器件	数量	介质	封装	出货
CSD16570Q5B	2500	13 英寸卷带	SON 5mm x 6mm 塑料封装	卷带封装
CSD16570Q5BT	250	7 英寸卷带		

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

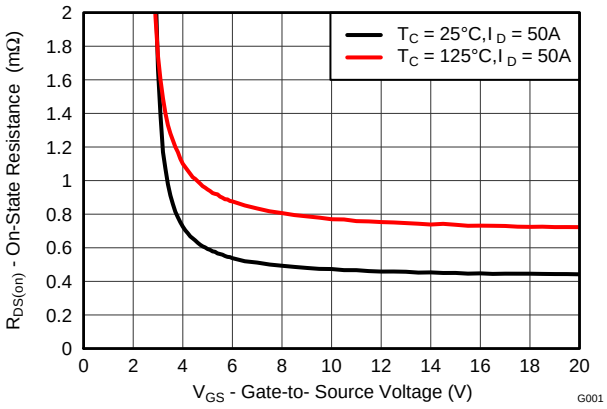
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	25	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	100	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	456	
	持续漏极电流(1)	59	
I_{DM}	脉冲漏极电流(2)	400	A
P_D	功率耗散(1)	3.2	W
	功率耗散，T_C = 25°C	195	
T_J，T_{stg}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 98A，L = 0.1mH，R_G = 25Ω	480	mJ

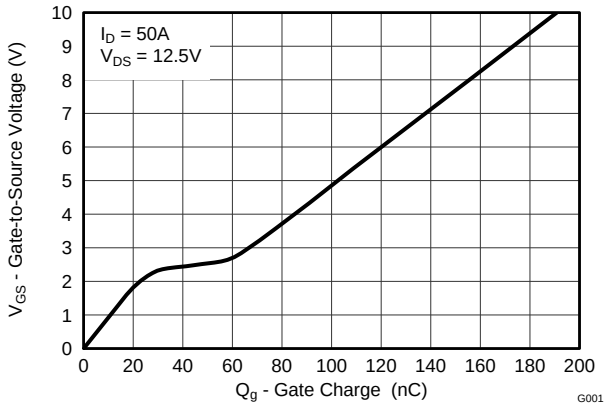
(1) $R_{\theta JA}$= 40°C/W，这是在一个厚度 0.06 英寸的环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸^2，2 盎司的铜焊盘上测得的典型值
。

(2) 最大 $R_{\theta JC}$ = 0.8°C/W，脉冲持续时间 ≤ 100µs，占空比 ≤ 1%

$R_{DS(on)}$ 与 V_{GS} 对比



栅极电荷



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

Changes from Original (July 2014) to Revision A **Page**

- 已添加 将*接收文档更新通知* 和*社区资源* 部分添加到了*器件和文档支持*。 7
- 已更改 在*建议 PCB 布局* 部分方框图中将焊盘 3 和 4 之间的尺寸从 0.028 英寸更改为了 0.050 英寸 9

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5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 μA	25			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 20 V			1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.1	1.5	1.9	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V, I_D = 50 A		0.68	0.82	mΩ
		V_{GS} = 10 V, I_D = 50 A		0.49	0.59	mΩ
g_{fs}	Transconductance	V_{DS} = 2.5 V, I_D = 50 A		278		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 12 V, f = 1 MHz		10700	14000	pF
C_{oss}	Output Capacitance			1660	2160	pF
C_{rss}	Reverse Transfer Capacitance			996	1290	pF
R_G	Series Gate Resistance			1.8	3.6	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 12.5 V, I_D = 50 A		95	124	nC
Q_g	Gate Charge Total (10 V)			192	250	nC
Q_{gd}	Gate Charge Gate-to-Drain			31		nC
Q_{gs}	Gate Charge Gate-to-Source			29		nC
$Q_{g(th)}$	Gate Charge at V_{th}			15		nC
Q_{oss}	Output Charge	V_{DS} = 12.5 V, V_{GS} = 0 V		35		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5 V, V_{GS} = 10 V, I_{DS} = 50 A, R_G = 0 Ω		5		ns
t_r	Rise Time			43		ns
$t_{d(off)}$	Turn Off Delay Time			156		ns
t_f	Fall Time			72		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 50 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 12.5 V, I_F = 50 A, di/dt = 300A/μs		34		nC
t_{rr}	Reverse Recovery Time			21		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance(1)			0.8	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)(2)			50	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches × 1.5-inches (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.

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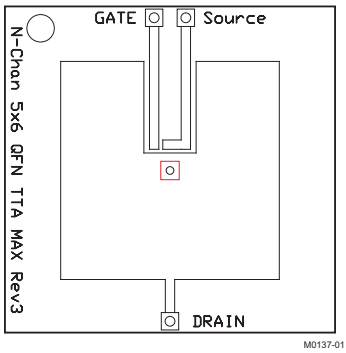
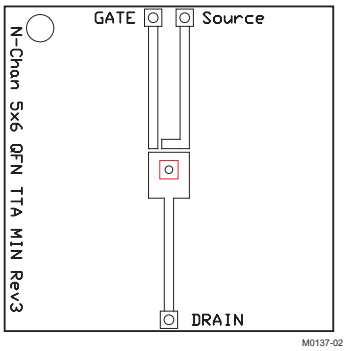


Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

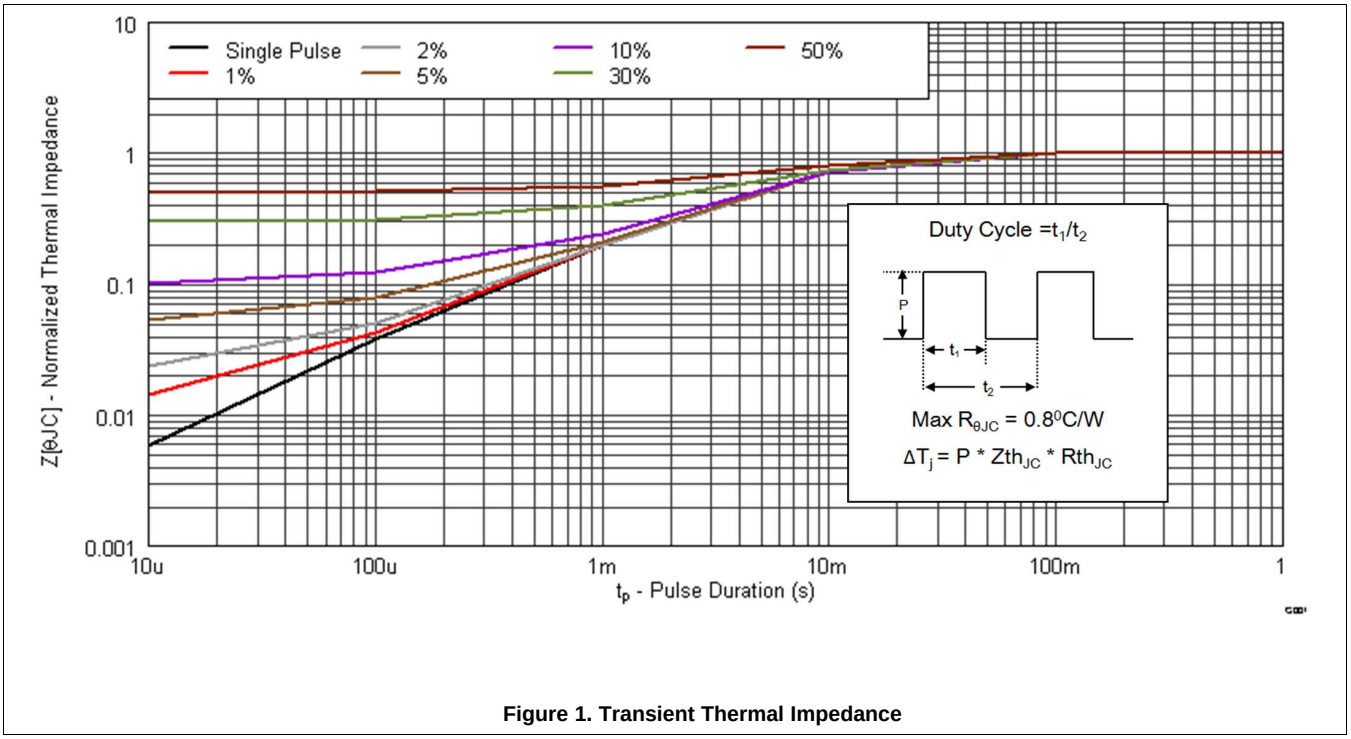


Figure 1. Transient Thermal Impedance

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

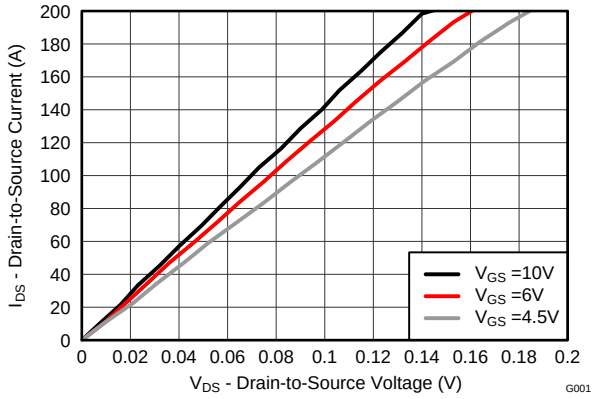

Figure 2. Saturation Characteristics

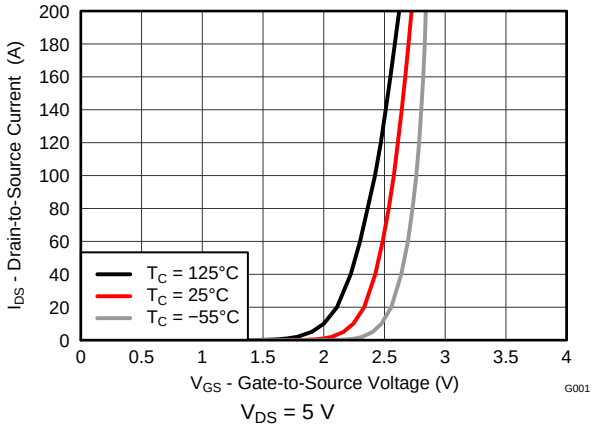

Figure 3. Transfer Characteristics

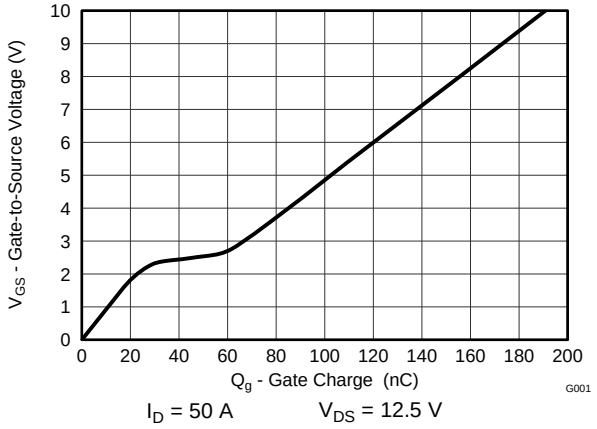

Figure 4. Gate Charge

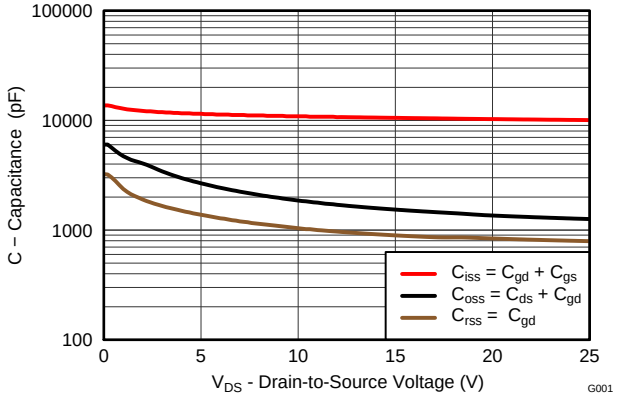

Figure 5. Capacitance

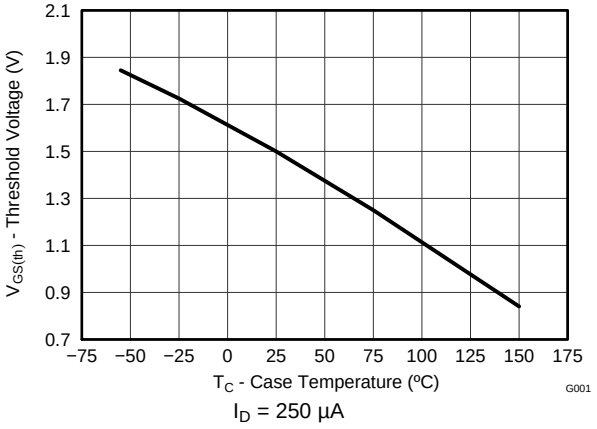

Figure 6. Threshold Voltage vs Temperature

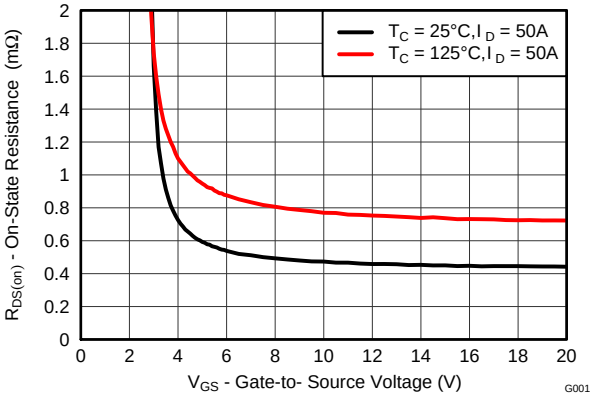

Figure 7. On-State Resistance vs Gate-to-Source Voltage

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

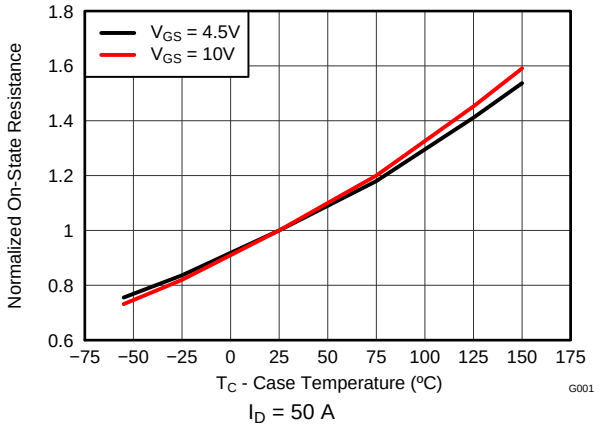

Figure 8. Normalized On-State Resistance vs Temperature

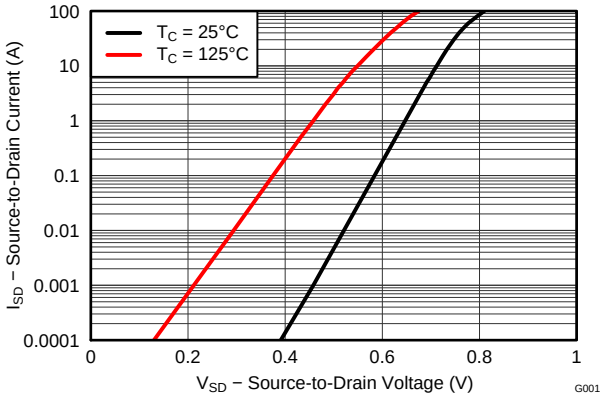

Figure 9. Typical Diode Forward Voltage

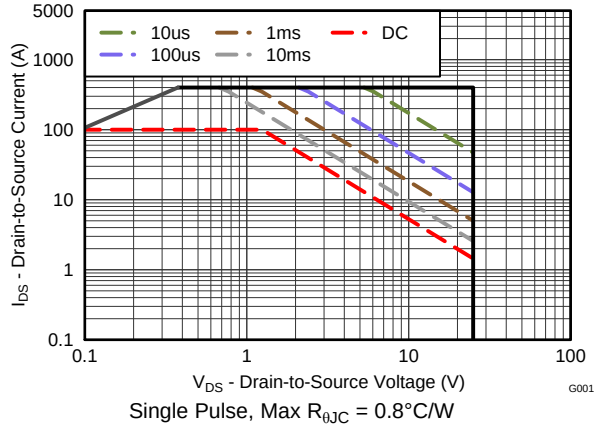

Figure 10. Maximum Safe Operating Area

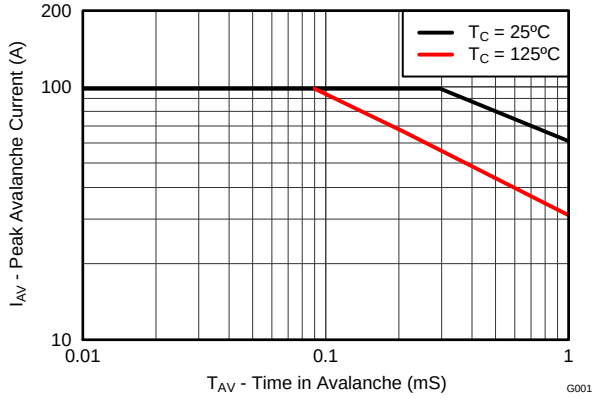

Figure 11. Single Pulse Unclamped Inductive Switching

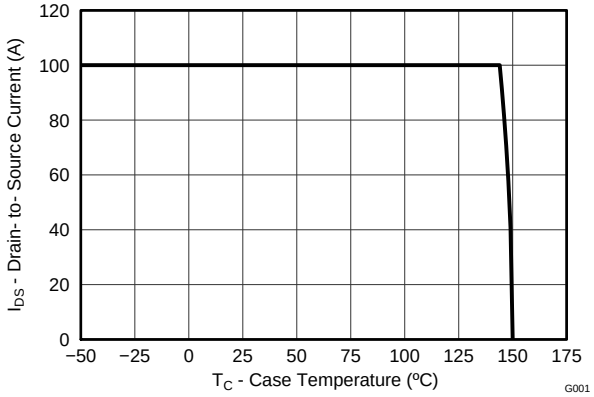

Figure 12. Maximum Drain Current vs Temperature

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6 器件和文档支持

6.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的*通知我*进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

6.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 商标

NexFET, E2E are trademarks of Texas Instruments.

6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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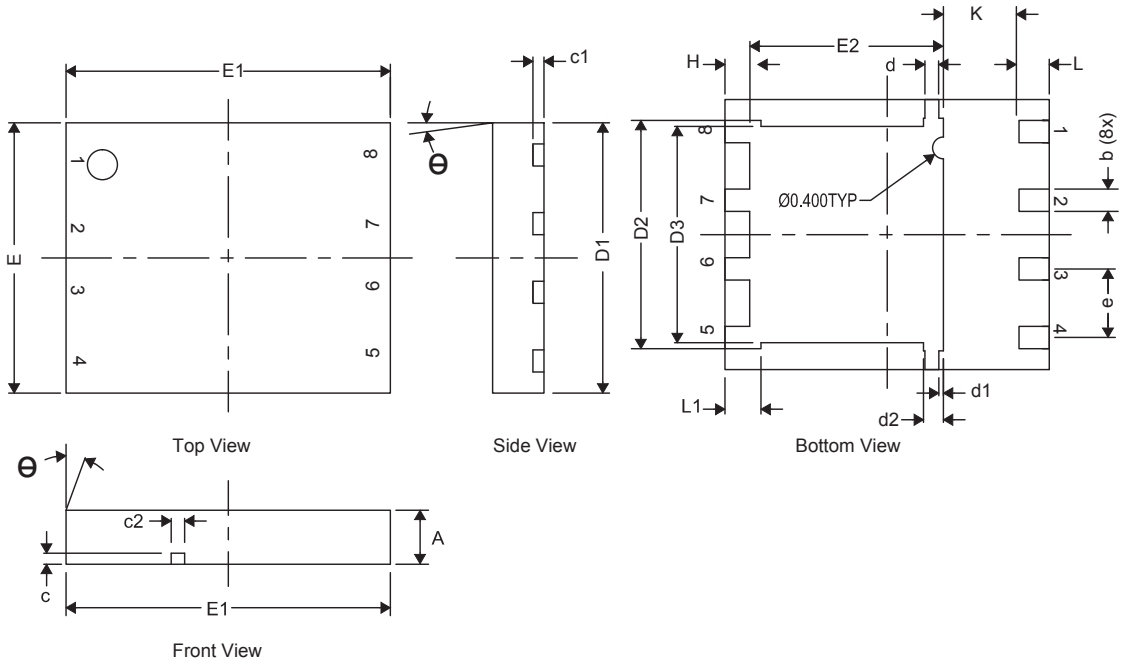
7 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

7.1 Q5B 封装尺寸



DIM	毫米		
	最小值	标称值	最大值
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 典型值		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 典型值		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	—	—
K	1.40 典型值		

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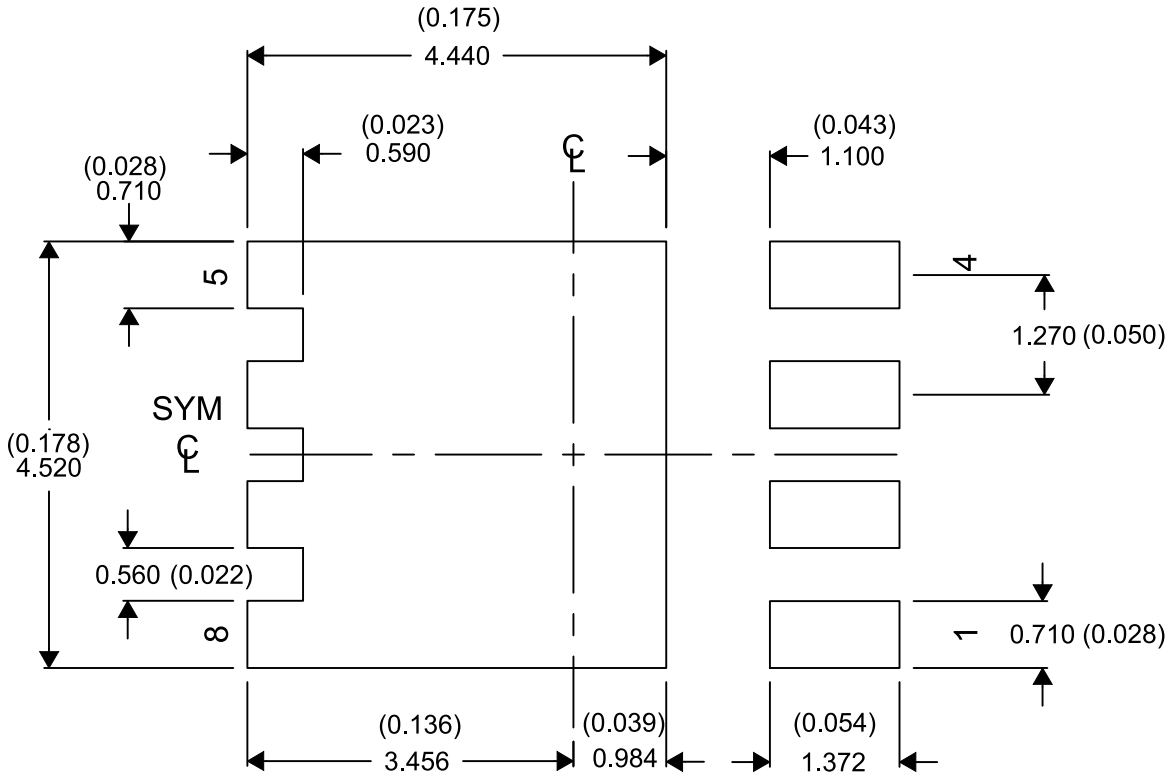
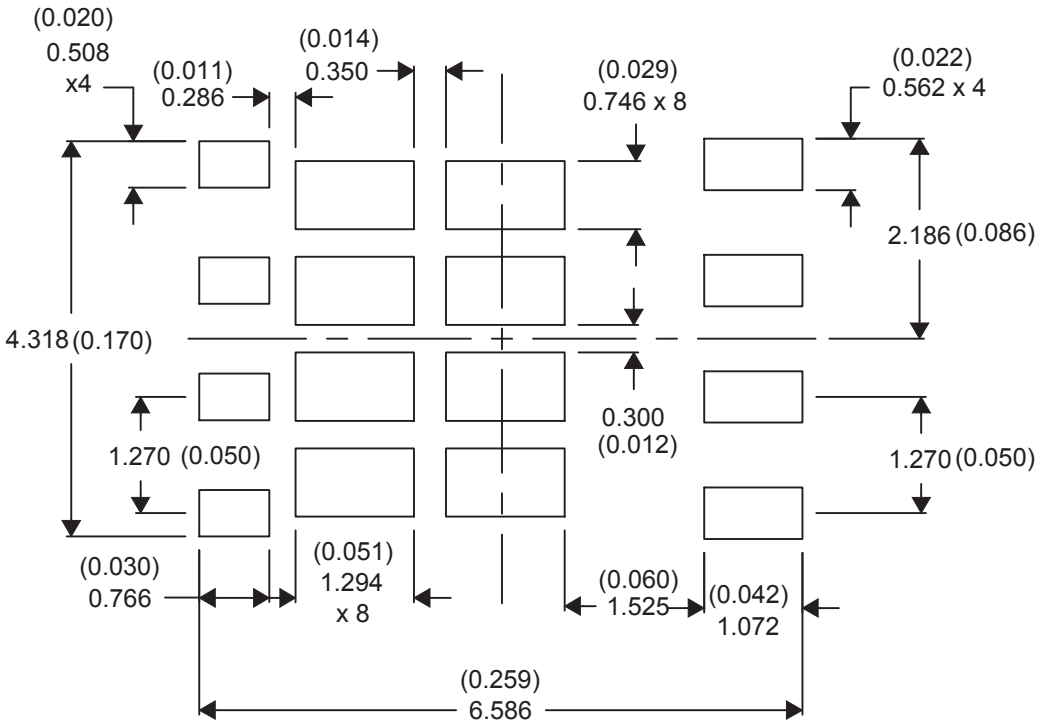
7.2 建议 PCB 布局

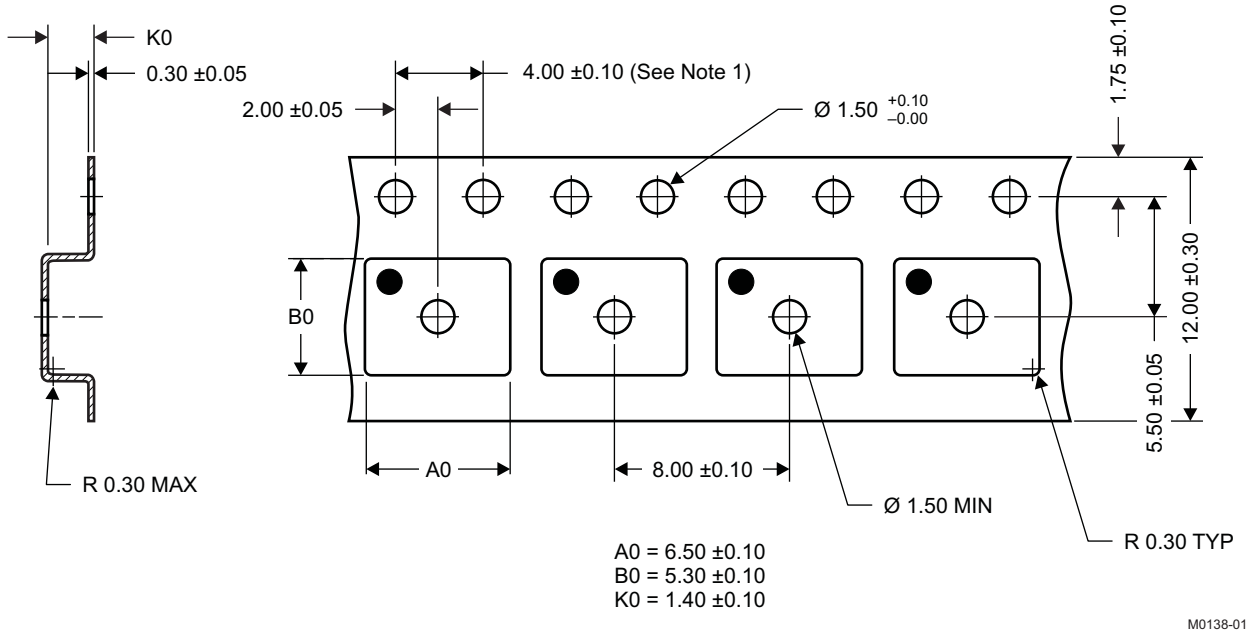


要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线，请参见《应用说明》SLPA005 - *通过 PCB 布局布线技巧来减少振铃*。

7.3 建议模板布局



7.4 Q5B 卷带信息



注释：

1. 10 个链齿孔的累积容差为 ±0.2
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积
3. 材料：黑色抗静电聚苯乙烯
4. 全部尺寸单位为 mm（除非另外注明）。
5. 高于孔眼底部 0.3mm 的平面上测量得到 A0 和 B0 值.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16570Q5B	ACTIVE	VSON-CLIP	DNK	8	2500	RoHS-Exempt & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	CSD16570	Samples
CSD16570Q5BT	ACTIVE	VSON-CLIP	DNK	8	250	RoHS-Exempt & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	CSD16570	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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