Preliminary Information [1] *(See Last Page)*

Single-Channel Supply Voltage Marginer/Monitor

FEATURES

- **Capable of margining supplies with trim inputs using either positive or negative trim pin control**
- **Wide Margin range from 0.3V to VDD using internal reference**
- **10-bit ADC readout of supply voltage over I^2C bus**
- **Margining Controlled Via:**
  - **I^2C Command**
  - **Input Pins (M_{UP}, M_{DN})**
- **Two programmable general purpose sensor inputs (COMP1/2) – UV/OV with FAULT Output**
- **Programmable glitch filter (COMP1/2)**
- **Programmable internal VREF, 0.5V or 1.25V**
- **Operates from 2.7V to 5.5V supply**
- **General Purpose 256-Byte EEPROM with Write Protect**
- **I^2C 2-wire serial bus for programming configuration and monitoring status**
- **28 lead QFN**
- **20 ball *Ultra* CSP™ (Chip-Scale) package**

Applications

- **In-system test and control of Point-of-Load (POL) Power Supplies for Multi-voltage Processors, DSPs and ASICs**
- **Routers, Servers, Storage Area Networks**

INTRODUCTION

The SMM150 is a highly accurate power supply voltage supervisor and environmental monitor with provisions for voltage margining of the monitored supply. The part includes an internal voltage reference to accurately monitor and margin the supply to within ±1%. The SMM150 has the capability to margin over a wide range from 0.3V to VDD using the internal reference and can read the value of the supply over the I^2C bus using an on-chip 10-bit ADC. The monitor and margin levels are set using the I^2C serial bus. The SMM150 initiates margining via the I^2C bus or by using the M_{UP} or M_{DN} inputs. Once the pre-programmed margin target voltage is reached, the SMM150 holds the converter at this voltage until receiving an I^2C command or de-asserting the margin input pin. When the SMM150 is not margining, the TRIM output pin is held in a high impedance state allowing the converter to operate at its nominal set point. Two general purpose input pins are provided for sensing under or overvoltage conditions. A programmable glitch filter associated with these inputs allows the user to ignore spurious noise signals. A FAULT# pin is asserted once either input set point is exceeded.

Using the I^2C interface, a host system can communicate with the SMM150 status register and utilize 256-bytes of nonvolatile memory.

SIMPLIFIED APPLICATIONS DRAWING

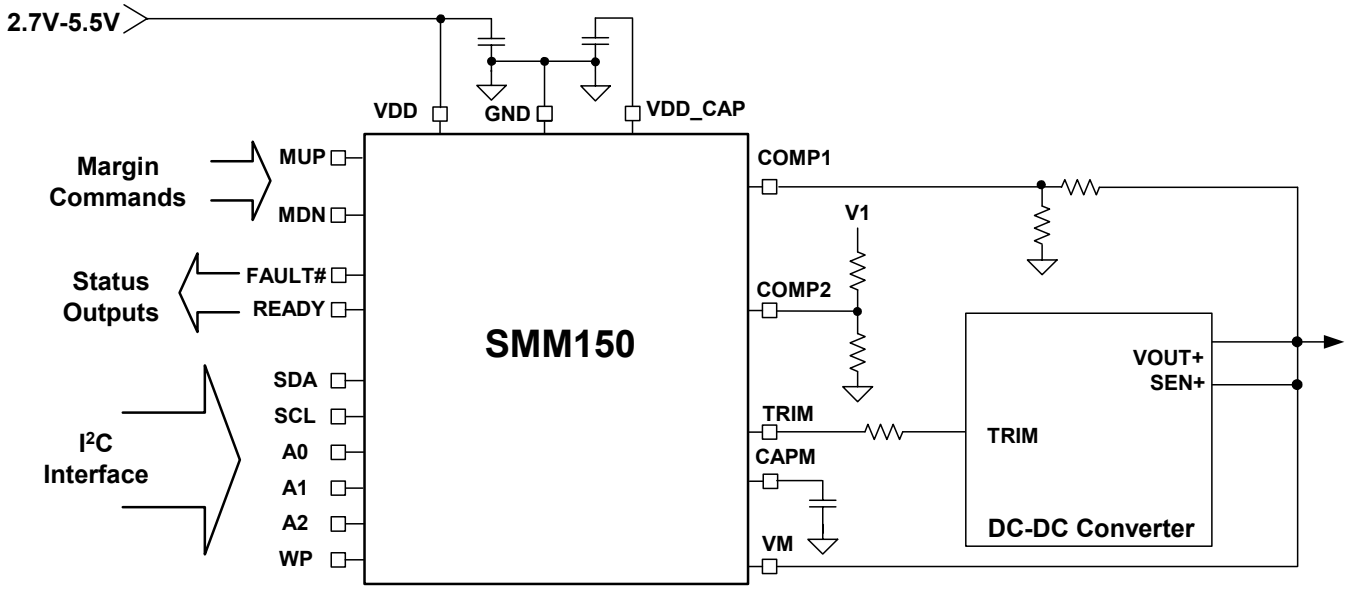


Figure 1 – Applications using the SMM150 Controller to control the Voltage Margining of a DC/DC Converter.

Note: This is an applications example only. Some components and values are not shown.

GENERAL DESCRIPTION

The SMM150 is capable of margining the DC output voltage of LDOs or DC/DC converters that use a trim/adjust pin. The Margin function is programmable over a standard 2-wire I^2C serial data interface and is used to set the margin low/high DC output voltages.

In margining mode the user communicates with the SMM150 via the I^2C serial data bus to select the desired values for margining. This allows the part to margin the supplies up or down to these set values either through asserting the MUP and MDN pins or by writing to the margin register directly. The margin high and margin low voltage settings can range from 0.3V to VDD around the converter's nominal output voltage setting depending on the specified margin range of the DC-DC converter and/or system components, usually ±10%.

When the SMM150 receives the command to margin, the TRIM output will begin adjusting the supply to the selected margin voltage. This is accomplished by incrementing (or decrementing) an internal counter based on the digital comparison between the voltage margin target value and that read by the ADC from the VM input. This operation is repeated until the 2 values are equal, after which the SMM150 holds the TRIM output pin at the voltage required to maintain the margin setting. An I^2C command or de-assertion of the MUP/MDN pin will return the TRIM output pin to a high impedance state thus allowing the converter to return to its nominal operating voltage.

The SMM150 has two additional input pins and one additional output pin. The input pins, COMP1 and COMP2, are high impedance inputs, each connected to a comparator and compared against the internal reference (VREF, 0.5V or 1.25V). Each comparator can be independently programmed to monitor for UV or OV. When either of the COMP1 or COMP2 inputs are in fault the open-drain FAULT# output will be pulled low. A configuration option exists to disable the FAULT# output during margining.

Programming of the SMM150 is performed over the industry standard I^2C 2-wire serial data interface. A status register is available to read the state of the part and a Write Protect (WP) pin is available to prevent writing to the configuration registers and EE memory.

INTERNAL BLOCK DIAGRAM

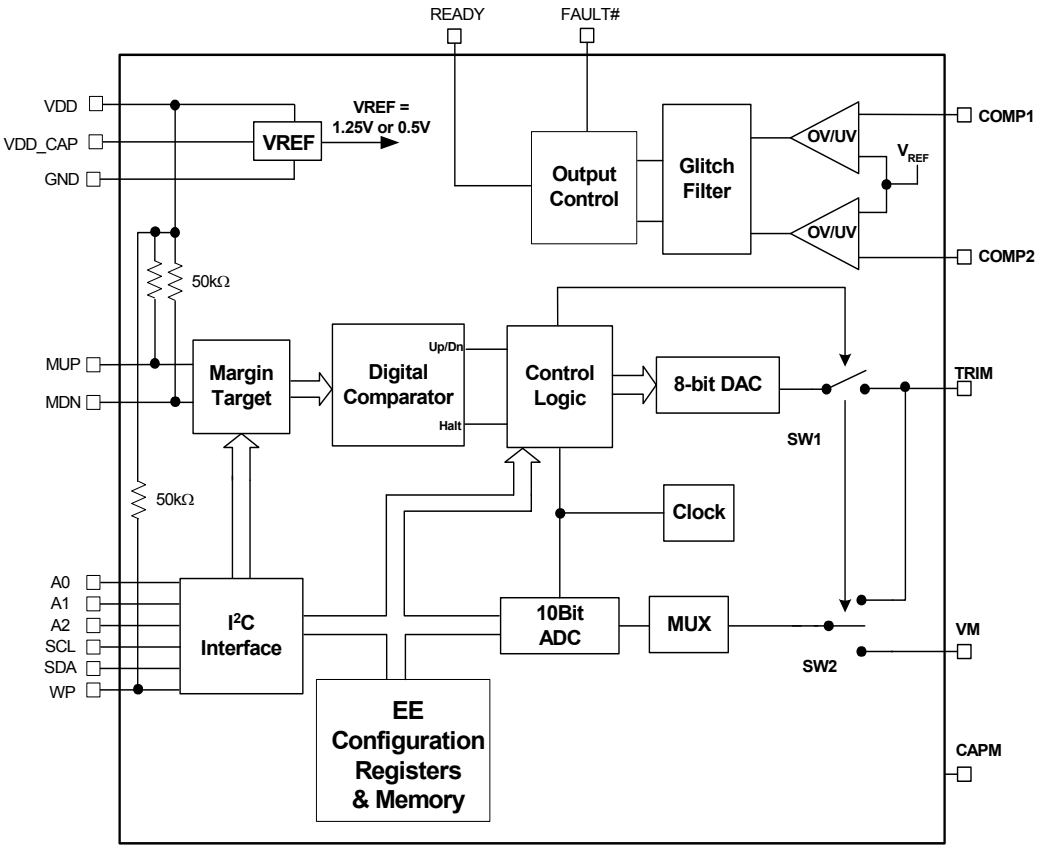
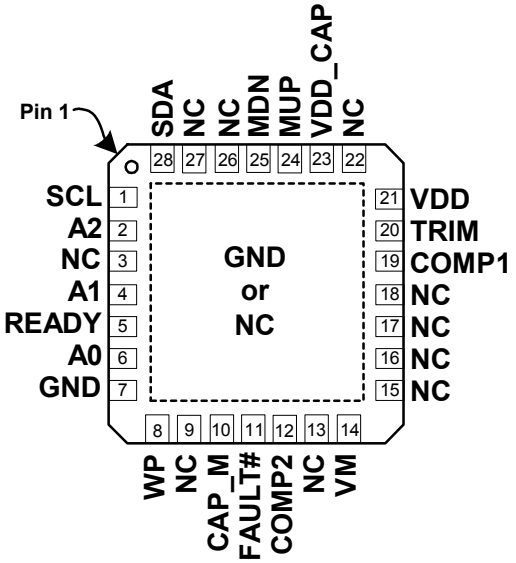


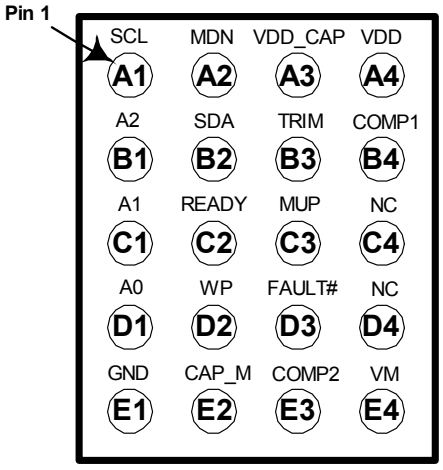
Figure 2 – SMM150 Controller Internal Block Diagram.

PACKAGE AND PIN CONFIGURATION

28 Pad QFN
Top View



20 Ball *Ultra* CSP™
Bottom View



PIN DESCRIPTIONS

QFN Pad Number	*Ultra* CSP™ Ball Number	Pin Type	Pin Name	Pin Description
28	B2	I/O	**SDA**	I^2C Bi-directional data line
1	A1	I	**SCL**	I^2C clock input.
2	B1	I	**A2**	The address pins are biased either to VDD, GND or left floating. This allows for a total of 21 distinct device addresses. When communicating with the SMM150 over the 2-wire bus these pins provide a mechanism for assigning a unique bus address.
4	C1	I	**A1**	
6	D1	I	**A0**	
8	D2	I	**WP**	Programmable Write Protect active high/low input. When asserted, writes to the configuration registers and general purpose EE are not allowed. The WP input is internally tied to VDD with a 50KΩ resistor.
10	E2	CAP	**CAPM**	External capacitor input used to filter the VM input, 0.2μF.
20	B3	O	**TRIM**	Output voltage used to control and/or margin converter voltages. Connect to the converter trim input.
14	E4	I	**VM**	Voltage monitor input. Connect to the DC-DC converter positive sense line or its' +Vout pin.
21	A4	PWR	**VDD**	Power supply of the part.
23	A3	PWR	**VDD_CAP**	External capacitor input used to filter the internal VDD supply rail.
7	E1	GND	**GND**	Ground of the part. The SMM150 ground pin should be connected to the ground of the device under control or to a star point ground. PCB layout should take into consideration ground drops.
24	C3	I	**MUP**	Margin up command input. Asserted high. The MUP input is internally tied to VDD with a 50KΩ resistor.
25	A2	I	**MDN**	Margin down command input. Asserted high. The MDN input is internally tied to VDD with a 50KΩ resistor.
19	B4	I	**COMP1**	COMP1 and COMP2 are high impedance inputs, each connected internally to a comparator and compared against the internally programmable VREF voltage. Each comparator can be independently programmed to monitor for UV or OV. The monitor level is set externally with a resistive voltage divider.
12	E3	I	**COMP2**	
11	D3	O	**FAULT#**	When either of the COMP1 or COMP2 inputs are in fault the open-drain FAULT# output will be pulled low. A configuration option exists to disable the FAULT# output while the device is margining.
5	C2	I/O	**READY**	Programmable active high/low open drain output indicates that VM is at its set point. When programmed as an active high output, READY can also be used as an input. When pulled low, it will latch the state of the comparator inputs.
3, 9, 13, 15-18, 22, 26, 27, 29	C4, D4	NC	**NC**	No Connect. The bottom side metal plate (Pad 29) can be connected to GND or left floating.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to 125°C
Storage Temperature QFN ..... -65°C to 150°C
Terminal Voltage with Respect to GND:
VDD Supply Voltage .....-0.3V to 6.0V
All Others .....-0.3V to V_{DD} + 0.7V
FAULT#..... GND to 15.0V
Output Short Circuit Current 100mA
Reflow Solder Temperature (10 secs).....240°C
Junction Temperature.....150°C
ESD Rating per JEDEC.....2000V
Latch-Up testing per JEDEC.....±100mA

Note - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

RECOMMENDED OPERATING CONDITIONS

Temperature Range (Industrial) .....–40°C to +85°C
(Commercial)..... 0°C to +70°C
VDD Supply Voltage..... 2.7V to 5.5V
Inputs.....GND to VDD

Package Thermal Resistance (θ_{JA})
28 Pad QFN.....80°C/W
20 Ball *Ultra* CSP™.....TBD°C/W

Moisture Classification Level 1 (MSL 1) per J-STD- 020

RELIABILITY CHARACTERISTICS
Data Retention.....100 Years
Endurance.....100,000 Cycles

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
VDD	Supply Voltage		2.7	3.3	5.5	V
VM	Positive Sense Voltage	VM pin	0.3		VDD	V
I_{DD}	Power Supply Current from VDD	TRIM pin floating		3		mA
I_{TRIM}	TRIM output current through 100Ω to 1.0V	TRIM Sourcing Max Current		1.5		mA
		TRIM Sinking Max Current		-1.5		mA
V_{TRIM}	TRIM output voltage range	I_{TRIM} ±1.5mA	GND		2.5	V
V_{ADOC}	Margin Range	Depends on Trim range of DC-DC Converter	0.3		VDD	V
V_{IH}	Input High Voltage SDA,SCL,WP,MUP,MDN	VDD = 2.7V	0.9xVDD		VDD	V
		VDD = 5.0V	0.7xVDD		VDD	
V_{IL}	Input Low Voltage SDA,SCL,WP,MUP,MDN	VDD = 2.7V			0.1xVDD	V
		VDD = 5.0V			0.3xVDD	
V_{OL}	Open Drain Output FAULT#, READY	ISINK = 1mA		0.2		V
V_{AIH}	Address Input High Voltage, A2, A1, A0	VDD = 2.7V, R_{pullup}≤300kΩ	0.9xVDD		VDD	V
		VDD = 5.0V, R_{pullup}≤300kΩ	0.7xVDD		VDD	
V_{AIL}	Address Input Low Voltage, A2, A1, A0	VDD = 2.7V, $R_{pulldown}$≤300kΩ			0.1xVDD	V
		VDD = 5.0V, $R_{pulldown}$≤300kΩ			0.3xVDD	
I_{AIT}	Address Input Tristate Maximum Leakage – High Z	VDD = 2.7V	-1.8		+1.4	µA
		VDD = 5.0V	-2.0		+1.6	
OV/UV	Monitor Voltage Range	COMP1 and COMP2 pins	0		VDD	V
V_{HYST}	COMP1/2 DC Hysteresis	COMP1 and COMP2 pins, V_{TH}-V_{TL} (see Note 1)		10		mV
$R_{Pull-Up}$	Input Pull-Up Resistors	See Pin Descriptions		50		kΩ

Note 1 – The Base DC Hysteresis voltage is measured with a 1.25V external voltage source. The resulting value is determined by subtracting Threshold Low from Threshold High, V_{TH}-V_{TL} while monitoring the FAULT# pin state. Base DC Hysteresis is measured with a 1.25V input. Actual DC Hysteresis is derived from the equation: (V_{IN}/V_{REF})(Base Hysteresis). For example, if V_{IN}=2.5V and V_{REF}=1.25V then Actual DC Hysteresis= (2.5V/1.25V)(0.003V)=6mV.

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
VREF	VREF Internal Reference	VREF=1.25V	1.24	1.25	1.26	V
		VREF=0.5V	0.496	0.500	0.504	
$MARG_{ACC}$	Margin Accuracy		-1.0	±0.75	+1.0	%

AC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
t_{ADC_DAC}	Monitor sampling/conversion period	Update period for ADC conversion and DAC update		1.8		ms
$t_{MARG_I/D}$	Margin single bit increment or decrement time	T_{MARG_UPDATE} = (X)(1.8ms) where: X=step number of possible 256 and 1 step=5mV		1.8		ms
t_{GLITCH}	Programmable glitch filter times			0		µs
				15		µs
				40		µs
				120		µs
t_{MARGIN}	Programmable Margin Delay Times	Note 1 – See Figure 4		2.5		ms
				5		ms
				10		ms
				17.5		ms

I²C 2-WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS – 100kHz

Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND. See Figure 3 Timing Diagram.

Symbol	Description	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency		0		100	KHz
t_{LOW}	Clock Low Period		4.7			µs
t_{HIGH}	Clock High Period		4.0			µs
t_{BUF}	Bus Free Time	Before New Transmission - Note 1/	4.7			µs
$t_{SU:STA}$	Start Condition Setup Time		4.7			µs
$t_{HD:STA}$	Start Condition Hold Time		4.0			µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7			µs
t_{AA}	Clock Edge to Data Valid	SCL low to valid SDA (cycle n)	0.2		3.5	µs
t_{DH}	Data Output Hold Time	SCL low (cycle n+1) to SDA change	0.2			µs
t_R	SCL and SDA Rise Time	Note 1/			1000	ns
t_F	SCL and SDA Fall Time	Note 1/			300	ns
$t_{SU:DAT}$	Data In Setup Time		250			ns
$t_{HD:DAT}$	Data In Hold Time		0			ns
TI	Noise Filter SCL and SDA	Noise suppression		100		ns
t_{WR}	Write Cycle Time				5	ms

Note: 1/ - Guaranteed by Design.

TIMING DIAGRAMS

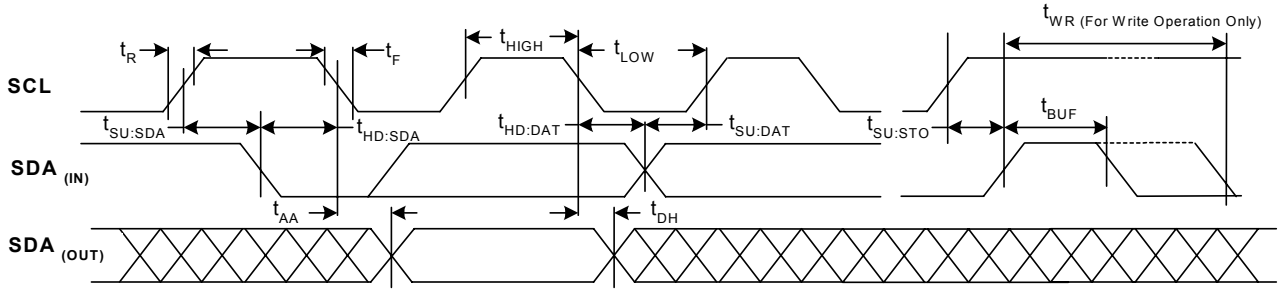


Figure 3. Basic I²C Serial Interface Timing

APPLICATIONS INFORMATION

DEVICE OPERATION

POWER SUPPLY

The SMM150 can be powered by a 2.7V to 5.5V input to the VDD pin (Figure 1). Care should be exercised that noise from the DC/DC converter is filtered from the SMM150 VDD pin. See figure 6 for suggestions.

VOLTAGE REFERENCE

The SMM150 uses an internal voltage reference, VREF with a user programmable level of 0.5V or 1.25V. Total accuracy of VREF is ±0.8% over temperature and supply variations. For DC/DC converters that have output voltages below 1.25V, set the internal VREF to 0.5V.

MODES OF OPERATION

The SMM150 has two basic modes of operation: UV and OV monitoring mode and supply margining mode. A detailed description of each mode and feature follows. A flow diagram is shown in Figure 5.

MARGIN MODE

The SMM150 can control margining of a DC/DC converter that has a trim pin or any regulator having access to its feedback node. The TRIM pin on the SMM150 is connected to the trim input pin on the power supply converter. A sense line from the converter's point-of-load connects to the VM input. The margin function begins upon an I^2C command or assertion of the MUP/MDN pins. The TRIM pin is driven by a DAC whose input is incremented or decremented every 200µS based on the digital comparison of the margin target value and the actual converter output voltage. The voltage on the TRIM output will continue increasing (decreasing) until the converter's output voltage equals the target margin voltage. This voltage adjustment allows the SMM150 to control the margined output voltage of the power supply converter to within ±1.0% in an open-loop manner.

The converter is held at the margin voltage until the SMM150 receives an I^2C command or the respective MUP/MDN pin is de-asserted. When not margining, the TRIM pin on the SMM150 is in a high impedance state. The voltage on the TRIM pin is buffered and applied to the ADC at the beginning of a margin cycle to ensure the converter is margined from its nominal setpoint. This allows a smooth transition from the converter's nominal voltage to the SMM150 controlling that margin voltage to the margin target setting. After margining high, low or nominal, issuing a margin Off command will cause the trim pin to go high impedance. The part margin time from Off to High or Off to Low is specified as a typical according to the equation:

T_{MARG_UPDATE} = (X)(1.8ms) where:

X=step number of possible 256 and 1 step=5mV

The Active Margin Command Delay Time using the MUP and MDN pins is shown in Figure 4

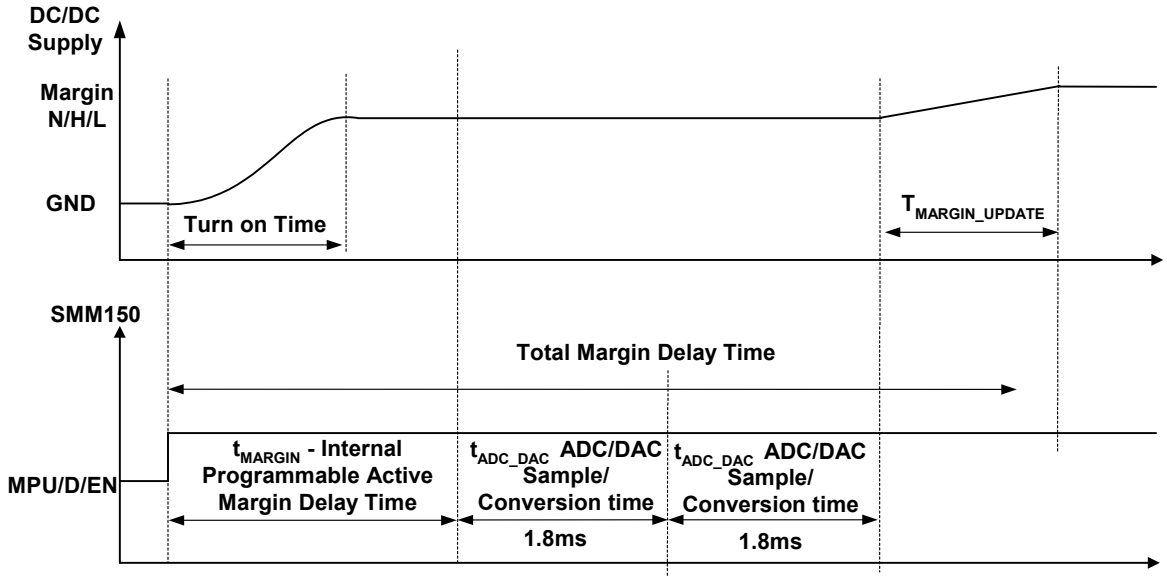


Figure 4 – Margin Delay Time

APPLICATIONS INFORMATION (CONTINUED)

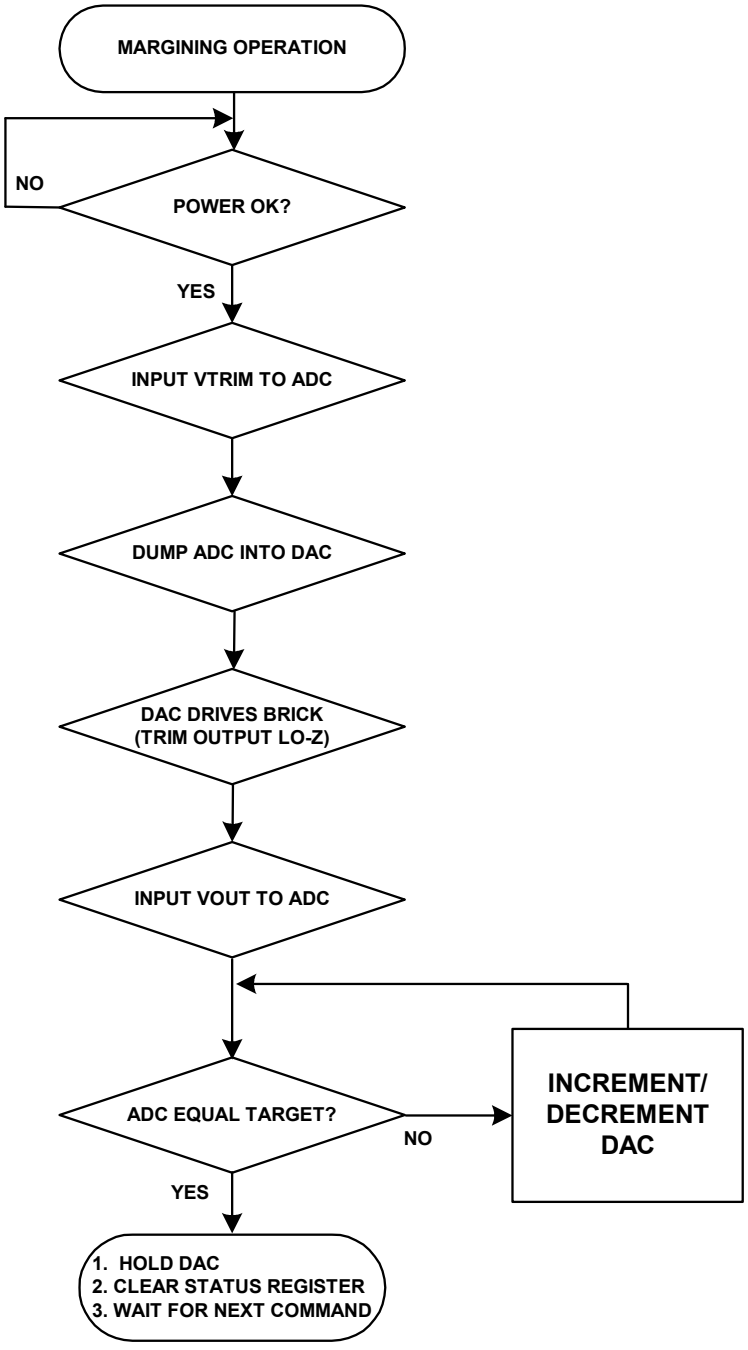


Figure 5 - SMM150 Margin Flow Chart

APPLICATIONS INFORMATION (CONTINUED)

When measuring the delay time external to the device, ADC sample time and Update Trim time (≅ 4ms) must be added to the internally programmed delay time as shown:

Spec	Actual measurement
2.5 ms	6.5 ms
5 ms	9 ms
10 ms	14 ms
17.5 ms	22 ms

MONITOR

The SMM150 monitors the COMP1 and COMP2 pins. COMP1 and COMP2 are high impedance inputs, each connected internally to a comparator and compared against the programmable internal reference voltage. Each comparator can be independently programmed to monitor for either UV or OV. The monitor level is set externally with a resistive voltage divider. The COMP pins can be connected to Vin, Vout or any voltage that needs to be monitored. The internal comparators COMP1/2 are compared to VREF, so the voltage dividers are set above or below the programmed VREF level depending on whether monitoring UV or OV. As an example, with VREF set to 1.25V, to monitor an OV of 1.7V on COMP1 and a UV of 1.3V on COMP2, the voltage divider resistors are:

For OV, RUpper = 1.37k, 1% RLower = 3.83k, 1%.

For UV, RUpper = 1.02k, 1% RLower = 25.5k, 1%.

The part can be programmed to trigger the FAULT# pin when either COMPx comparator has exceeded the UV or OV range. The READY and FAULT# outputs of the SMM150 are active as long as the triggering limit remains in a fault condition. The READY pin is programmable active high/low open drain output indicates that VM is at its' set point.

When programmed as an active high output, READY can also be used as an input. When pulled low, it will latch the state of the comparator inputs. When either of the COMP1 or COMP2 inputs are in fault, the open-drain FAULT# output will be pulled low. A configuration option exists to disable the FAULT# output while the device is in margining mode.

STATUS REGISTER

A status register exists for I^2C polling of the status of the COMP1 and COMP2 inputs. Two bits in this status register reflect the current state of the inputs (1 = fault, 0 = no fault). Two additional bits show the state of the inputs latched by one of two events programmed in the configuration.

The first event option is the FAULT# output going active. The second event option is the READY pin going low. The READY pin is an I/O. As an output, the READY output pin goes active when the DC controlled voltages are at their set point. As an input programmed to active high, it can be pulled low externally and latch the state of the COMP inputs. This second event option allows the state of the COMP inputs on multiple devices to be latched at the same time while a host monitors their FAULT# outputs.

MARGINING

The SMM150 has two additional control voltage settings: margin high and margin low. The margin high and margin low settings can be as much as ±10% of the nominal setting depending on the manufacturer. The margin high and margin low voltage settings can range from 0.3V to VDD around the converters' nominal output voltage setting depending on the specified margin range of the DC-DC converter. These settings are stored in the configuration registers and are loaded into the control voltage setting by margin commands issued via the I^2C bus.

The margin command registers contain two bits that decode the commands to margin high or margin low. Once the SMM150 receives the command to margin the supply voltage, it begins adjusting the supply voltage to move toward the desired setting. When this voltage setting is reached, a bit is set in the margin status registers and the READY signal becomes active.

Note: Configuration writes or reads of registers 00_{HEX} to 03_{HEX} should not be performed while the SMM150 is margining.

FAULTS

When either of the COMP1 or COMP2 inputs are in fault, the open-drain FAULT# output will be pulled low. A configuration option exists to disable the FAULT# output while the device is margining. If "Fault Output Disabled while Margining" is selected, Faults are disabled for all margining except when margining to the 'Off' and 'Nominal' states. Also, the programmable feature 'Fault Holds Off and Shutdown Control' is enabled only for the Nominal margin state.

APPLICATIONS INFORMATION (CONTINUED)

Fault Latched by a Fault Condition:

The "Fault Latched by a Fault Condition" programmable option is triggered only on the leading edge of a Fault. That is, a latched fault can be cleared while the Fault yet exists.

Fault Latched by Ready I/O Pin:

Fault Latched by Ready I/O pin functions on the margin transitions from Off to Hi/Low/Nominal or from Nominal to Hi/Low or Hi/Low to Nominal but not from Hi/Low/Nominal to Off.

WRITE PROTECTION

Write protection for the SMM150 is located in a volatile register where the power-on state is defaulted to write protect. There are separate write protect modes for the configuration registers and memory. In order to remove write protection, the code 55_{HEX} is written to the write protection register.

Other codes will enable write protection. For example, writing 59_{HEX} will allow writes to the configuration register but not to the memory, while writing 35_{HEX} will allow writes to the memory but not to the configuration registers. The SMM150 also features a Write Protect pin (WP input) which, when asserted, prevents writing to the configuration registers and EE memory. In addition to these two forms of write protection there is a configuration register lock bit which, once programmed, does not allow the configuration registers to be changed.

A2, A1, A0

The address bits A[2:0] can be hard wired High or Low or may be left open (High-Z) to allow for a total of 21 distinct device addresses. When floating, the inputs can tolerate the amount of leakage as described by the specification I_{AIT}. An external 100k pull-up or pull down resistor is sufficient to set a High or Low logic level.

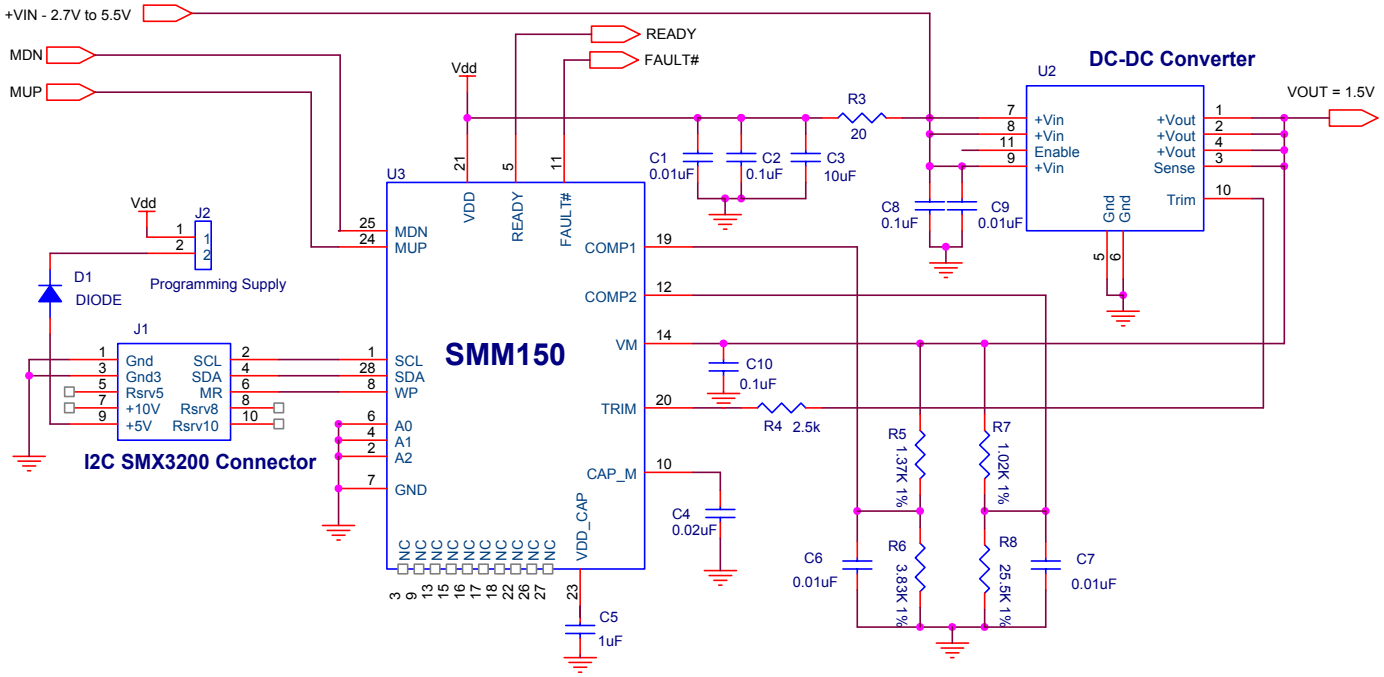


Figure 6 – Typical applications schematic which shows the SMM150 controlling a 3.3V in/1.5V out DC/DC converter. Care should be taken to filter DC/DC converter noise from the SMM150 VDD supply pin. This is accomplished with optional components R3, C1, C2, C3 and C10. This example, using a 1.25V VREF, also shows the COMP1/2 pins monitoring the DC/DC converter VOUT set to an OV of 1.7V on COMP1 and a UV of 1.3V on COMP2, the voltage divider resistors are:
For OV, R5 = 1.37k, 1% R6 = 3.83k, 1%, For UV, R7= 1.02k, 1% R8 = 25.5k, 1%.
The jumper J2 can be used to supply the SMM150 VDD voltage from the SMX3200 programmer when the device is programmed with board power off and the controlled supply unloaded.

APPLICATIONS INFORMATION (CONTINUED)

Maximizing Accuracy

Maximum margining accuracy is obtained by placing a resistor between the SMM150 TRIM output and the TRIM input of the converter. From the manufacturer's data sheet obtain the value of the internal voltage reference and equivalent TRIM input series resistance.

Figure 7 below displays the internal trimming circuit for a typical isolated DC-DC converter. In this example, the converter uses positive trimming, i.e., an increase in voltage at the TRIM pin causes an increase in output voltage.

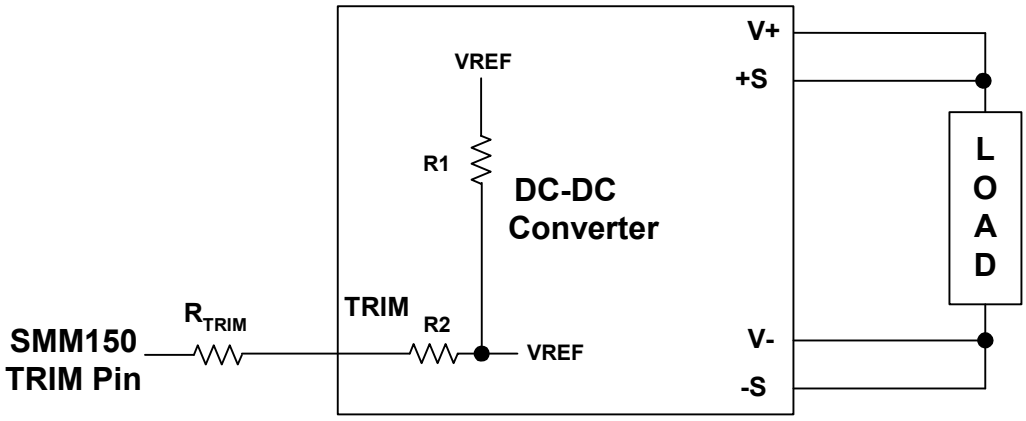


Figure 7 - Simplified TRIM circuit of an isolated DC-DC converter connects to SMM150 TRIM output

For this example R_{TRIM} is found:

$$R_{TRIM} = \frac{R2 \times \left[\frac{(VREF \times k) - 0.3}{(VREF - 0.3)} \right]}{1 - \frac{(k \times VREF - 0.3)}{(VREF - 0.3)}}$$

Where:

$$k = \frac{VM\,\arg(Low)}{VNom}$$

0.3 = TRIM output saturation voltage
Vnom = Nominal (non-trimmed output voltage)

The next example applies to most non-isolated DC-DC converters, LDO's and in-system designed converters using monolithic PWM controllers. Figure 8 is a simplified schematic showing the resistor divider network used to close the loop from the output to the circuit's feedback node. These type circuits employ negative trimming, meaning any decrease in voltage into the feedback node cause an increase in output voltage.

$$R_{TRIM} = \frac{R1 \times (VREF - 0.3)}{VNom \times (k - 1)}$$

$$k = \frac{VM\,\arg(High)}{VNom}$$

0.3 = TRIM output saturation voltage
Vnom = Nominal (non-trimmed output voltage)

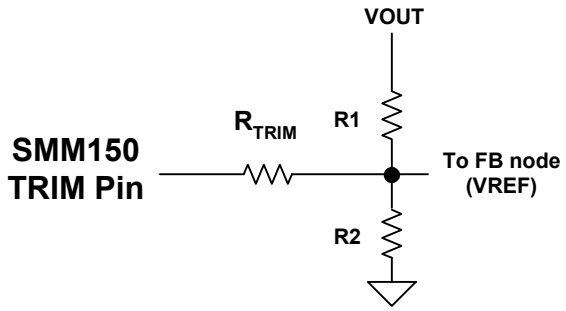


Figure 8 - Simplified TRIM circuit of a non-isolated DC-DC converter connects to SMM150 TRIM output

DEVELOPMENT HARDWARE & SOFTWARE

The end user can obtain the Summit SMX3200 programming system for device prototype development. The SMX3200 system consists of a programming Dongle, cable and Windows™ GUI software. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3200 is available from the website (www.summitmicro.com).

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus.

The Windows GUI software will generate the data and send it in I^2C serial bus format so that it can be directly downloaded to the SMM150 via the programming Dongle and cable. An example of the connection interface is shown in Figure 9.

When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

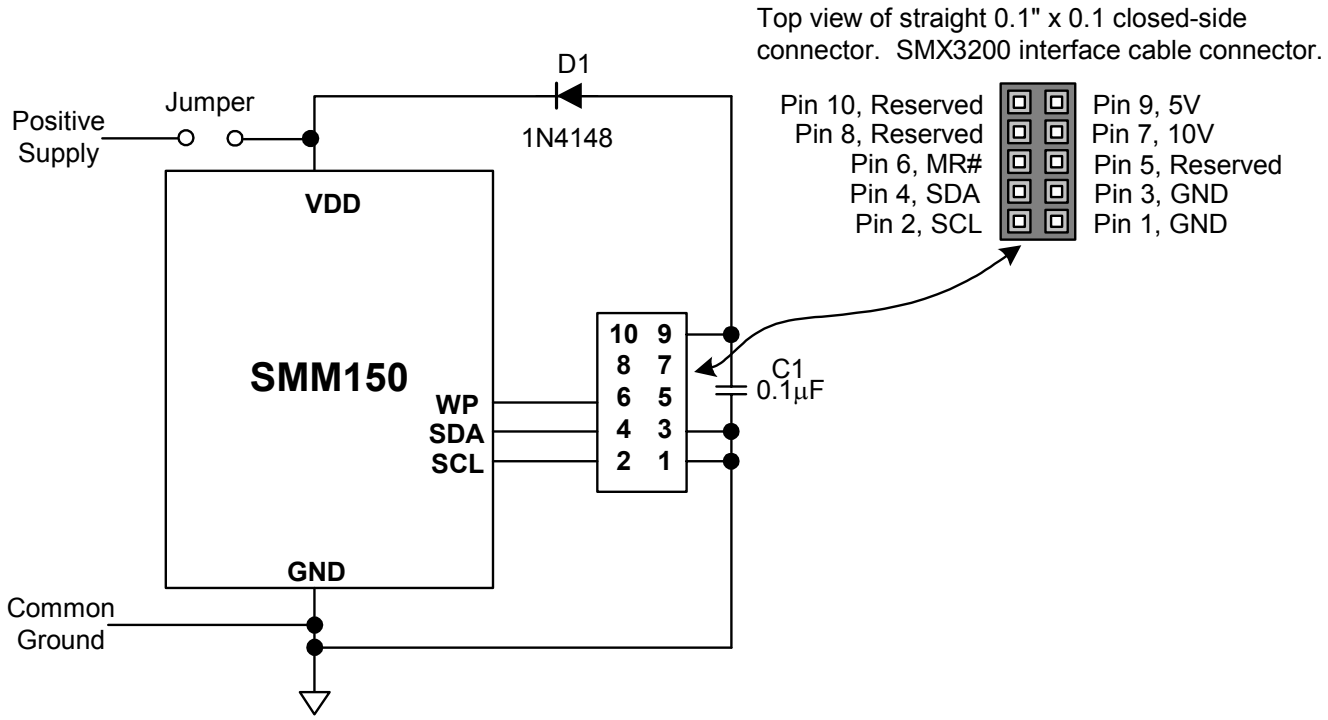


Figure 9– SMX3200 Programmer I^2C serial bus connections to program the SMM150. The SMM150 has a Write Protect pin (WP input) which when, asserted, prevents writing to the configuration registers and EE memory. In addition, there is a configuration register lock bit, which, once programmed, does not allow the configuration registers to be changed.

I²C PROGRAMMING INFORMATION

SERIAL INTERFACE

Access to the configuration registers, general-purpose memory and command and status registers is carried out over an industry standard 2-wire serial interface (I^2C). SDA is a bi-directional data line and SCL is a clock input. Data is clocked in on the rising edge of SCL and clocked out on the falling edge of SCL. All data transfers begin with the MSB. During data transfers SDA must remain stable while SCL is high. Data is transferred in 8-bit packets with an intervening clock period in which an Acknowledge is provided by the device receiving data. The SCL high period (t_{HIGH}) is used for generating Start and Stop conditions that precede and end most transactions on the serial bus. A high-to-low transition of SDA while SCL is high is considered a Start condition while a low-to-high transition of SDA while SCL is high is considered a Stop condition.

The interface protocol allows operation of multiple devices and types of devices on a single bus through unique device addressing. The address byte is comprised of a 4-bit device type identifier (slave address) and a unique (three-state) 3-bit bus address. The remaining bit indicates either a read or a write operation. Refer to Table 1 for a description of the address bytes used by the SMM150. Refer to Table 2 for an example of the unique address handling of the SMM150.

The device type identifier for the memory array, the configuration registers and the command and status registers are accessible with the same slave address. It can be set using the address pins as described in table 2.

The bus address bits A[2:0] are hard wired only through address pins 2, 4 and 6 (A2, A1 and A0) or may be left open (Z) to allow for a total of 21 distinct device addresses. The bus address accessed in the address byte of the serial data stream must match the setting on the SMM150 address pins.

WRITE

Writing to the memory or a configuration register is illustrated in Figures 10, 11, 12, 14, 15 and 17. A Start condition followed by the address byte is provided by the host; the SMM150 responds with an Acknowledge; the host then responds by sending the memory address pointer or configuration register address pointer; the SMM150 responds with an acknowledge; the host then clocks in one byte of data. For memory and configuration register writes, up to 15 additional bytes of data can be clocked in by the host to write to consecutive addresses within the same page. After the last byte is clocked in and the host receives an Acknowledge, a Stop condition must be issued to initiate the nonvolatile write operation.

READ

The address pointer for the configuration registers, memory, command and status registers and ADC registers must be set before data can be read from the SMM150. This is accomplished by issuing a dummy write command, which is simply a write command that is not followed by a Stop condition. The dummy write command sets the address from which data is read. After the dummy write command is issued, a Start command followed by the address byte is sent from the host. The host then waits for an Acknowledge and then begins clocking data out of the slave device. The first byte read is data from the address pointer set during the dummy write command. Additional bytes can be clocked out of consecutive addresses with the host providing an Acknowledge after each byte. After the data is read from the desired registers, the read operation is terminated by the host holding SDA high during the Acknowledge clock cycle and then issuing a Stop condition. Refer to Figures 13, 15 and 18 for an illustration of the read sequence.

WRITE PROTECTION

The SMM150 powers up into a write protected mode. Writing a code to the volatile write protection register (write only) can disable the write protection. The write protection register is located at address 38_{HEX}. Writing to the write protection register is shown in Figure 10.

Writing 0101_{BIN} to bits [7:4] of the write protection register allow writes to the general-purpose memory while writing 0101_{BIN} to bits [3:0] allow writes to the configuration registers. The write protection can be re-enabled by writing other codes (not 0101_{BIN}) to the write protection register.

I²C PROGRAMMING INFORMATION (CONTINUED)

CONFIGURATION REGISTERS

The majority of the configuration registers are grouped with the general-purpose memory. Writing and reading the configuration registers is shown in Figures 11, 12 and 13. See Application Note 46 for a complete description.

Note: Configuration writes or reads of registers 00 to 03_{HEX} should not be performed while the SMM150 is margining.

GENERAL-PURPOSE MEMORY

The 256-byte general-purpose memory is located at any slave address. The bus address bits are hard wired by the address pins A2, A1 and A0. They can be tied low, high or left floating, (Z). Memory writes and reads are shown in Figures 14, 15 and 16.

COMMAND AND STATUS REGISTERS

Writes and reads of the command and status registers are shown in Figures 17 and 18.

GRAPHICAL USER INTERFACE (GUI)

Device configuration utilizing the Windows based SMM150 graphical user interface (GUI) is highly recommended. The software is available from the Summit website (www.summitmicro.com). Using the GUI in conjunction with this datasheet simplifies the process of device prototyping and the interaction of the various functional blocks. A programming Dongle (SMX3200) is available from Summit to communicate with the SMM150. The Dongle connects directly to the parallel port of a PC and programs the device through a cable using the I²C bus protocol. See Figure 5 and the SMX3200 Data Sheet.

Slave Address	Bus Address	Register Type
10XX	A2 A1 A0	Configuration Registers are located in 00_{HEX} thru 05_{HEX} and 30_{HEX} thru $3E_{HEX}$
		General-Purpose Memory is located in 40_{HEX} thru FF_{HEX}

Table 1 - Address bytes used by the SMM150.

Slave Address programmed as 10XX

Pins A[2:0]				
A2	**A1**	**A0**	**Slave Address**	**Bus Address**
0	0	0	1000	000
0	0	1	1000	001
0	0	Z	1000	010
0	1	0	1000	100
0	1	1	1000	101
0	1	Z	1000	110
0	Z	X	1000	011
1	0	0	1001	000
1	0	1	1001	001
1	0	Z	1001	010
1	1	0	1001	100
1	1	1	1001	101
1	1	Z	1001	110
1	Z	X	1001	011
Z	0	0	1010	000
Z	0	1	1010	001
Z	0	Z	1010	010
Z	1	0	1010	100
Z	1	1	1010	101
Z	1	Z	1010	110
Z	Z	X	1010	011

Table 2 – Example device addresses allowed by the SMM150.

I²C PROGRAMMING INFORMATION (CONTINUED)

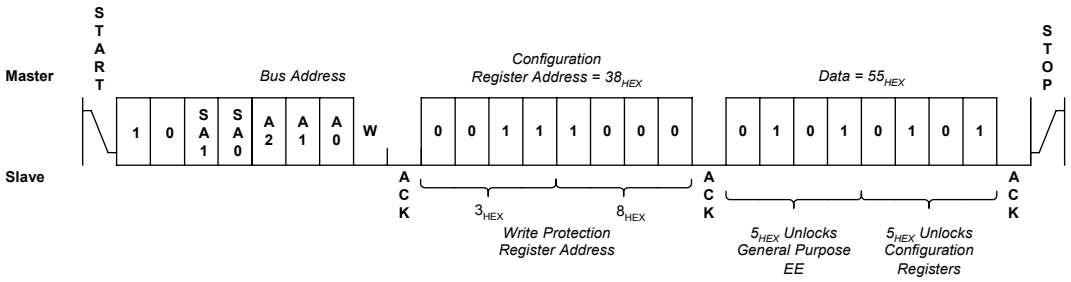


Figure 10 – Write Protection Register Write

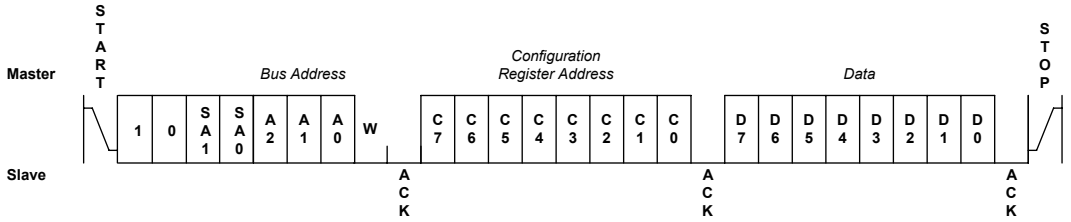


Figure 11 – Configuration Register Byte Write

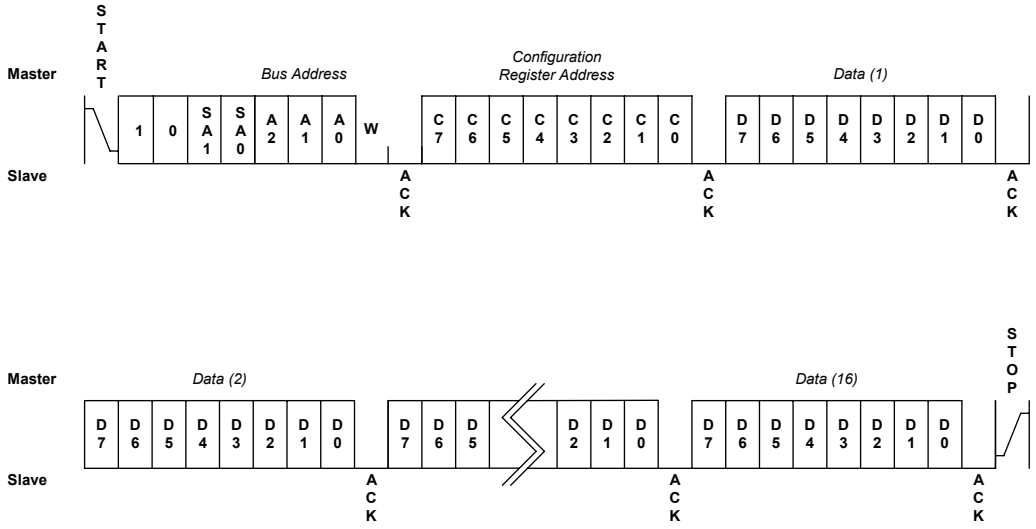


Figure 12 – Configuration Register Page Write

I²C PROGRAMMING INFORMATION (CONTINUED)

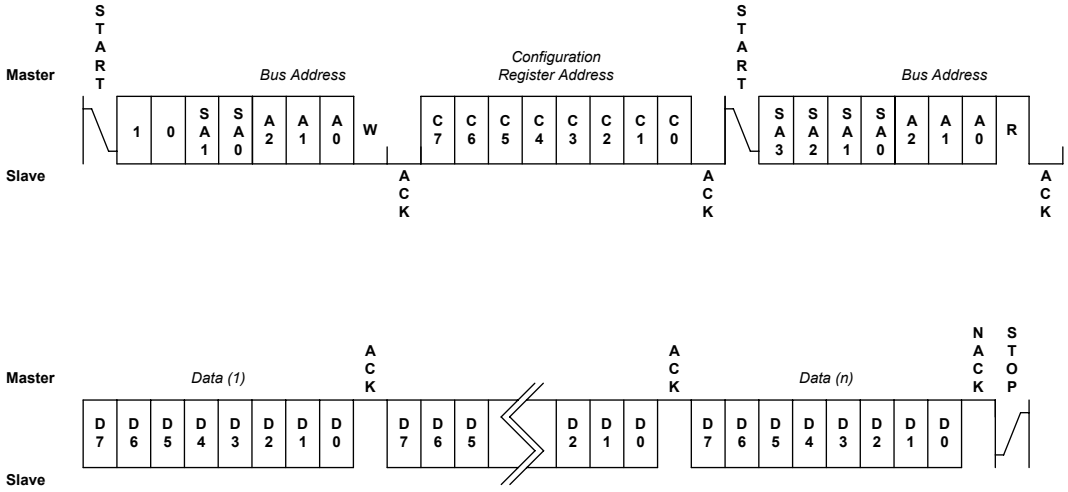


Figure 13 - Configuration Register Read

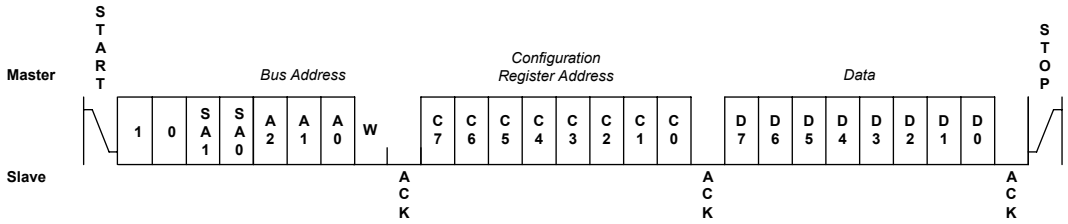


Figure 14 – General Purpose Memory Byte Write

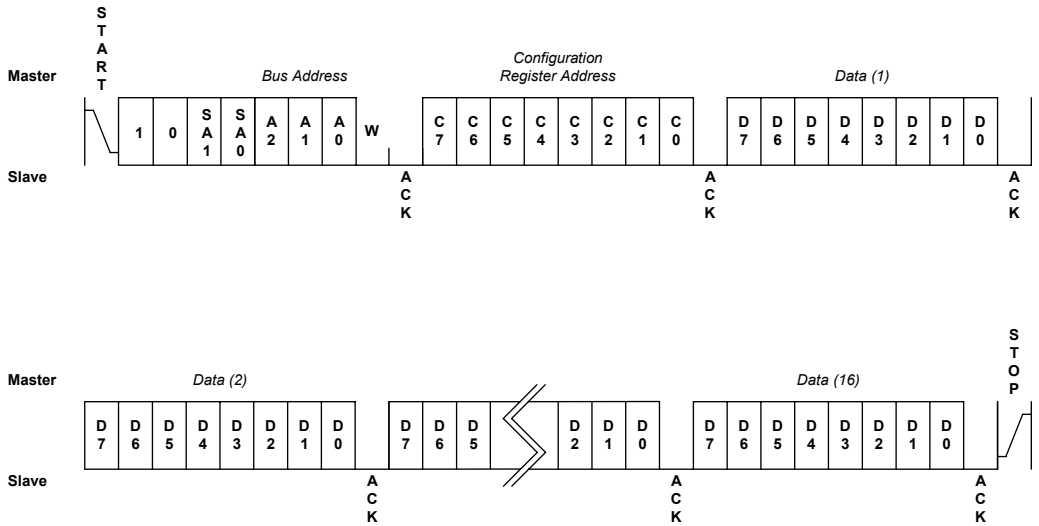


Figure 15 - General Purpose Memory Page Write

I²C PROGRAMMING INFORMATION (CONTINUED)

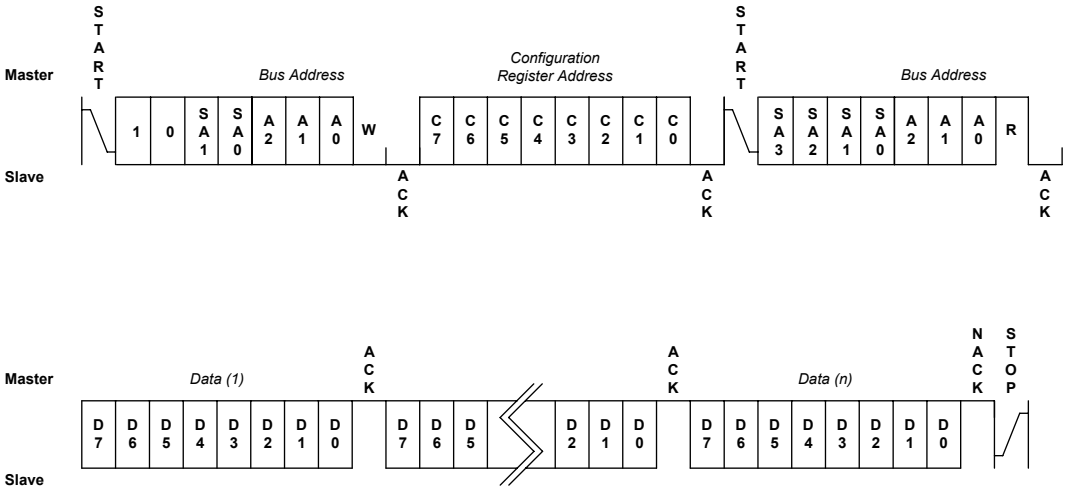


Figure 16 - General Purpose Memory Read

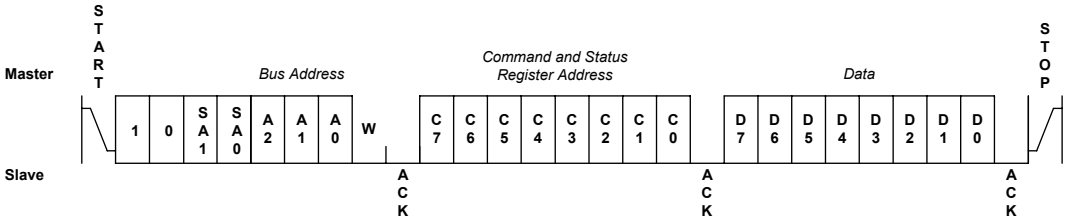


Figure 17 – Command and Status Register Write

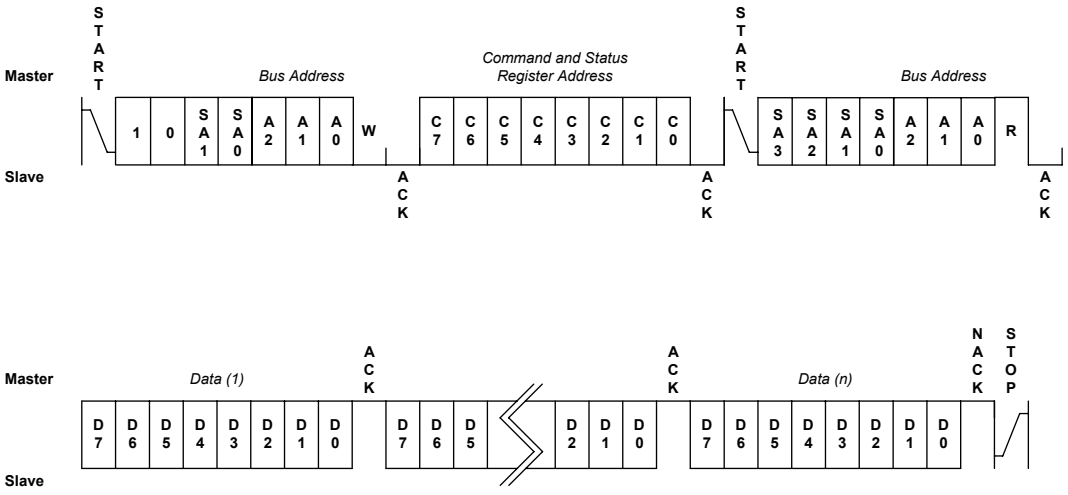


Figure 18 - Command and Status Register Read

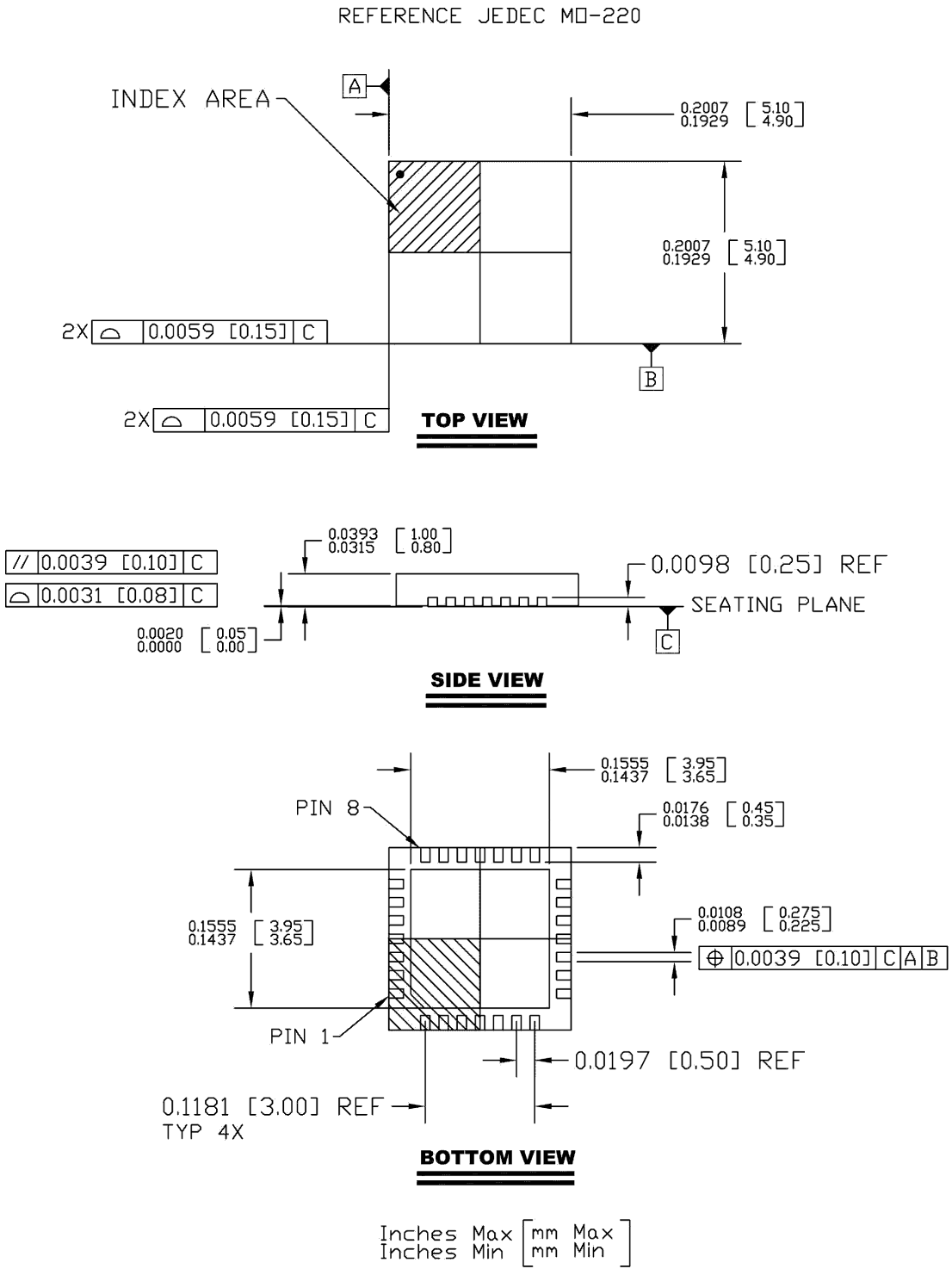
DEFAULT CONFIGURATION REGISTER SETTINGS – SMM150NC-356

Register	Contents	Function
R00	D5	Glitch filter delay time set to 120µs.
R01	71	Nominal setting is 1.802V.
R02	9A	Margin high setting is 2.002V.
R03	48	Margin low setting is 1.602V.
R04	E0	COMP1 is UV sensor, COMP2 is OV sensor, Fault output disabled when margining, Fault does not hold off or shutdown, Fault latched by Ready I/O Pin.
R05	28	Max converter Settling Time is 2.5ms, Margin I^2C command enabled, MUP/MDN pins disabled, WP is active low. VREF set to 1.25V

The default device ordering number is SMM150NC-356, is programmed as described above and tested over the commercial temperature range. See Application Note 46 for a complete description of the Configuration Register settings and corresponding Windows GUI control.

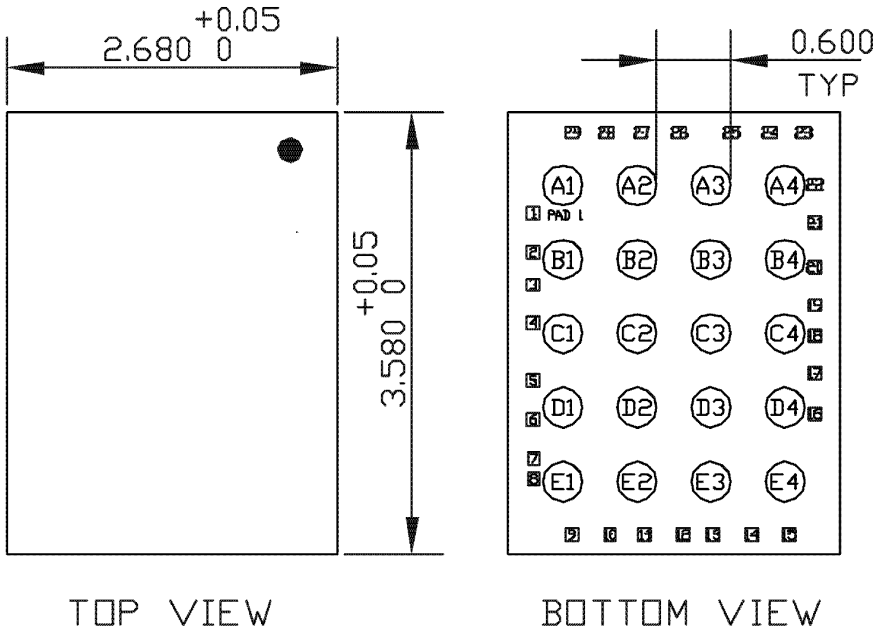
PACKAGE OUTLINES

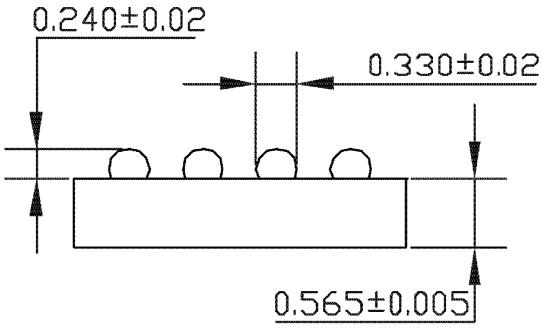
28 Pad QFN



PACKAGE OUTLINES (CONTINUED)

20 Ball *Ultra* CSP™

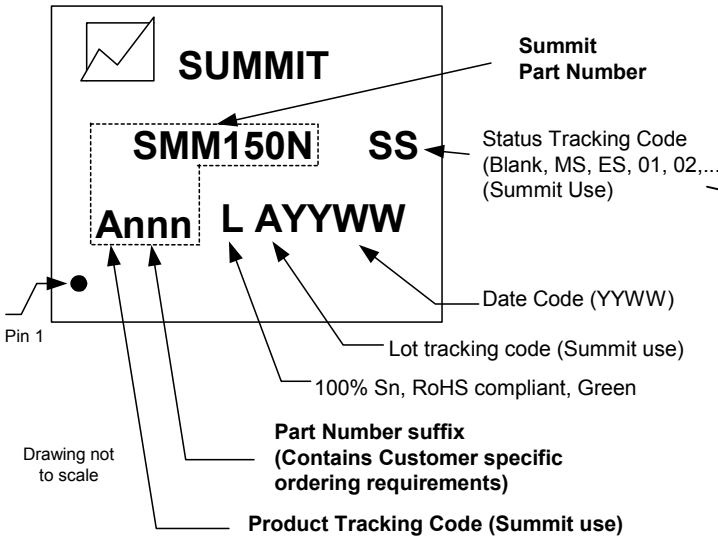




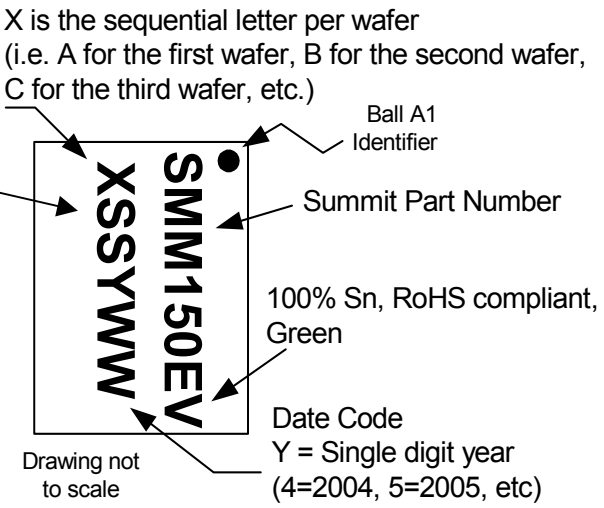
NOTES:
1. SOLDER COMPOSITION IS Sn 63% , Pb 37%
2. MELTING POINT IS 182°C ± 2°C
3. PART IS LASER MARKED 0.3mm FONT HEIGHT.
   0.2mm FONT PITCH.
   WHITE MARKING
   DEPTH: 3 TO 8um
4. ALL DIMENSIONS ARE IN MILLIMETERS [mm]

PART MARKING – QFN PACKAGE

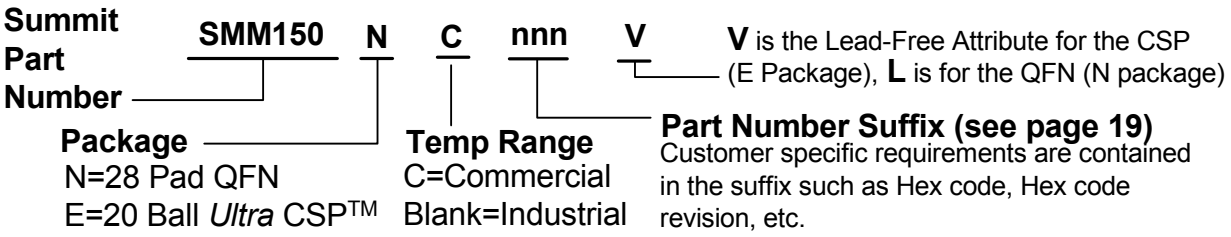
28 Pad QFN



20 Ball *Ultra* CSP™



ORDERING INFORMATION



NOTICE

NOTE 1 - This is a ***Preliminary Information*** data sheet that describes a Summit product currently in pre-production with limited characterization.

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