Data Sheet | December 15, 2011 | FN6749.1

Real-Time Clock/Calendar with Embedded Unique ID

The ISL12024IRTCZ device is a micro-power real-time clock with embedded 64-bit unique ID, timing and crystal compensation, clock/calender, power-fail indicator, two periodic or polled alarms, intelligent battery backup switching, and integrated 512x8-bit EEPROM configured in 16 Bytes per page.

The device contains a 64-bit unique ID number for security and product identification applications. It is housed in a tiny 3mmx3mm TDFN package for small handheld applications. The clock output defaults to 32.768kHz on initial power-up for low power microcontroller clocking applications. The low 800nA battery supply current extends backup battery life.

Ordering Information

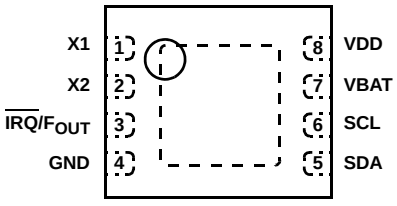
PART NUMBER (Note)	PART MARKING	V_{DD} RANGE	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL12024IRTCZ*	024C	2.7V to 5.5V	-40 to +85	8 Ld TDFN	L8.3x3I

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL12024IRTCZ
(8 LD TDFN)
TOP VIEW



Features

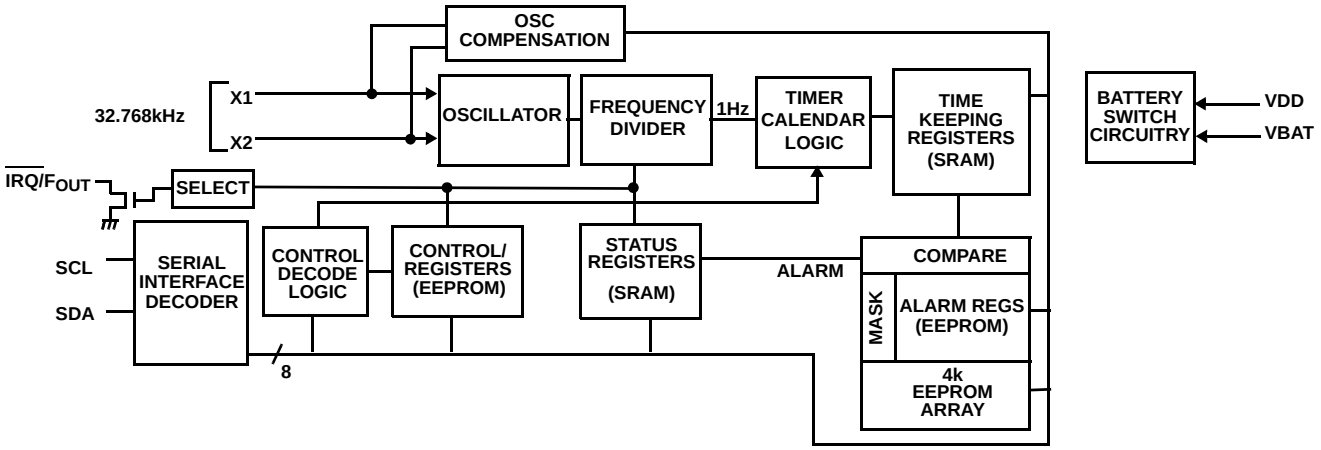
- Real-Time Clock/Calendar
  - Tracks Time in Hours, Minutes, and Seconds
  - Day of the Week, Day, Month and Year
  - 3 Selectable Frequency Outputs
- 64-Bit Unique ID
- Two Non-Volatile Alarms
  - Settable on the Second, Minute, Hour, Day of the Week, Day or Month
  - Repeat Mode (Periodic Interrupts)
- Automatic Backup to Battery or Super Cap
- Default 32.768kHz Output at $\overline{IRQ}/F_{OUT}$ (FO1 = 0, FO0 = 1)
- On-Chip Oscillator Compensation
  - Internal Feedback Resistor and Compensation Capacitors
  - 64 Position Digitally Controlled Trim Capacitor
  - 6 Digital Frequency Adjustment Settings to ±30ppm
- 512x8-Bits of EEPROM
  - 16-Bytes Page Write Mode (32 total pages)
  - 8 Modes of BlockLock™ Protection
  - Single Byte Write Capability
- High Reliability
  - Data Retention: 50 years
  - Endurance: 2,000,000 Cycles Per Byte
- I^2C Interface
  - 400kHz Data Transfer Rate
- 800nA Battery Supply Current
- Available in 8 Ld TDFN package
- Pb-Free (RoHS Compliant)

Applications

- Utility Meters
- Audio Video Equipment
- Modems
- Network Routers, Hubs, Switches, Bridges
- Cellular Infrastructure Equipment
- Fixed Broadband Wireless Equipment
- Pagers/PDA
- POS Equipment
- Test Meters/Fixtures
- Office Automation (Copiers, Fax)
- Computer Products
- Security Related Application

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Block Diagram



Pin Descriptions

PIN NUMBER		
TDFN	SYMBOL	DESCRIPTION
1	X1	The X1 pin is the input of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal.
2	X2	The X2 pin is the output of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. (See “Application Section” on page 20.)
3	$\overline{IRQ}/F_{OUT}$	Interrupt Output/Frequency Output is a multi-functional pin that can be used as interrupt or frequency output pin. The function is set via the control register. This output is an open drain configuration.
4	GND	Ground.
5	SDA	Serial Data (SDA) is a bidirectional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR’ed with other open drain or open collector outputs.
6	SCL	The Serial Clock (SCL) input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated).
7	VBAT	This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin should be tied to ground if not used.
8	VDD	Power Supply.

Absolute Maximum Ratings

Voltage on V_{DD}, V_{BAT}, SCL, SDA, and $\overline{IRQ}/F_{OUT}$ Pins (Respect to Ground). . . . . -0.3V to 6.0V
Voltage on X1 and X2 Pins (Respect to Ground). . . . . -0.3V to 2.5V
Latchup (Note 1) . . . . . Class II, Level B @ +85°C
ESD Rating (MIL-STD-883, Method 3014) . . . . . >±2kV
ESD Rating (Machine Model) . . . . . >175V

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TDFN Package	53.7	2.8

Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Operating Specifications

Unless otherwise noted, V_{DD} = +2.7V to +5.5V, T_A = -40°C to +85°C, Typical values are @ T_A = +25°C and V_{DD} = 3.3V.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 12)	TYP	MAX (Note 12)	UNIT
V_{DD}	Main Power Supply		2.7		5.5	V
V_{BAT}	Backup Power Supply		1.8		5.5	V

Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 12)	TYP	MAX (Note 12)	UNIT	NOTES
I_{DD1}	Supply Current with I^2C Active	V_{DD} = 2.7V			500	µA	3, 4, 5
		V_{DD} = 5.5V			800	µA	3, 4, 5
I_{DD2}	Supply Current for Non-Volatile Programming	V_{DD} = 2.7V			2.5	mA	3, 4, 5
		V_{DD} = 5.5V			3.5	mA	3, 4, 5
I_{DD3}	Supply Current for Main Timekeeping (Low Power Mode)	$V_{DD} = V_{SDA} = V_{SCL}$ = 2.7V			10	µA	5
		$V_{DD} = V_{SDA} = V_{SCL}$ = 5.5V			20	µA	5
I_{BAT}	Battery Supply Current	V_{BAT} = 1.8V, $V_{DD} = V_{SDA} = V_{SCL}$ = 0V		800	1000	nA	3, 6, 7
		V_{BAT} = 3.0V, $V_{DD} = V_{SDA} = V_{SCL}$ = 0V		850	1200	nA	3, 6, 7
I_{BATLKG}	Battery Input Leakage	V_{DD} = 5.5V, V_{BAT} = 1.8V			100	nA	
V_{TRIP}	V_{BAT} Mode Threshold		1.8	2.2	2.6	V	7
$V_{TRIPHYS}$	V_{TRIP} Hysteresis			30		mV	7
V_{BATHYS}	V_{BAT} Hysteresis			50		mV	7
$V_{DD\ SR-}$	V_{DD} Negative Slew Rate				10	V/ms	8
$\overline{IRQ}/F_{OUT}$							
V_{OL}	Output Low Voltage	V_{DD} = 5V I_{OL} = 3mA			0.4	V	
		V_{DD} = 1.8V I_{OL} = 1mA			0.4	V	
I_{LO}	Output Leakage Current	V_{DD} = 5.5V V_{OUT} = 5.5V		100	400	nA	

EEPROM Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Endurance		2,000,000			Cycles
EEPROM Retention	Temperature ≤ +75°C	50			Years

Serial Interface (I^2C) Specifications

DC Electrical Specifications

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 12)	TYP	MAX (Note 12)	UNITS	NOTES
V_{IL}	SDA, and SCL Input Buffer LOW Voltage		-0.3		0.3 x V_{DD}	V	
V_{IH}	SDA, and SCL Input Buffer HIGH Voltage		0.7 x V_{DD}		V_{DD} + 0.3	V	
Hysteresis	SDA and SCL Input Buffer Hysteresis		0.05 x V_{DD}			V	9, 11
V_{OL}	SDA Output Buffer LOW Voltage	I_{OL} = 4mA	0		0.4	V	
I_{LI}	Input Leakage Current on SCL	V_{IN} = 5.5V		100		nA	
I_{LO}	I/O Leakage Current on SDA	V_{IN} = 5.5V		100		nA	

AC Electrical Specifications

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 12)	TYP	MAX (Note 12)	UNITS	NOTES
f_{SCL}	SCL Frequency				400	kHz	
t_{IN}	Pulse width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.			50	ns	
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window.			900	ns	
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition.	1300			ns	
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{DD} crossing.	1300			ns	
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{DD} crossing.	600			ns	
$t_{SU:STA}$	START Condition Set-up Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}.	600			ns	
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}.	600			ns	
$t_{SU:DAT}$	Input Data Set-up Time	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}.	100			ns	
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing 70% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window.	0			ns	
$t_{SU:STO}$	STOP Condition Set-up Time	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}.	600			ns	
$t_{HD:STO}$	STOP Condition Hold Time for Read, or Volatile Only Write	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}.	600			ns	
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window.	0			ns	

AC Electrical Specifications (Continued)

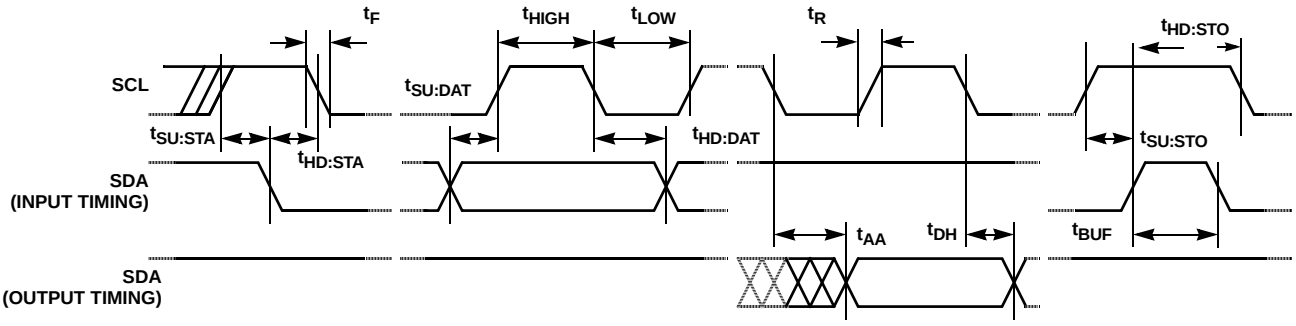
SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 12)	TYP	MAX (Note 12)	UNITS	NOTES
Cpin	SDA and SCL Pin Capacitance				10	pF	9, 11
t_{WC}	Non-Volatile Write Cycle Time			12	20	ms	10
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{DD}	20+0.1xCb		300	ns	9, 11
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{DD}	20+0.1xCb		300	ns	9, 11
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip.	10		400	pF	9, 11
R_{PU}	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2kΩ~2.5kΩ. For Cb = 40pF, max is about 15kΩ~20kΩ	1			kΩ	9, 11

NOTES:

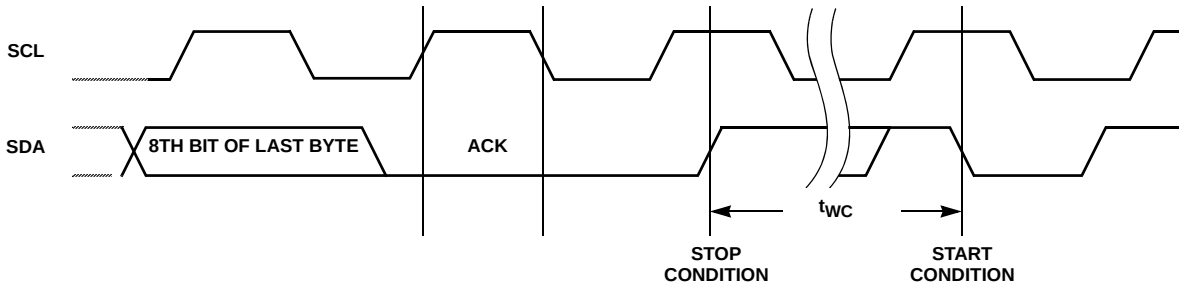
3. $\overline{IRQ}/F_{OUT}$ Inactive.
4. $V_{IL} = V_{DD}$ x 0.1, $V_{IH} = V_{DD}$ x 0.9, f_{SCL} = 400kHz
5. $V_{DD} > V_{BAT} + V_{BATHYS}$
6. Bit BSW = 0 (Standard Mode), ATR = 00h, $V_{BAT} \geq 1.8V$
7. Specified at +25°C.
8. In order to ensure proper timekeeping, the $V_{DD\ SR-}$ specification must be followed.
9. Limits established by characterization and are not production tested.
10. t_{WC} is the minimum cycle time to be allowed for any non-volatile Write by the user (it is the time from valid STOP condition at the end of Write sequence of a serial interface Write operation) to the end of the self-timed internal non-volatile write cycle.
11. These are I^2C specific parameters and are not directly tested, however they are used during device testing to validate device specification.
12. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Timing Diagrams

Bus Timing



Write Cycle Timing



Typical Performance Curves

Temperature is +25°C unless otherwise specified.

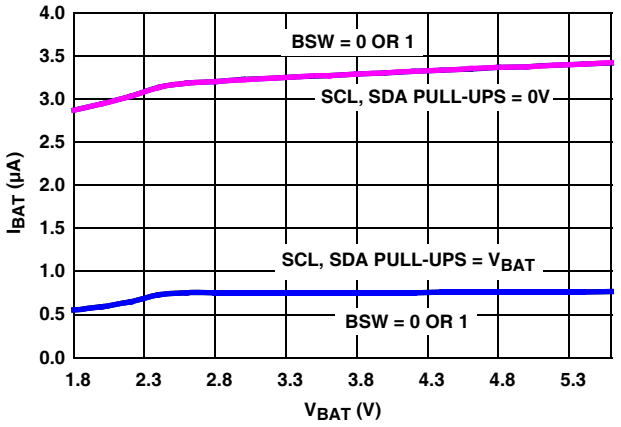


FIGURE 1. I_{BAT} vs V_{BAT}, SBIB = 0

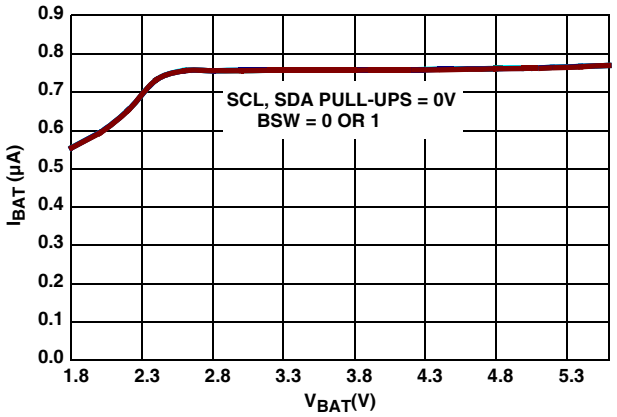


FIGURE 2. I_{BAT} vs V_{BAT}, SBIB = 1

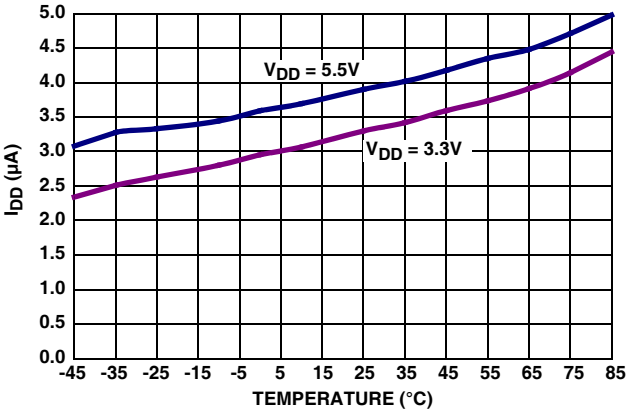


FIGURE 3. I_{DD3} vs TEMPERATURE

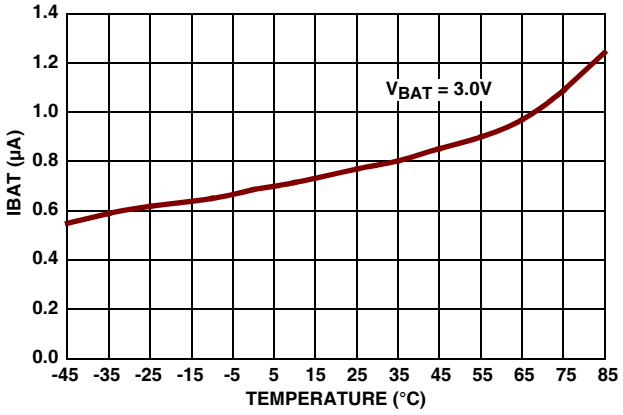


FIGURE 4. I_{BAT} vs TEMPERATURE

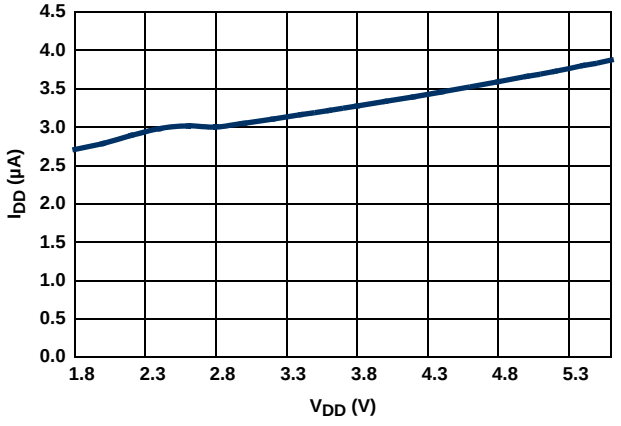


FIGURE 5. I_{DD3} vs V_{DD}

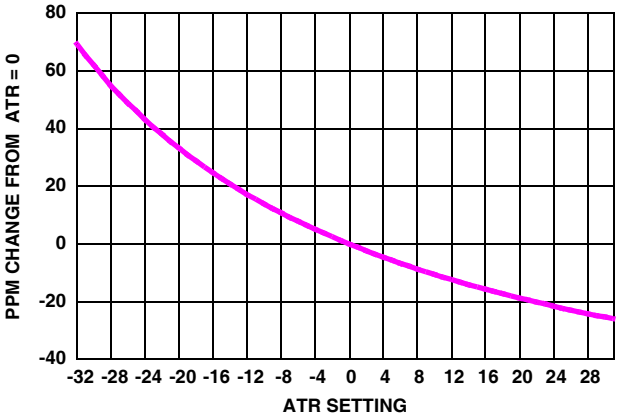


FIGURE 6. ΔF_{OUT} vs ATR SETTING

Description

The ISL12024IRTCZ device is a real-time clock with clock/calendar, 64-bit unique ID, two polled alarms with integrated 512x8 EEPROM, oscillator compensation, and battery backup switch.

The oscillator uses an external, low-cost 32.768kHz crystal. All compensation and trim components are integrated on the chip. This eliminates several external discrete components and a trim capacitor, saving board area and component cost.

The real-time clock keeps track of time with separate registers for hours, minutes and seconds. The calendar has separate registers for date, month, year and day-of-week. The calendar is correct through 2099, with automatic leap year correction.

The 64-bit unique ID is a random numbers programmed, verified and locked at the factory and it is only accessible for reading and cannot be altered by the customer.

The Dual Alarms can be set to any clock/calendar value for a match. For instance, every minute, every Tuesday, or 5:23 AM on March 21. The alarms can be polled in the Status Register or can provide a hardware interrupt ($\overline{IRQ}/F_{OUT}$ Pin). There is a pulse mode for the alarms allowing for repetitive alarm functionality.

The $\overline{IRQ}/F_{OUT}$ pin may be software selected to provide a frequency output of 1Hz, 4096Hz, or 32,768Hz or inactive.

The device offers a backup power input pin. This V_{BAT} pin allows the device to be backed up by battery or Super Cap. The entire ISL12024IRTCZ device is fully operational from 2.7V to 5.5V and the clock/calendar portion of the ISL12024IRTCZ device remains fully operational down to 1.8V (Standby Power Mode).

The ISL12024IRTCZ device provides 4k bits of EEPROM with eight modes of BlockLock™ control. The BlockLock™ allows a safe, secure memory for critical user and configuration data, while allowing a large user storage area.

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device. The input buffer on this pin is always active (not gated). The pull-up resistor on this pin must use the same voltage source as V_{DD}.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. The input buffer is always active (not gated).

This open drain output requires the use of a pull-up resistor. The pull-up resistor on this pin must use the same voltage source as V_{DD}. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed to comply with 400kHz I^2C interface speed.

V_{BAT}

This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event the V_{DD} supply fails. This pin can be connected to a battery, a Super Cap or tied to ground if not used.

$\overline{IRQ}/F_{OUT}$ (Interrupt Output/Frequency Output)

This dual function pin can be used as an interrupt or frequency output pin. The $\overline{IRQ}/F_{OUT}$ mode is selected via the frequency out control bits of the INT register.

- **Interrupt Mode.** The pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action. It is an open drain active low output.
- **Frequency Output Mode.** The pin outputs a clock signal which is related to the crystal frequency. The frequency output is user selectable and enabled via the I^2C bus. It is an open drain output.

X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal is used with the ISL12024IRTCZ to supply a timebase for the real-time clock. Internal compensation circuitry provides high accuracy over the operating temperature range from -40°C to +85°C. This oscillator compensation network can be used to calibrate the crystal timing accuracy over-temperature either during manufacturing, or with an external temperature sensor and microcontroller for active compensation. The X2 pin is intended to drive a crystal only, and should not drive any external circuit.

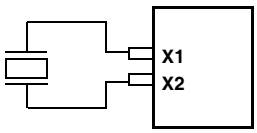


FIGURE 7. RECOMMENDED CRYSTAL CONNECTION

Real-Time Clock Operation

The real-time clock (RTC) uses an external 32.768kHz quartz crystal to maintain an accurate internal representation of the second, minute, hour, day, date, month and year. The RTC has leap-year correction. The clock also corrects for months having fewer than 31 days and has a bit that controls 24 hour or AM/PM format. When the ISL12024IRTCZ powers up after the loss of both V_{DD} and V_{BAT}, the clock will not operate until at least one byte is written to the clock register.

Reading the Real-Time Clock

The RTC is read by initiating a Read command and specifying the address corresponding to the register of the real-time clock. The RTC registers can then be read in a sequential read mode. Since the clock runs continuously, and a read

takes a finite amount of time, there is the possibility that the clock could change during the course of a read operation. In this device, the time is latched by the read command (falling edge of the clock on the ACK bit prior to RTC data output) into a separate latch to avoid time changes during the read operation. The clock continues to run. Alarms occurring during a read are unaffected by the read operation.

Writing to the Real-Time Clock

The time and date may be set by writing to the RTC registers. RTC Register should be written ONLY with Page Write. To avoid changing the current time by an incomplete write operation, write to the all 8 bytes in one write operation. When writing the RTC registers, the new time value is loaded into a separate buffer at the falling edge of the clock during the Acknowledge. This new RTC value is loaded into the RTC Register by a stop bit at the end of a valid write sequence. An invalid write operation aborts the time update procedure and the contents of the buffer are discarded. After a valid write operation, the RTC will reflect the newly loaded data beginning with the next “one second” clock cycle after the stop bit is written. The RTC continues to update the time while an RTC register write is in progress and the RTC continues to run during any non-volatile write sequences.

Accuracy of the Real-Time Clock

The accuracy of the real-time clock depends on the accuracy of the quartz crystal that is used as the time base for the RTC. Since the resonant frequency of a crystal is temperature dependent, the RTC performance will also be dependent upon temperature. The frequency deviation of the crystal is a function of the turnover-temperature of the crystal from the crystal’s nominal frequency. For example, a >20ppm frequency deviation translates into an accuracy of >1 minute per month. These parameters are available from the crystal manufacturer. Intersil’s RTC family provides on-chip crystal compensation networks to adjust load-capacitance to tune oscillator frequency from -34ppm to +80ppm when using a 12.5pF load crystal. For more detailed information, see the “Application Section” on page 20.

Clock/Control Registers (CCR)

The Control/Clock Registers are located in an area separate from the EEPROM array, and are only accessible following a slave byte of “1101111x”, and reads or writes to addresses [0000h:003Fh]. The clock/control memory map has memory addresses from 0000h to 003Fh. The defined addresses are described in Table 1. Writing to and reading from the undefined addresses are not recommended.

CCR Access

The contents of the CCR can be modified by performing a byte or a page write operation directly to any address in the CCR. Prior to writing to the CCR (except the status register), however, the WEL and RWEL bits must be set using a three step process (see section See “Writing to the Clock/Control Registers” on page 12.)

The CCR is divided into 6 sections. These are:

1. Alarm 0 (8 bytes; non-volatile)
2. Alarm 1 (8 bytes; non-volatile)
3. Control (5 bytes; non-volatile)
4. Unique ID (8 bytes; non-volatile)
5. Real-Time clock (8 bytes; volatile)
6. Status (1 byte; volatile)

Each register is read and written through buffers. The non-volatile portion (or the counter portion of the RTC) is updated only if RWEL is set, and only after a valid write operation and stop bit. A sequential read or page write operation provides access to the contents of only one section of the CCR per operation. Access to another section requires a new operation. A read or write can begin at any address in the CCR.

It is not necessary to set the RWEL bit prior to writing the status register. Section 5 (status register) supports a single byte read or write only. Continued reads or writes from this section terminates the operation.

The state of the CCR can be read by performing a random read at any address in the CCR at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. The read instruction latches all Clock registers into a buffer, so an update of the clock does not change the time being read. A sequential read of the CCR will not result in the output of data from the memory array. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read of the CCR, the address remains at the previous address +1 so the user can execute a current address read of the CCR and continue reading the next Register.

Real-Time Clock Registers

SC, MN, HR, DT, MO, YR: Clock/Calendar Registers

These registers depict BCD representations of the time. As such, SC (Seconds) and MN (Minutes) range from 00 to 59, HR (Hour) is 1 to 12 with an AM or PM indicator (H21 bit) or 0 to 23 (with MIL = 1), DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (Year) is 0 to 99.

DW: Day of the Week Register

This register provides a day of the week status, and uses three bits DY2 to DY0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-… The assignment of a numerical value to a specific day of the week is arbitrary, and may be decided by the system software designer. The default value is defined as ‘0’.

24 Hour Time

If the MIL bit of the HR register is 1, the RTC uses a 24-hour format. If the MIL bit is 0, the RTC uses a 12-hour format, and the H21 bit functions as an AM/PM indicator with a ‘1’ representing PM. The clock defaults to standard time with H21 = 0.

Leap Years

Leap years add the day February 29 and are defined as those years that are divisible by 4.

Status Register (SR)

The Status Register is located in the CCR memory map at address 003Fh. This is a volatile register only, and is used to control the WEL and RWEL write enable latches, read power status and two alarm bits. This register is separate from both the array and the Clock/Control Registers (CCR).

TABLE 1. STATUS REGISTER (SR)

ADDR	7	6	5	4	3	2	1	0
003Fh	BAT	AL1	AL0	0	0	RWEL	WEL	RTCF
Default	0	0	0	0	0	0	0	1

BAT: Battery Supply - Volatile

This bit set to “1” indicates that the device is operating from V_{BAT}, not V_{DD}. It is a read-only bit and is set/reset by hardware (ISL12024IRTCZ internally). Once the device begins operating from V_{DD}, the device sets this bit to “0”.

AL1, AL0: Alarm Bits - Volatile

These bits announce if either alarm 0 or alarm 1 match the real-time clock. If there is a match, the respective bit is set to ‘1’. The falling edge of the last data bit in a SR Read operation resets the flags. (Note: Only the AL bits that are set when an SR read starts will be reset). An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

RWEL: Register Write Enable Latch Volatile

This bit is a volatile latch that powers up in the LOW (disabled) state. The RWEL bit must be set to “1” prior to any writes to the Clock/Control Registers. Writes to RWEL bit do not cause a non-volatile write cycle, so the device is ready for the next operation immediately after the stop condition. A write to the CCR requires both the RWEL and WEL bits to be set in a specific sequence.

WEL: Write Enable Latch - Volatile

The WEL bit controls the access to the CCR during a write operation. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes to the CCR address will be ignored, although acknowledgment is still issued. The WEL bit is set by writing a “1” to the WEL bit and zeroes to the other bits of the Status Register. Once set, WEL remains set until either reset to 0 (by writing a “0” to the WEL bit and zeroes to the other bits of the Status Register) or until the part powers up again. Writes to WEL bit do not cause a non-volatile write cycle, so the device is ready for the next operation immediately after the stop condition.

RTCF: Real-Time Clock Fail Bit - Volatile

This bit is set to a ‘1’ after a total power failure. This is a read only bit that is set internally when the device powers up after having lost all power to the device. The bit is set regardless of whether V_{DD} or V_{BAT} is applied first. The loss of only one of the supplies does not result in setting the RTCF bit. The first valid write to the RTC after a complete power failure (writing one byte is sufficient) resets the RTCF bit to ‘0’.

Unused Bits:

Bit 3 in the SR is not used, but must be zero. The Data Byte output during a SR read will contain a zero in this bit location.

TABLE 2. CLOCK/CONTROL MEMORY MAP

ADDR.	TYPE	REG NAME	BIT 7	6	5	4	3	2	1	0	RANGE	DEFAULT
003F	Status	SR	BAT	AL1	AL0	0	0	RWEL	WEL	RTCF		01h
0037	RTC (SRAM)	Y2K	0	0	Y2K21	Y2K20	Y2K13	0	0	Y2K10	19/20	20h
0036		DW	0	0	0	0	0	DY2	DY1	DY0	0-6	00h
0035		YR	Y23	Y22	Y21	Y20	Y13	Y12	Y11	Y10	0-99	00h
0034		MO	0	0	0	G20	G13	G12	G11	G10	1-12	00h
0033		DT	0	0	D21	D20	D13	D12	D11	D10	1-31	01h
0032		HR	MIL	0	H21	H20	H13	H12	H11	H10	0-23	00h
0031		MN	0	M22	M21	M20	M13	M12	M11	M10	0-59	00h
0030		SC	0	S22	S21	S20	S13	S12	S11	S10	0-59	00h
0027	Device ID	ID7	ID77	ID76	ID75	ID74	ID73	ID72	ID71	ID70		*
0026		ID6	ID67	ID66	ID65	ID64	ID63	ID62	ID61	ID60		*
0025		ID5	ID57	ID56	ID55	ID54	ID53	ID52	ID51	ID50		*
0024		ID4	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40		*
0023		ID3	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		*
0022		ID2	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		*
0021		ID1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		*
0020		ID0	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00		*
0014	Control (EEPROM)	PWR	SBIB	BSW	0	0	0	0	0	0		40h
0013		DTR	0	0	0	0	0	DTR2	DTR1	DTR0		00h
0012		ATR	0	0	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0		00h
0011		INT	IM	AL1E	AL0E	FO1	FO0	0	0	0		08h
0010		BL	BP2	BP1	BP0	0	0	0	0	0		00h
000F	Alarm1 (EEPROM)	Y2K1	0	0	A1Y2K21	A1Y2K20	A1Y2K13	0	0	A1Y2K10	19/20	20h
000E		DWA1	EDW1	0	0	0	0	DY2	DY1	DY0	0-6	00h
000D		YRA1	Unused - Default = RTC Year value (No EEPROM) - Future expansion									
000C		MOA1	EMO1	0	0	A1G20	A1G13	A1G12	A1G11	A1G10	1-12	00h
000B		DTA1	EDT1	0	A1D21	A1D20	A1D13	A1D12	A1D11	A1D10	1-31	00h
000A		HRA1	EHR1	0	A1H21	A1H20	A1H13	A1H12	A1H11	A1H10	0-23	00h
0009		MNA1	EMN1	A1M22	A1M21	A1M20	A1M13	A1M12	A1M11	A1M10	0-59	00h
0008		SCA1	ESC1	A1S22	A1S21	A1S20	A1S13	A1S12	A1S11	A1S10	0-59	00h
0007	Alarm0 (EEPROM)	Y2K0	0	0	A0Y2K21	A0Y2K20	A0Y2K13	0	0	A0Y2K10	19/20	20h
0006		DWA0	EDW0	0	0	0	0	DY2	DY1	DY0	0-6	00h
0005		YRA0	Unused - Default = RTC Year value (No EEPROM) - Future expansion									
0004		MOA0	EMO0	0	0	A0G20	A0G13	A0G12	A0G11	A0G10	1-12	00h
0003		DTA0	EDT0	0	A0D21	A0D20	A0D13	A0D12	A0D11	A0D10	1-31	00h
0002		HRA0	EHR0	0	A0H21	A0H20	A0H13	A0H12	A0H11	A0H10	0-23	00h
0001		MNA0	EMN0	A0M22	A0M21	A0M20	A0M13	A0M12	A0M11	A0M10	0-59	00h
0000		SCA0	ESC0	A0S22	A0S21	A0S20	A0S13	A0S12	A0S11	A0S10	0-59	00h

NOTE: Shaded cells indicate that NO other value is to be written to that bit. *Indicates set at the factory, read only:

Alarm Registers (Non-Volatile)

Alarm0 and Alarm1

The alarm register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = “1”). These enable bits specify which alarm registers (seconds, minutes, etc.) are used to make the comparison. Note that there is no alarm byte for year.

The alarm function works as a comparison between the alarm registers and the RTC registers. As the RTC advances, the alarm will be triggered once a match occurs between the alarm registers and the RTC registers. Any one alarm register, multiple registers, or all registers can be enabled for a match. See “Device Operation” on page 12 and “Application Section” on page 20 for more information.

Control Registers (Non-Volatile)

The Control Bits and Registers described in the following are non-volatile.

BL Register

BP2, BP1, BP0 - Block Protect Bits

The Block Protect Bits, BP2, BP1 and BP0, determine which blocks of the array are write protected. A write to a protected block of memory is ignored. The block protect bits will prevent write operations to one of eight segments of the array. The partitions are described in Table 3.

TABLE 3.

BP2	BP1	BP0	PROTECTED ADDRESSES ISL12024IRTCZ	ARRAY LOCK
0	0	0	None (Default)	None
0	0	1	180_h – $1FF_h$	Upper 1/4
0	1	0	100_h – $1FF_h$	Upper 1/2
0	1	1	000_h – $1FF_h$	Full Array
1	0	0	000_h – $03F_h$	First 4 Pages
1	0	1	000_h – $07F_h$	First 8 Pages
1	1	0	000_h – $0FF_h$	First 16 Pages
1	1	1	000_h – $1FF_h$	Full Array

INT Register: Interrupt Control and Frequency Output Register

IM, AL1E, AL0E - Interrupt Control and Status Bits

There are two Interrupt Control bits; Alarm 1 Interrupt Enable (AL1E) and Alarm 0 Interrupt Enable (AL0E) to specifically enable or disable the alarm interrupt signal output ($\overline{IRQ}/F_{OUT}$). The interrupts are enabled when either the AL1E or AL0E or both bits are set to ‘1’ and both the FO1 and FO0 bits are set to 0 (F_{OUT} disabled).

The IM bit enables the pulsed interrupt mode. To enter this mode, the AL0E or AL1E bits are set to “1”, and the IM bit to “1”. The $\overline{IRQ}/F_{OUT}$ output will now be pulsed each time an alarm occurs. This means that once the interrupt mode alarm is set, it will continue to alarm for each occurring match of the alarm and present time. This mode is convenient for hourly or daily hardware interrupts in microcontroller applications such as security cameras or utility meter reading.

In this case, both Alarms are enabled.

FO1, FO0 - Programmable Frequency Output Bits

These are two output control bits. They select one of three divisions of the internal oscillator, that is applied to the $\overline{IRQ}/F_{OUT}$ output pin. Table 4 shows the selection bits for this output. When using this function, the Alarm output function is disabled.FO1 and FO0 are set to “01” for 32.768kHz output at power-up.

TABLE 4. PROGRAMMABLE FREQUENCY OUTPUT BITS

FO1	FO0	OUTPUT FREQUENCY
0	0	Alarm output (F_{OUT} disabled)
0	1	32.768kHz (default setting)
1	0	4096Hz
1	1	1Hz

Oscillator Compensation Registers

There are two trimming options.

- ATR. Analog Trimming Register
- DTR. Digital Trimming Register

These registers are non-volatile. The combination of analog and digital trimming can give up to -64ppm to +110 ppm of total adjustment.

ATR Register - ATR5, ATR4, ATR3, ATR2, ATR1, ATR0: Analog Trimming Register

Six analog trimming bits, ATR0 to ATR5, are provided in order to adjust the on-chip load capacitance value for frequency compensation of the RTC. Each bit has a different weight for capacitance adjustment. For example, using a Citizen CFS-206 crystal with different ATR bit combinations provides an estimated ppm adjustment range from -34ppm to +80ppm to the nominal frequency compensation.

The effective on-chip series load capacitance, C_{LOAD}, ranges from 4.5pF to 20.25pF with a mid-scale value of 12.5pF (default). C_{LOAD} is changed via two digitally controlled capacitors, C_{X1} and C_{X2}, connected from the X1 and X2 pins to ground (see Figure 8). The value of C_{X1} and C_{X2} is given Equation 1:

$$C_X = (16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9)pF \quad \text{(EQ. 1)}$$

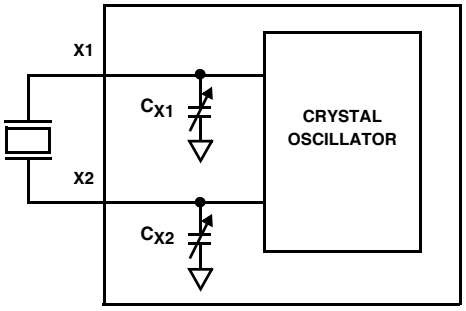


FIGURE 8. DIAGRAM OF ATR

The effective series load capacitance is the combination of C_{X1} and C_{X2}:

$$C_{LOAD} = \frac{1}{\left(\frac{1}{C_{X1}} + \frac{1}{C_{X2}}\right)} \quad \text{(EQ. 2)}$$

$$C_{LOAD} = \left(\frac{16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9}{2}\right) pF$$

For example:
C_{LOAD}(ATR = 00000) = 12.5pF,
C_{LOAD}(ATR = 100000) = 4.5pF, and
C_{LOAD}(ATR = 011111) = 20.25pF.

The entire range for the series combination of load capacitance goes from 4.5pF to 20.25pF in 0.25pF steps. Note that these are typical values.

DTR Register - DTR2, DTR1, DTR0: Digital Trimming Register

The digital trimming Bits DTR2, DTR1 and DTR0 adjust the number of counts per second and average the ppm error to achieve better accuracy.

DTR2 is a sign bit, where:
DTR2 = 0 means frequency compensation is >0.
DTR2 = 1 means frequency compensation is <0.

DTR1 and DTR0 are scale bits. DTR1 gives 10 ppm adjustment and DTR0 gives 20 ppm adjustment.

A range from -30ppm to +30ppm can be represented by using the three DTR bits above.

TABLE 5. DIGITAL TRIMMING REGISTERS

DTR REGISTER			ESTIMATED FREQUENCY PPM
DTR2	DTR1	DTR0	
0	0	0	0
0	1	0	+10
0	0	1	+20
0	1	1	+30
1	0	0	0
1	1	0	-10
1	0	1	-20
1	1	1	-30

PWR Register: SBIB, BSW

SBIB: Serial Bus Interface (Enable)

The serial bus can be disabled in Battery Backup Mode by setting this bit to “1”. This will minimize power drain on the battery. The Serial Interface can be enabled in Battery Backup Mode by setting this bit to “0” (default is “0”). See “Power Control Operation” on page 13.

BSW: Power Control Bit

The Power Control bit, BSW, determines the conditions for switching between V_{DD} and Backup Battery. There are two options:

- Option 1. Standard/Default Mode: Set “BSW = 0”
- Option 2. Legacy Mode: Set “BSW = 1”

See “Power Control Operation” on page 13 for more details. Also see “I^2C Communications During Battery Backup” on page 23 for important details.

Unique ID Registers

There are eight register bytes for storing the device ID. (Address 0020h to 0027h). Each device contains these bytes to provide a unique 64-bit ID programmed and tested in the factory before shipment. These registers are read-only, intended for serialization of end equipment, and cannot be changed or overwritten.

Device Operation

Writing to the Clock/Control Registers

Changing any of the bits of the clock/control registers requires the following steps:

1. Write a 02h to the Status Register to set the Write Enable Latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation preceded by a start and ended with a stop).
2. Write a 06h to the Status Register to set both the Register Write Enable Latch (RWEL) and the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation proceeded by a start and ended with a stop).

Write all eight bytes to the RTC registers, or one byte to the SR, or one to five bytes to the control registers. This sequence starts with a start bit, requires a slave byte of “11011110” and an address within the CCR and is terminated by a stop bit. A write to the EEPROM registers in the CCR will initiate a non-volatile write cycle and will take up to 20ms to complete. A write to the RTC registers (SRAM) will require much shorter cycle time ($t = t_{BUF}$). Writes to undefined areas have no effect. The RWEL bit is reset by the completion of a write to the CCR, so the sequence must be repeated to again initiate another change to the CCR contents. If the sequence is not completed for any reason (by sending an incorrect number of bits or sending a start instead of a stop, for example) the RWEL bit is not reset and the device remains in an active mode. Writing all zeros to the status

register resets both the WEL and RWEL bits. A read operation occurring between any of the previous operations will not interrupt the register write operation.

Alarm Operation

Since the alarm works as a comparison between the alarm registers and the RTC registers, it is ideal for notifying a host processor of a particular time event and trigger some action as a result. The host can be notified by either a hardware interrupt (the $\overline{IRQ}/F_{OUT}$ pin) or by polling the Status Register (SR) Alarm bits. These two volatile bits (AL1 for Alarm 1 and AL0 for Alarm 0), indicate if an alarm has happened. The bits are set on an alarm condition regardless of whether the $\overline{IRQ}/F_{OUT}$ interrupt is enabled. The AL1 and AL0 bits in the status register are reset by the falling edge of the eighth clock of status register read.

There are two alarm operation modes: Single Event and periodic Interrupt Mode:

1. **Single Event Mode** is enabled by setting the AL0E or AL1E bit to “1”, the IM bit to “0”, and disabling the frequency output. This mode permits a one-time match between the alarm registers and the RTC registers. Once this match occurs, the AL0 or AL1 bit is set to “1” and the $\overline{IRQ}/F_{OUT}$ output will be pulled low and will remain low until the AL0 or AL1 bit is read, which will automatically resets it. Both Alarm registers can be set at the same time to trigger alarms. The $\overline{IRQ}/F_{OUT}$ output will be set by either alarm, and will need to be cleared to enable triggering by a subsequent alarm. Polling the SR will reveal which alarm has been set.
2. **Interrupt Mode** (or “Pulsed Interrupt Mode” or PIM) is enabled by setting the AL0E or AL1E bit to “1” the IM bit to “1”, and disabling the frequency output. If both AL0E and AL1E bits are set to 1, then only the AL0E PIM alarm will function (AL0E overrides AL1E). The $\overline{IRQ}/F_{OUT}$ output will now be pulsed each time an alarm occurs. This means that once the Interrupt Mode alarm is set, it will continue to alarm for each occurring match of the alarm and present time. This mode is convenient for hourly or daily hardware interrupts in microcontroller applications such as security cameras or utility meter reading. Interrupt Mode CANNOT be used for general periodic alarms, however, since a specific time period cannot be programmed for interrupt, only matches to a specific time of day. The Interrupt Mode is only stopped by disabling the IM bit or the Alarm Enable bits.

Writing to the Alarm Registers

The Alarm Registers are non-volatile but require special attention to insure a proper non-volatile write takes place. Specifically, byte writes to individual registers are good for all but registers 0006h and 0000Eh, which are the DWA0 and DWA1 registers, respectively. Those registers will require a special page write for nonvolatile storage. The recommended page write sequences are as follows:

1. **16-byte page writes:** The best way to write or update the Alarm Registers is to perform a 16-byte write beginning at address 0001h (MNA0) and wrapping around and ending at address 0000h (SCA0). This will insure that non-volatile storage takes place. This means that the code must be designed so that the Alarm0 data is written starting with Minutes register, and then all the Alarm1 data, with the last byte being the Alarm0 Seconds (the page ends at the Alarm1 Y2k register and then wraps around to address 0000h).

   Alternatively, the 16-byte page write could start with address 0009h, wrap around and finish with address 0008h. Note that any page write ending at address 0007h or 000Fh (the highest byte in each Alarm) will not trigger a non-volatile write, so wrapping around or overlapping to the following Alarm's Seconds register is advised.
2. **Other non-volatile writes:** It is possible to do writes of less than an entire page, but the final byte must always be addresses 0000h through 0004h or 0008h though 000Ch to trigger a non-volatile write. Writing to those blocks of 5 bytes sequentially, or individually, will trigger a non-volatile write. If the DWA0 or DWA1 registers need to be set, then enough bytes will need to be written to overlap with the other Alarm register and trigger the non-volatile write. For Example, if the DWA0 register is being set, then the code can start with a multiple byte write beginning at address 0006h, and then write 3 bytes ending with the SCA1 register as follows:

Addr	Name
0006h	DWA0
0007h	Y2K0
0008h	SCA1

If the Alarm1 is used, SCA1 would need to have the correct data written.

Power Control Operation

The power control circuit accepts a V_{DD} and a V_{BAT} input. Many types of batteries can be used with Intersil RTC products. For example, 3.0V or 3.6V Lithium batteries are appropriate, and battery sizes are available that can power an Intersil RTC device for up to 10 years. Another option is to use a Super Cap for applications where V_{DD} is interrupted for up to a month. See the “Application Section” on page 20 for more information.

There are two options for setting the change-over conditions from V_{DD} to Battery Backup Mode. The BSW bit in the PWR register controls this operation:

- Option 1 - Standard Mode
- Option 2 - Legacy Mode (Default)

Note that the I^2C bus may or may not be operational during battery backup, which is controlled by the SBIB bit. See “Backup Battery Operation” on page 21 for information.

The V_{DD}/V_{BAT} power circuit also contains a glitch detection circuit to protect from incorrect serial bus writes after a brownout situation. This circuit disables the serial bus for about 90ms following the power-up. To trigger the delay, the

V_{DD} must drop below the battery trip point yet stay above approximately 1.0V (limit of active circuit operation). After that, the power-up ramp must be slower than 0.25V/ms to trigger the delay. To be safe, serial interface software may need to consider the 90ms delay in all power-up routines.

OPTION 1 - STANDARD (POWER CONTROL) MODE

In the Standard Mode, the supply will switch over to the battery when V_{DD} drops below V_{TRIP} or V_{BAT}, whichever is lower. In this mode, accidental operation from the battery is prevented since the battery backup input will only be used when the V_{DD} supply is shut off.

To select Option 1, BSW bit in the Power Register must be set to “BSW = 0”. A description of power switchover follows:

Standard Mode Power Switchover

- Normal Operating Mode (V_{DD}) to Battery Backup Mode (V_{BAT})

  To transition from the V_{DD} to V_{BAT} mode, both of the following conditions must be met:

  - Condition 1:
    $V_{DD} < V_{BAT} - V_{BATHYS}$
    where $V_{BATHYS} \approx 50mV$
  - Condition 2:
    $V_{DD} < V_{TRIP}$
    where $V_{TRIP} \approx 2.2V$

- Battery Backup Mode (V_{BAT}) to Normal Mode (V_{DD})

  The ISL12024IRTCZ device will switch from the V_{BAT} to V_{DD} mode when one of the following conditions occurs:

  - Condition 1:
    $V_{DD} > V_{BAT} + V_{BATHYS}$
    where $V_{BATHYS} \approx 50mV$
  - Condition 2**:**
    $V_{DD} > V_{TRIP} + V_{TRIPHYS}$
    where $V_{TRIPHYS} \approx 30mV$

There are two discrete situations that are possible when using Standard Mode: $V_{BAT} < V_{TRIP}$ and $V_{BAT} > V_{TRIP}$. These two power control situations are illustrated in Figures 9 and 10.

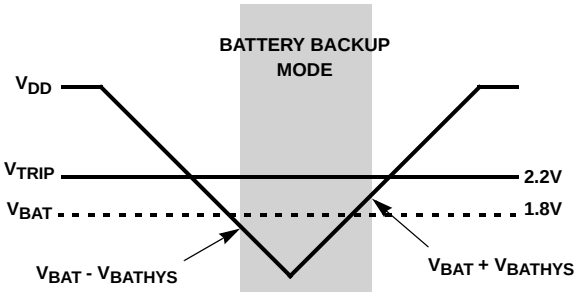


FIGURE 9. BATTERY SWITCHOVER WHEN $V_{BAT} < V_{TRIP}$

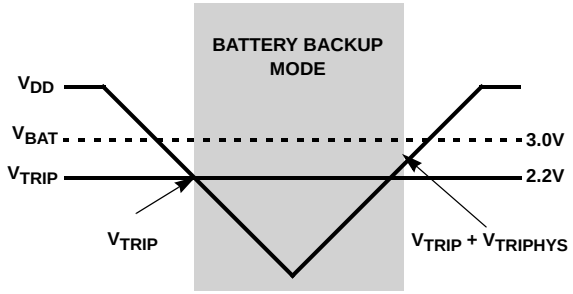


FIGURE 10. BATTERY SWITCHOVER WHEN $V_{BAT} > V_{TRIP}$

OPTION 2 - LEGACY (POWER CONTROL) MODE (DEFAULT)

The Legacy Mode follows conditions set in X1226 products. In this mode, switching from V_{DD} to V_{BAT} is simply done by comparing the voltages and the device operates from whichever is the higher voltage. Care should be taken when changing from Normal to Legacy Mode. If the V_{BAT} voltage is higher than V_{DD}, then the device will enter battery backup and unless the battery is disconnected or the voltage decreases, the device will no longer operate from V_{DD}.

To select Option 2, the BSW bit in the Power Register must be set to “BSW = 1”.

- Normal Mode (V_{DD}) to Battery Backup Mode (V_{BAT})

  To transition from the V_{DD} to V_{BAT} mode, the following conditions must be met:

  $V_{DD} < V_{BAT} - V_{BATHYS}$

- Battery Backup Mode (V_{BAT}) to Normal Mode (V_{DD})

  The device will switch from the V_{BAT} to V_{DD} mode when the following condition occurs:

  $V_{DD} > V_{BAT} + V_{BATHYS}$

The Legacy Mode power control conditions are illustrated in Figure 11..

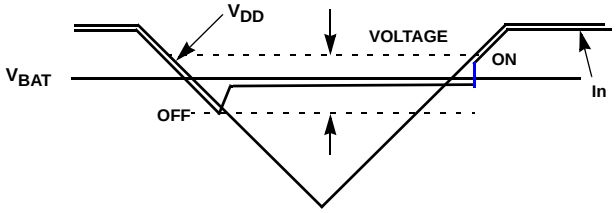


FIGURE 11. BATTERY SWITCHOVER IN LEGACY MODE

Serial Communication

The device supports the I^2C protocol.

Clock and Data

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (see Figure 12).

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met (see Figure 13).

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby Power Mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus (see Figure 13).

Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting 8 bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the 8 bits of data (see Figure 14).

The device will respond with an acknowledge after recognition of a start condition and if the correct Device Identifier and Select bits are contained in the Slave Address Byte. If a write operation is selected, the device will respond with an acknowledge after the receipt of each subsequent 8-bit word. The device will not acknowledge if the slave address byte is incorrect.

In the read mode, the device will transmit 8-bits of data, release the SDA line, then monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. The device will terminate further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to Standby Power Mode and place the device into a known state.

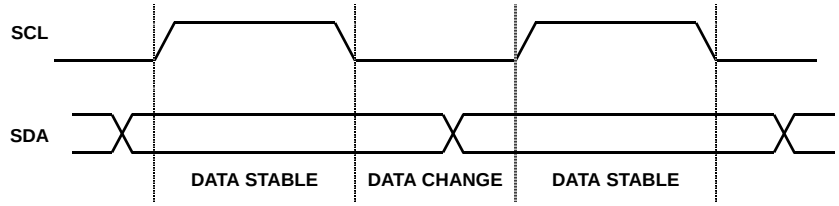


FIGURE 12. VALID DATA CHANGES ON THE SDA BUS

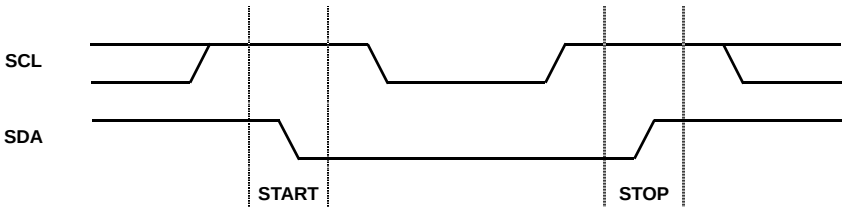


FIGURE 13. VALID START AND STOP CONDITIONS

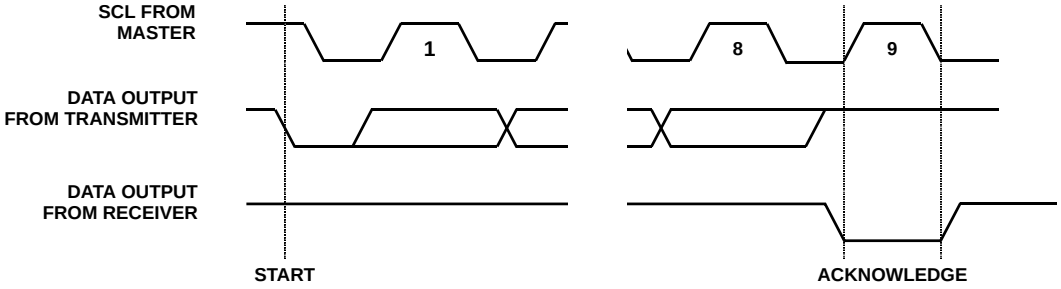


FIGURE 14. ACKNOWLEDGE RESPONSE FROM RECEIVER

Device Addressing

Following a start condition, the master must output a Slave Address Byte. The first four bits of the Slave Address Byte specify access to either the EEPROM array or to the CCR. Slave bits ‘1010’ access the EEPROM array. Slave bits ‘1101’ access the CCR.

When shipped from the factory, EEPROM array is UNDEFINED, and should be programmed by the customer to a known state.

Bit 3 through Bit 1 of the slave byte specify the device select bits. These are set to ‘111’.

The last bit of the Slave Address Byte defines the operation to be performed. When this R/$\overline{W}$ bit is a one, then a read operation is selected. A zero selects a write operation (see Figure 15.)

After loading the entire Slave Address Byte from the SDA bus, the ISL12024IRTCZ compares the device identifier and device select bits with ‘1010111’ or ‘1101111’. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a two byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up, the internal address counter is set to address 0h, so a current address read of the EEPROM array starts at address 0. When required, as part of a random read, the master must supply the 2 Word Address Bytes as shown in Figure 15.

In a random read operation, the slave byte in the “dummy write” portion must match the slave byte in the “read” section. That is if the random read is from the array the slave byte must be 1010111x in both instances. Similarly, for a random read of the Clock/Control Registers, the slave byte must be 1101111x in both places.

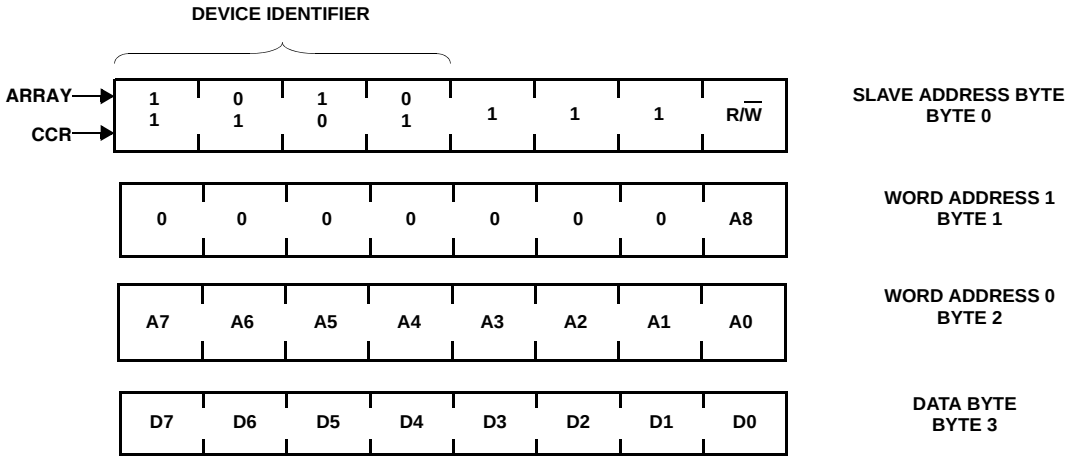


FIGURE 15. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES (16 BYTE PAGES)

Write Operations

Byte Write

For a write operation, the device requires the Slave Address Byte and the Word Address Bytes. This gives the master access to any one of the words in the array or CCR. (Note: Prior to writing to the CCR, the master must write a 02h, then 06h to the status register in two preceding operations to enable the write operation. See “Writing to the Clock/Control Registers” on page 12). Upon receipt of each address byte, the ISL12024IRTCZ responds with an acknowledge. After receiving both address bytes the ISL12024IRTCZ awaits the 8 bits of data. After receiving the 8 data bits, the ISL12024IRTCZ again responds with an acknowledge. The master then terminates the transfer by generating a stop condition. The ISL12024IRTCZ then begins an internal write cycle of the data to the nonvolatile memory. During the internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. The SDA output is at high impedance. (See Figure 16).

A write to a protected block of memory is ignored, but will still receive an acknowledge. At the end of the write command, the ISL12024IRTCZ will not initiate an internal write cycle, and will continue to ACK commands.

Byte writes to all of the non-volatile registers are allowed, except the DWAn registers which require multiple byte writes or page writes to trigger non-volatile writes. See “Device Operation” on page 12 for more information.

Page Write

The ISL12024IRTCZ has a page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit up to 15 more bytes to the memory array and up to 7 more bytes to the clock/control registers. The RTC registers require a page write (8 bytes), individual register writes are not allowed. (Note: Prior to writing to the CCR, the master must write a 02h, then 06h to the status register in two preceding operations to enable the write operation. See “Writing to the Clock/Control Registers” on page 12.)

After the receipt of each byte, the ISL12024IRTCZ responds with an acknowledge, and the address is internally incremented by one. The address pointer remains at the last address byte written. When the counter reaches the end of the page, it “rolls over” and goes back to the first address on the same page. This means that the master can write 16 bytes to a memory array page or 8 bytes to a CCR section starting at any location on that page. For example, if the master begins writing at location 10 of the memory and loads 15 bytes, then the first 6 bytes are written to addresses 10 through 15, and the last 6 bytes are written to columns 0 through 5. Afterwards, the address counter would point to location 6 on the page that was just written. If the master supplies more than the maximum bytes in a page, then the previously loaded data is over-written by the new data, one byte at a time (see Figure 17). The master terminates the Data Byte loading by issuing a stop condition, which causes the ISL12024IRTCZ to begin the non-volatile write cycle. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. See Figure 18 for the address, acknowledge and data transfer sequence.

Stops and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte and its associated ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte + ACK is sent, then the ISL12024IRTCZ resets itself without performing the write. The contents of the array are not affected.

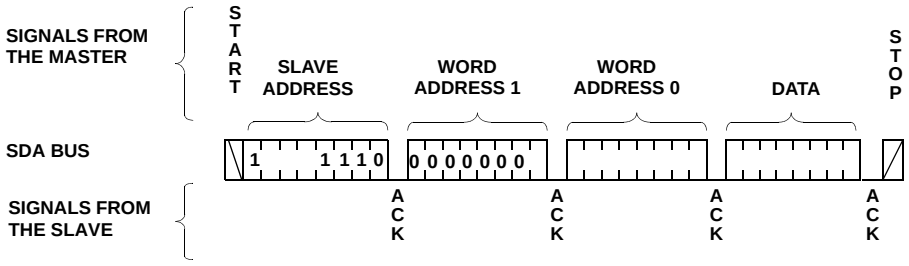


FIGURE 16. BYTE WRITE SEQUENCE

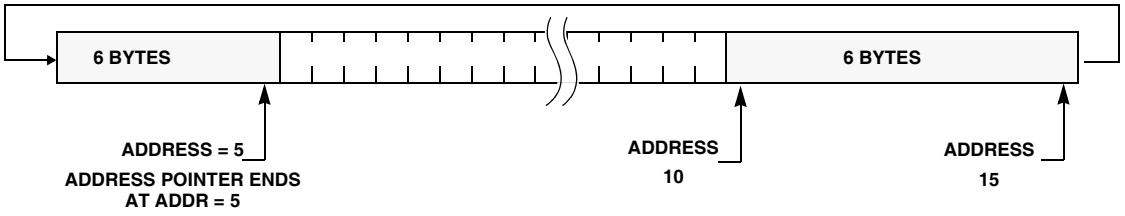


FIGURE 17. WRITING 12 BYTES TO A 16-BYTE MEMORY PAGE STARTING AT ADDRESS 10

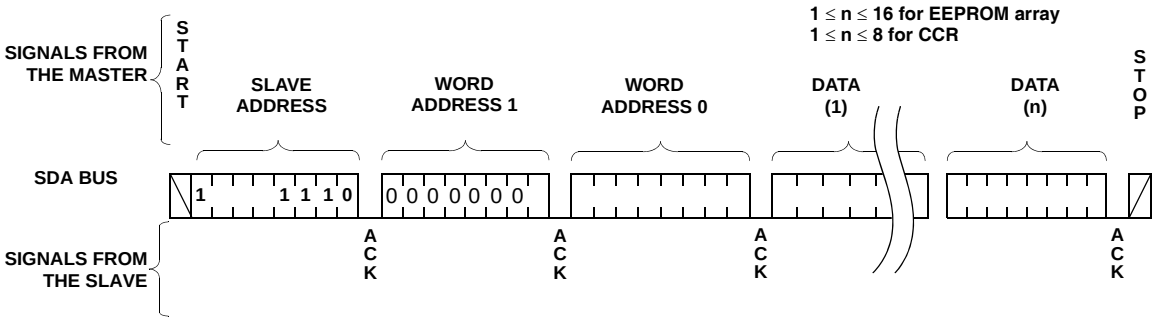


FIGURE 18. PAGE WRITE SEQUENCE

Acknowledge Polling

Disabling of the inputs during non-volatile write cycles can be used to take advantage of the 12ms (typ) write cycle time. Once the stop condition is issued to indicate the end of the master's byte load operation, the ISL12024IRTCZ initiates the internal non-volatile write cycle. Acknowledge polling can begin immediately. To do this, the master issues a start condition followed by the Memory Array Slave Address Byte for a write or read operation (AEh or AFh). If the ISL12024IRTCZ is still busy with the non-volatile write cycle then no ACK will be returned. When the ISL12024IRTCZ has completed the write operation, an ACK is returned and the host can proceed with the read or write operation. See the flow chart in Figure 20. Note: Do not use the CCR Slave byte (DEh or DFh) for Acknowledge Polling.

Read Operations

There are three basic read operations: Current Address Read, Random Read and Sequential Read.

CURRENT ADDRESS READ

Internally the ISL12024IRTCZ contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n + 1. On power-up, the 16-bit address is initialized to 00h. In this way, a current address read immediately after the power-on reset can download the entire contents of memory starting at the first location. Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the ISL12024IRTCZ issues an acknowledge, then transmits 8 data bits. The master terminates the read operation by not responding with an acknowledge during the ninth clock and issuing a stop condition. See Figure 19 for the address, acknowledge, and data transfer sequence.

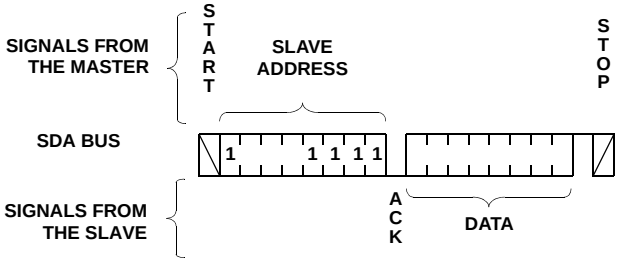


FIGURE 19. CURRENT ADDRESS READ SEQUENCE

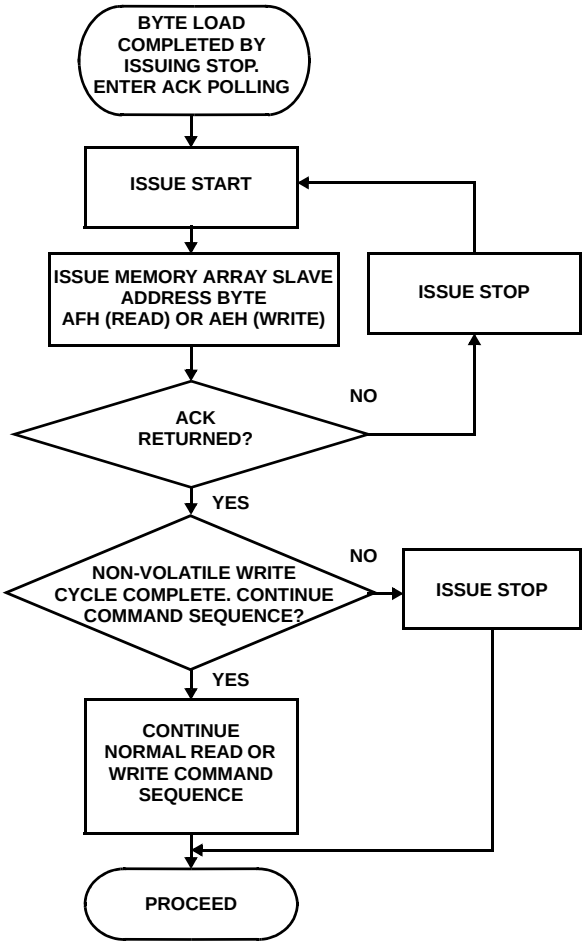


FIGURE 20. ACKNOWLEDGE POLLING SEQUENCE

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

RANDOM READ

Random read operations allow the master to access any location in the ISL12024IRTCZ. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to zero, the master must first perform a “dummy” write operation.

The master issues the start condition and the slave address byte, receives an acknowledge, then issues the word address bytes. After acknowledging receipt of each word address byte, the master immediately issues another start condition and the slave address byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the 8 -bit data word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. See Figure 21 for the address, acknowledge and data transfer sequence.

In a similar operation called “Set Current Address,” the device sets the address if a stop is issued instead of the second start shown in Figure 21. The ISL12024IRTCZ then goes into Standby Power Mode after the stop and all bus activity will be ignored until a start is detected. This operation loads the new address into the address counter. The next Current Address Read operation will read from the newly loaded address. This operation could be useful if the master knows the next address it needs to read, but is not ready for the data.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random address read. The first data byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through all page and column addresses, allowing the entire memory contents to be serially read during one operation. At the end of the address space the counter “rolls over” to the start of the address space and the ISL12024IRTCZ continues to output data for each acknowledge received. See Figure 22 for the acknowledge and data transfer sequence.

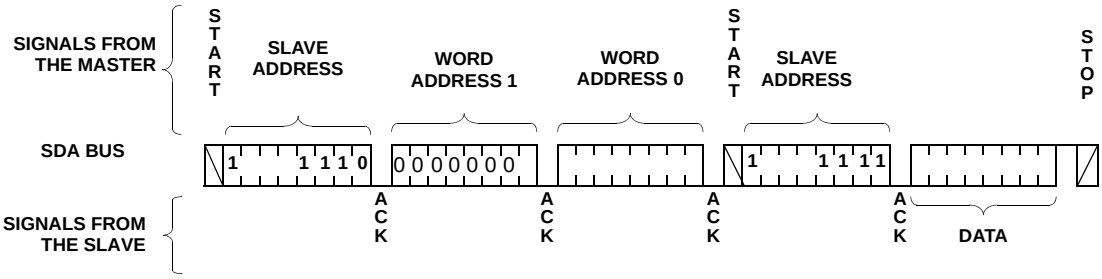


FIGURE 21. RANDOM ADDRESS READ SEQUENCE

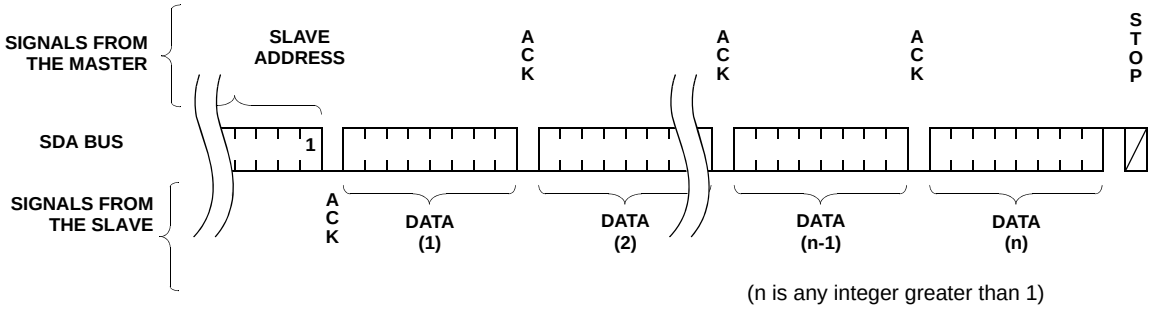


FIGURE 22. SEQUENTIAL READ SEQUENCE

Application Section

Crystal Oscillator and Temperature Compensation

Intersil has now integrated the oscillator compensation circuity on-chip, to eliminate the need for external components and adjust for crystal drift over-temperature and enable very high accuracy time keeping (<5ppm drift).

The Intersil RTC family uses an oscillator circuit with on-chip crystal compensation network, including adjustable load-capacitance. The only external component required is the crystal. The compensation network is optimized for operation with certain crystal parameters which are common in many of the surface mount or tuning-fork crystals available today. Table 6 summarizes these parameters.

Table 7 contains some crystal manufacturers and part numbers that meet the requirements for the Intersil RTC products.

The turnover-temperature in Table 6 describes the temperature where the apex of the of the drift vs temperature curve occurs. This curve is parabolic with the drift increasing as $(T-T0)^2$. For an Epson MC-405 device, for example, the turnover-temperature is typically +25°C, and a peak drift of >110ppm occurs at the temperature extremes of -40 and +85°C. It is possible to address this variable drift by adjusting the load capacitance of the crystal, which will result in predictable change to the crystal frequency. The Intersil RTC family allows this adjustment over-temperature since the devices include on-chip load capacitor trimming. This control is handled by the Analog Trimming Register, or ATR, which has 6-bits of control. The load capacitance range covered by the ATR circuit is approximately 3.25pF to 18.75pF, in 0.25pF increments. Note that actual capacitance would also include about 2pF of package related capacitance. In-circuit tests with commercially available crystals demonstrate that this range of capacitance allows frequency control from +80ppm to -34ppm, using a 12.5pF load crystal.

In addition to the analog compensation afforded by the adjustable load capacitance, a digital compensation feature is available for the Intersil RTC family. There are 3-bits known as the Digital Trimming Register or DTR, and they operate by adding or skipping pulses in the clock signal. The range provided is ±30ppm in increments of 10ppm. The default setting is 0ppm. The DTR control can be used for coarse adjustments of frequency drift over-temperature or for crystal initial accuracy correction.

A final application for the ATR control is in-circuit calibration for high accuracy applications, along with a temperature sensor chip. Once the RTC circuit is powered up with battery backup, the $\overline{IRQ}/F_{OUT}$ output is set at 32.768kHz and frequency drift is measured. The ATR control is then adjusted to a setting which minimizes drift. Once adjusted at a particular temperature, it is possible to adjust at other discrete temperatures for minimal overall drift, and store the resulting settings in the EEPROM. Extremely low overall temperature drift is possible with this method. The Intersil evaluation board contains the circuitry necessary to implement this control.

TABLE 6. CRYSTAL PARAMETERS REQUIRED FOR INTERSIL RTCs

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Frequency		32.768		kHz	
Frequency Tolerance			±100	ppm	Down to 20ppm if desired
Turnover-temperature	20	25	30	°C	Typically the value used for most crystals
Operating Temperature Range	-40		85	°C	
Parallel Load Capacitance		12.5		pF	
Equivalent Series Resistance			50	kΩ	For best oscillator performance

TABLE 7. CRYSTAL MANUFACTURERS

MANUFACTURER	PART NUMBER	TEMP RANGE (°C)	+25°C FREQUENCY TOLERANCE (PPM)
Citizen	CM201, CM202, CM200S	-40 to +85	±20
Epson	MC-405, MC-406	-40 to +85	±20
Raltron	RSM-200S-A or B	-40 to +85	±20
SaRonix	32S12A or B	-40 to +85	±20
Ecliptek	ECPSM29T-32.768K	-10 to +60	±20
ECS	ECX-306/ECX-306I	-10 to +60	±20
Fox	FSM-327	-40 to +85	±20

Layout Considerations

The crystal input at X1 has a very high impedance and will pick up high frequency signals from other circuits on the board. Since the X2 pin is tied to the other side of the crystal, it is also a sensitive node. These signals can couple into the oscillator circuit and produce double clocking or mis-clocking, seriously affecting the accuracy of the RTC. Care needs to be taken in layout of the RTC circuit to avoid noise pickup. Figure 23 is a suggested layout for the 8 Ld SOIC package.

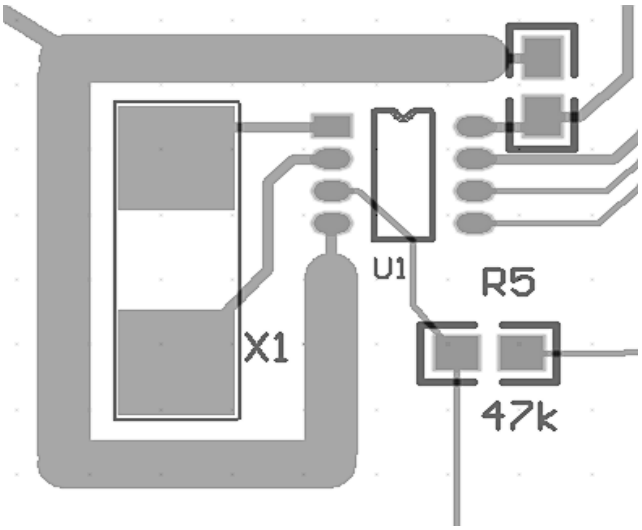


FIGURE 23. SUGGESTED LAYOUT FOR INTERSIL RTC IN 8 Ld SOIC PACKAGE

The X1 and X2 connections to the crystal are to be kept as short as possible. A thick ground trace around the crystal is advised to minimize noise intrusion, but ground near the X1 and X2 pins should be avoided as it will add to the load capacitance at those pins. Keep in mind these guidelines for other PCB layers in the vicinity of the RTC device. A small decoupling capacitor at the V_{DD} pin of the chip is mandatory, with a solid connection to ground.

The ISL12024IRTCZ product has a special consideration. The $\overline{IRQ}/F_{OUT}$ pin on the 8 Ld TDFN package is located next to the X2 pin. When this pin is used as a frequency output ($\overline{IRQ}/F_{OUT}$) and is set to 32.768kHz noise can couple to the X1 or X2 pins and cause double-clocking. The layout in Figure 23 minimizes this by running the $\overline{IRQ}/F_{OUT}$ output away from the X1 and X2 pins. Also, reducing the switching current at this pin by careful selection of the pull-up resistor value will reduce noise. Intersil suggests a minimum value of 5.1kΩ for 32.768kHz, and higher values (up to 20kΩ) for lower frequency $\overline{IRQ}/F_{OUT}$ outputs.

For other RTC products, the same rules stated above should be observed, but adjusted slightly since the packages and pinouts are different.

Oscillator Measurements

When a proper crystal is selected and the layout guidelines above are observed, the oscillator should start-up in most circuits in less than one second. Some circuits may take slightly longer, but startup should definitely occur in less than 5 seconds. When testing RTC circuits, the most common impulse is to apply a scope probe to the circuit at the X2 pin (oscillator output) and observe the waveform. DO NOT DO THIS! Although in some cases you may see a usable waveform, due to the parasitics (usually 10pF to ground) applied with the scope probe, there will be no useful information in that waveform other than the fact that the circuit is oscillating. The X2 output is sensitive to capacitive impedance so the voltage levels and the frequency will be affected by the parasitic elements in the scope probe. Applying a scope probe can possibly cause a faulty oscillator to start-up, hiding other issues (although in the Intersil RTCs, the internal circuitry assures startup when using the proper crystal and layout).

The best way to analyze the RTC circuit is to power it up and read the real-time clock as time advances, or if the chip has the $\overline{IRQ}/F_{OUT}$ output, look at the output of that pin on an oscilloscope (after enabling it with the control register, and using a pull-up resistor for an open-drain output). Alternatively, the ISL12024IRTCZ device has an $\overline{IRQ}/F_{OUT}$ output which can be checked by setting an alarm for each minute. Using the pulse interrupt mode setting, the once-per-minute interrupt functions as an indication of proper oscillation.

Backup Battery Operation

Many types of batteries can be used with the Intersil RTC products. 3.0V or 3.6V Lithium batteries are appropriate, and sizes are available that can power a Intersil RTC device for up

to 10 years. Another option is to use a super capacitor for applications where V_{DD} may disappear intermittently for short periods of time. Depending on the value of superconductor used, backup time can last from a few days to two weeks (with >1F). A simple silicon or Schottky barrier diode can be used in series with V_{DD} to charge the superconductor, which is connected to the V_{BAT} pin. Try to use Schottky diodes with very low leakages, <1µA desirable. Do not use the diode to charge a battery (especially lithium batteries!)

There are two possible modes for battery backup operation; Standard and Legacy Mode. In Standard Mode, there are no operational concerns when switching over to battery backup since all other devices functions are disabled. Battery drain is minimal in Standard Mode, and return to Normal V_{DD} powered operations is predictable. In Legacy Mode, the V_{BAT} pin can power the chip if the voltage is above V_{DD} and less than V_{TRIP}. In this mode, it is possible to generate alarm and communicate with the device, unless SBI = 1, but the supply current drain is much higher than the Standard Mode and backup time is reduced. In this case if alarms are used in backup mode, the $\overline{IRQ}/F_{OUT}$ pull-up resistor must be connected to V_{BAT} voltage source. During initial power-up the default mode is the Standard Mode.

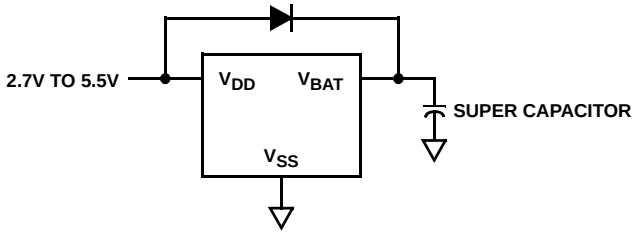


FIGURE 24. SUPER CAPACITOR CHARGING CIRCUIT

Alarm Operation Examples

Below are examples of both Single Event and periodic Interrupt Mode alarms.

EXAMPLE 1

Alarm0 set with single interrupt (IM = “0”)

A single alarm will occur on January 1 at 11:30am.

A. Set Alarm0 registers as follows:

ALARM0 REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
SCA0	0	0	0	0	0	0	0	0	00h	Seconds disabled
MNA0	1	0	1	1	0	0	0	0	B0h	Minutes set to 30, enabled
HRA0	1	0	0	1	0	0	0	1	91h	Hours set to 11, enabled
DTA0	1	0	0	0	0	0	0	1	81h	Date set to 1, enabled
MOA0	1	0	0	0	0	0	0	1	81h	Month set to 1, enabled
DWA0	0	0	0	0	0	0	0	0	00h	Day of week disabled

B. Also, the AL0E bit must be set as follows:

CONTROL REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
INT	0	0	1	0	0	0	0	0	x0h	Enable Alarm

After these registers are set, an alarm will be generated when the RTC advances to exactly 11:30am on January 1 (after seconds changes from 59 to 00) by setting the AL0 bit in the status register to “1” and also bringing the $\overline{IRQ}/F_{OUT}$ output low.

EXAMPLE 2

Pulsed interrupt once per minute (IM = “1”)

Interrupts at one minute intervals when the seconds register is at 30 seconds.

A. Set Alarm0 registers as follows:

ALARM0 REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
SCA0	1	0	1	1	0	0	0	0	B0h	Seconds set to 30, enabled
MNA0	0	0	0	0	0	0	0	0	00h	Minutes disabled
HRA0	0	0	0	0	0	0	0	0	00h	Hours disabled
DTA0	0	0	0	0	0	0	0	0	00h	Date disabled
MOA0	0	0	0	0	0	0	0	0	00h	Month disabled
DWA0	0	0	0	0	0	0	0	0	00h	Day of week disabled

B. Set the Interrupt register as follows:

CONTROL REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
INT	1	0	1	0	0	0	0	0	x0h	Enable Alarm and Int Mode

Once the registers are set, the following waveform will be seen at $\overline{IRQ}/F_{OUT}$:

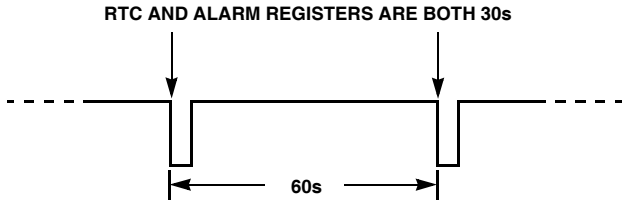


FIGURE 25.

Note that the status register AL0 bit will be set each time the alarm is triggered, but does not need to be read or cleared.

I^2C Communications During Battery Backup

Operation in Battery Backup Mode is affected by the BSW and SBIB bits as described earlier. These bits allow flexible operation of the serial bus and EEPROM in Battery Backup Mode, but certain operational details need to be clear before utilizing the different modes. Table 8 describes four different modes possible with using the BSW and SBIB bits, and how they affect the serial interface and battery backup operation.

- Mode A - In this mode, selection bits indicate a Standard Mode switchover combined with I^2C operation in Battery Backup Mode. When the V_{DD} voltage drops below the lower of V_{TRIP} or V_{BAT}, then the device will enter Battery Backup Mode. If the microcontroller and bus pull-ups are also powered by the battery, then the ISL12024IRTCZ can communicate in Battery Backup Mode.
- Mode B - In this mode selection, bits indicate Legacy Mode switchover combined with I^2C operation in Battery Backup Mode. When the V_{DD} voltage drops below V_{BAT}, the device will enter Battery Backup Mode. If the microcontroller and bus pull-ups are also powered by the battery, then the ISL12024IRTCZ can communicate in Battery Backup Mode. This mode places the ISL12024IRTCZ device in the same operating mode as the X1226 legacy device.
- Mode C - This mode combines Standard Mode battery switchover with no I^2C operation in Battery Backup Mode. When the V_{DD} voltage drops below the lower of V_{TRIP} or V_{BAT}, then the device will enter Battery Backup Mode and the I^2C interface will be disabled, minimizing V_{BAT} current drain.
- Mode D - This mode combines Legacy Mode battery switchover with no I^2C operation in Battery Backup Mode. When the V_{DD} voltage drops below V_{BAT}, the device will enter Battery Backup Mode and the I^2C interface will be disabled, minimizing V_{BAT} current drain.

Note that the $\overline{IRQ}/F_{OUT}$ open drain output pin is active in battery backup for all modes, allowing clocking of devices while in Battery Backup Mode. The pull-up on the pin will need to go to V_{BAT}, and thus battery mode current draw will increase accordingly.

TABLE 8.

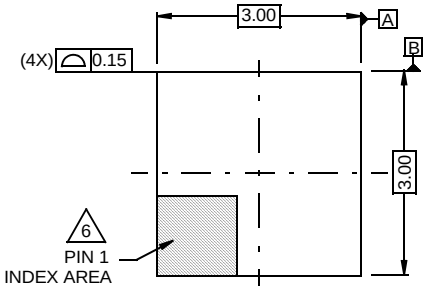
MODE	SBIB BIT	BSW BIT	V_{BAT} SWITCHOVER VOLTAGE	I^2C ACTIVE IN BATTERY BACKUP?	EEPROM WRITE/READ IN BATTERY BACKUP?	FREQ/IRQ ACTIVE?	NOTES
A	0	0	Standard Mode, V_{TRIP} = 2.2V typ	Yes	NO	YES, needs pull-up to V_{BAT}	V_{BAT} switchover at lower of V_{BAT} or V_{TRIP}. Pull-ups needed on I^2C to V_{BAT} to operate in Battery Backup.
B (X1226 Mode)	0	1	Legacy Mode, $V_{DD} < V_{BAT}$	Yes	NO	YES, needs pull-up to V_{BAT}	V_{BAT} switchover at $<V_{DD}$. Pull-ups needed on I^2C to V_{BAT} to operate in Battery Backup.
C	1	0	Standard Mode, V_{TRIP} = 2.2V typ	NO	NO	YES, needs pull-up to V_{BAT}	V_{BAT} switchover at lower of V_{BAT} or V_{TRIP}.
D	1	1	Legacy Mode, $V_{DD} < V_{BAT}$	NO	NO	YES, needs pull-up to V_{BAT}	V_{BAT} switchover at $<V_{DD}$.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

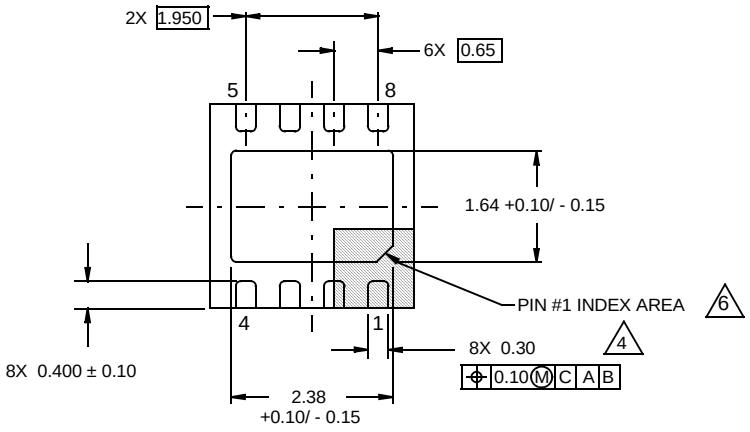
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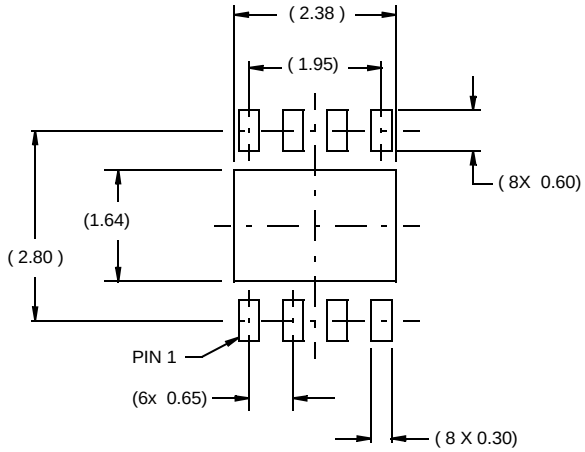
Package Outline Drawing
L8.3x3I
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 1 6/09



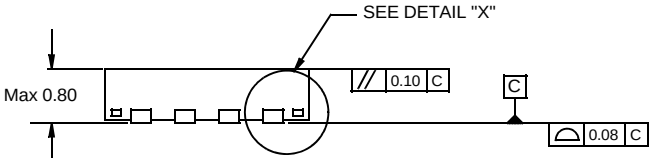
TOP VIEW



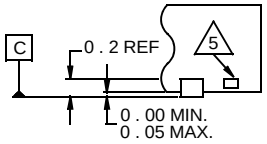
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.