CY7C68000A

MoBL-USB™ TX2 USB 2.0 UTMI Transceiver

MoBL-USB™ TX2 Features

- UTMI-compliant/USB 2.0 certified for device operation
- Operates in both USB 2.0 high-speed (HS), 480 Mbits/second, and full-speed (FS), 12 Mbits/second
- Optimized for seamless interface with Intel® Monahans Applications Processors
- Tri-state Mode allows sharing of UTMI bus with other devices
- Serial-to-parallel and parallel-to-serial conversions
- 8-bit unidirectional, 8-bit bidirectional, or 16-bit bidirectional external data interface
- Synchronous field and EOP detection on receive packets
- Synchronous field and EOP generation on transmit packets
- Data and clock recovery from the USB serial stream
- Bit stuffing/unstuffing; bit stuff error detection
- Staging register to manage data rate variation due to bit stuffing/unstuffing
- 16-bit 30 MHz and 8-bit 60 MHz parallel interface
- Ability to switch between FS and HS terminations and signaling
- Supports detection of USB reset, suspend, and resume
- Supports HS identification and detection as defined by the USB 2.0 Specification
- Supports transmission of resume signaling
- 3.3V operation
- Two package options: 56-pin QFN and 56-pin VFBGA
- All required terminations, including 1.5 Kohm pull up on DPLUS, are internal to chip
- Supports USB 2.0 test modes

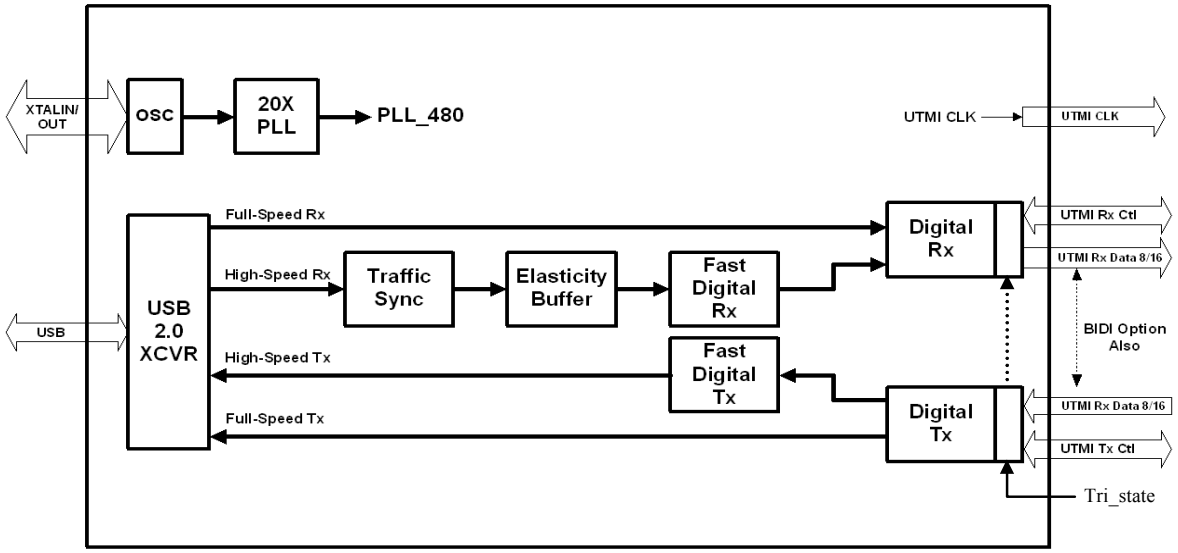
The Cypress MoBL-USB™ TX2 is a Universal Serial Bus (USB) specification revision 2.0 transceiver, serial/deserializer, to a parallel interface of either 16 bits at 30 MHz or eight bits at 60 MHz. The MoBL-USB TX2 provides a high-speed physical layer interface that operates at the maximum allowable USB 2.0 bandwidth. This allows the system designer to keep the complex high-speed analog USB components external to the digital ASIC which decreases development time and associated risk. A standard interface is provided that is USB 2.0 certified and is compliant with Transceiver Macrocell Interface (UTMI) specification version 1.05 dated 3/29/2001.

This product is also optimized to seamlessly interface with Monahans -P & -L applications processors. It has been characterized by Intel and is recommended as the USB 2.0 UTMI transceiver of choice for its Monahans processors. It is also capable of tri-stating the UTMI bus while suspended to allow the bus to be shared with other devices.

Two packages are defined for the family: 56-pin QFN and 56-pin VFBGA.

The functional block diagram is shown below.

Block Diagram



Applications

Mobile Applications

- Smart Phones
- PDA Phones
- Gaming Phones
- MP3 players
- Portable Media Players (PMP)
- GPS Tracking Devices

Consumer Applications

- Cameras
- Scanners
- DSL Modems
- Memory Card Readers

Non-Consumer Applications

- Networking
- Wireless LAN
- Home PNA

Functional Overview

The functionality of this chip is described in the sections below.

USB Signaling Speed

The MoBL-USB TX2 operates at two of the rates defined in the USB Specification 2.0, dated April 27, 2000.

- Full speed, with a signaling bit rate of 12 Mbps
- High speed, with a signaling bit rate of 480 Mbps

The MoBL-USB TX2 does not support the low-speed (LS) signaling rate of 1.5 Mbps.

Transceiver Clock Frequency

The MoBL-USB TX2 has an on-chip oscillator circuit that uses an external 24 MHz (±100-ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 500 μW drive level
- 27–33 pF (5% tolerance) load capacitors

An on-chip phase-locked loop (PLL) multiplies the 24 MHz oscillator up to 30/60 MHz, as required by the transceiver parallel data bus. The default UTMI interface clock (CLK) frequency is determined by the DataBus16_8 pin.

Buses

The two packages allow for a 8- or 16-bit bidirectional data bus for data transfers to a controlling unit.

Suspend and Tri-state Modes

When the MoBL-USB TX2 is not in use, the processor can reduce power consumption by putting it into Suspend mode using the Suspend pin.

While in Suspend mode, Tri-state mode may be enabled, which tri-states all outputs and IO's, allowing the UTMI interface pins to be shared with other devices. This is valuable in mobile handset applications, where GPIO's are at a premium. The outputs and IO's will be tri-stated ~50ns following Tri-state Mode being enabled, and will be driven ~50ns following Tri-state Mode being disabled. All inputs must not be left floating while in Tri-state Mode.

When resuming after a suspend, the PLL stabilizes approximately 200 μs after the suspend pin goes high.

Reset Pin

An input pin (Reset) resets the chip. This pin has hysteresis and is active HIGH according to the UTMI specification. The internal PLL stabilizes approximately 200 μs after V_{CC} has reached 3.3 volts.

Line State

The Line State output pins LineState[1:0] are driven by combinational logic and may be toggling between the 'J' and the 'K' states. They are synchronized to the CLK signal for a valid signal. On the CLK edge the state of these lines reflect the state of the USB data lines. Upon the clock edge the '0' bit of the LineState pins is the state of the DPLUS line and the '1' bit of LineState is the DMINUS line. When synchronized, the set-up and hold timing of the LineState is identical to the parallel data bus.

Full-speed vs. High-speed Select

The FS vs. HS is done through the use of both XcvrSelect and the TermSelect input signals. The TermSelect signal enables the 1.5 Kohm pull up on to the DPLUS pin. When TermSelect is driven LOW, a SE0 is asserted on the USB providing the HS termination and generating the HS Idle state on the bus. The XcvrSelect signal is the control that selects either the FS transceivers or the HS transceivers. By setting this pin to a'0' the HS transceivers are selected and by setting this bit to a'1' the FS transceivers are selected.

Operational Modes

The operational modes are controlled by the OpMode signals. The **OpMode** signals are capable of inhibiting normal operation of the transceiver and evoking special test modes. These modes take effect immediately and take precedence over any pending data operations. The transmission data rate when in **OpMode** depends on the state of the **XcvrSelect** input.

OpMode[1:0]	Mode	Description
00	0	Normal operation
01	1	Non-driving
10	2	Disable Bit Stuffing and NRZI encoding
11	3	Reserved

Mode 0 allows the transceiver to operate with normal USB data decoding and encoding.

Mode 1 allows the transceiver logic to support a soft disconnect feature that tri-states both the HS and FS transmitters, and removes any termination from the USB, making it appear to an upstream port that the device has been disconnected from the bus.

Mode 2 disables Bit Stuff and NRZI encoding logic so '1's loaded from the data bus becomes 'J's on the **DPLUS**/**DMINUS** lines and '0's become 'K's.

DPLUS/DMINUS Impedance Termination

The CY7C68000A does not require external resistors for USB data line impedance termination or an external pull up resistor on the DPLUS line. These resistors are incorporated into the part. They are factory trimmed to meet the requirements of USB 2.0. Incorporating these resistors also reduces the pin count on the part.

Pin Assignments

The following pages illustrate the individual pin diagrams that are available in the 56-pin QFN and 56-pin VFBGA packages. The packages offered use either an 8-bit (60 MHz) or 16-bit (30 MHz) bus interface.

Figure 1. CY7C68000A 56-pin QFN Pin Assignment

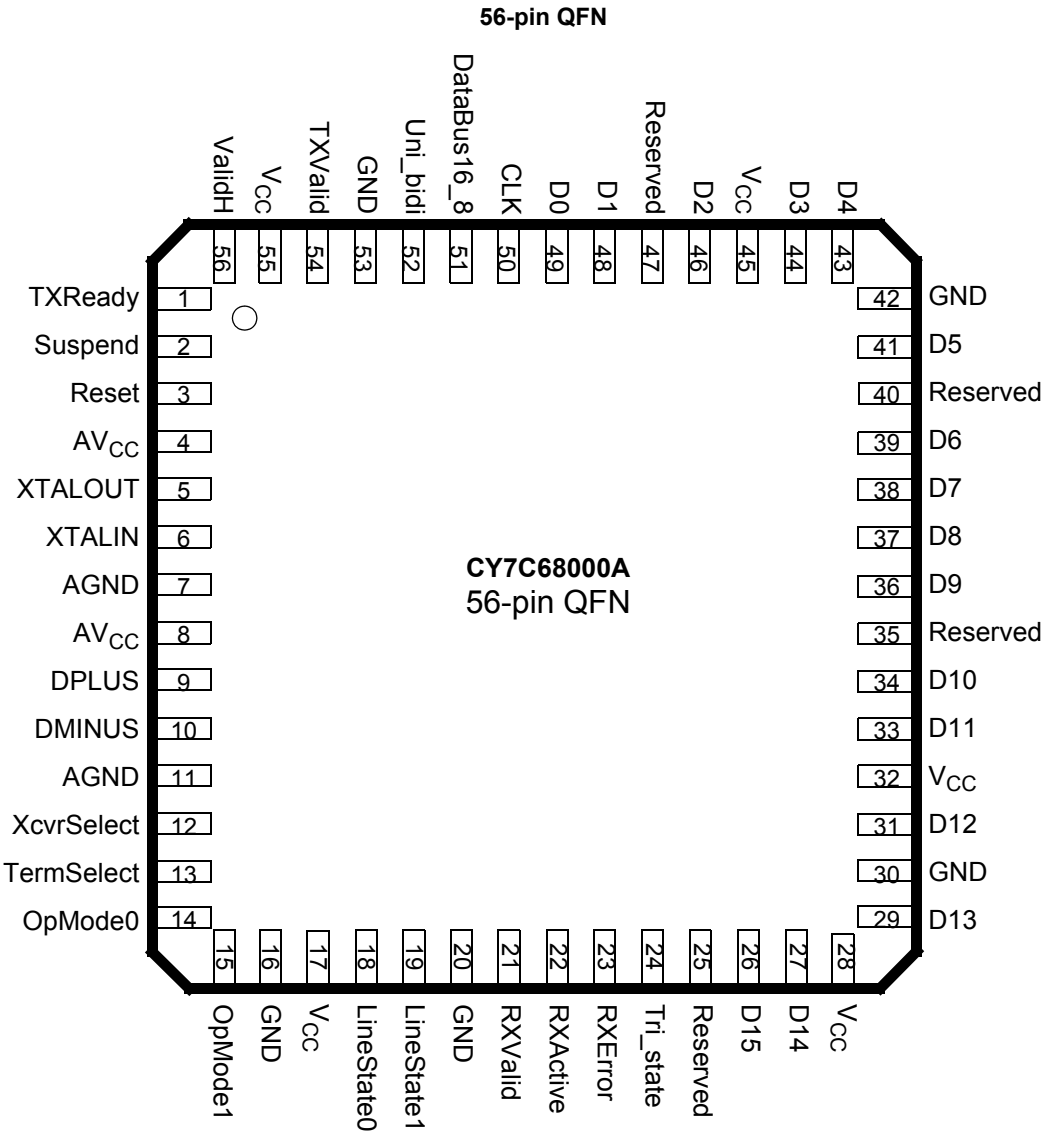
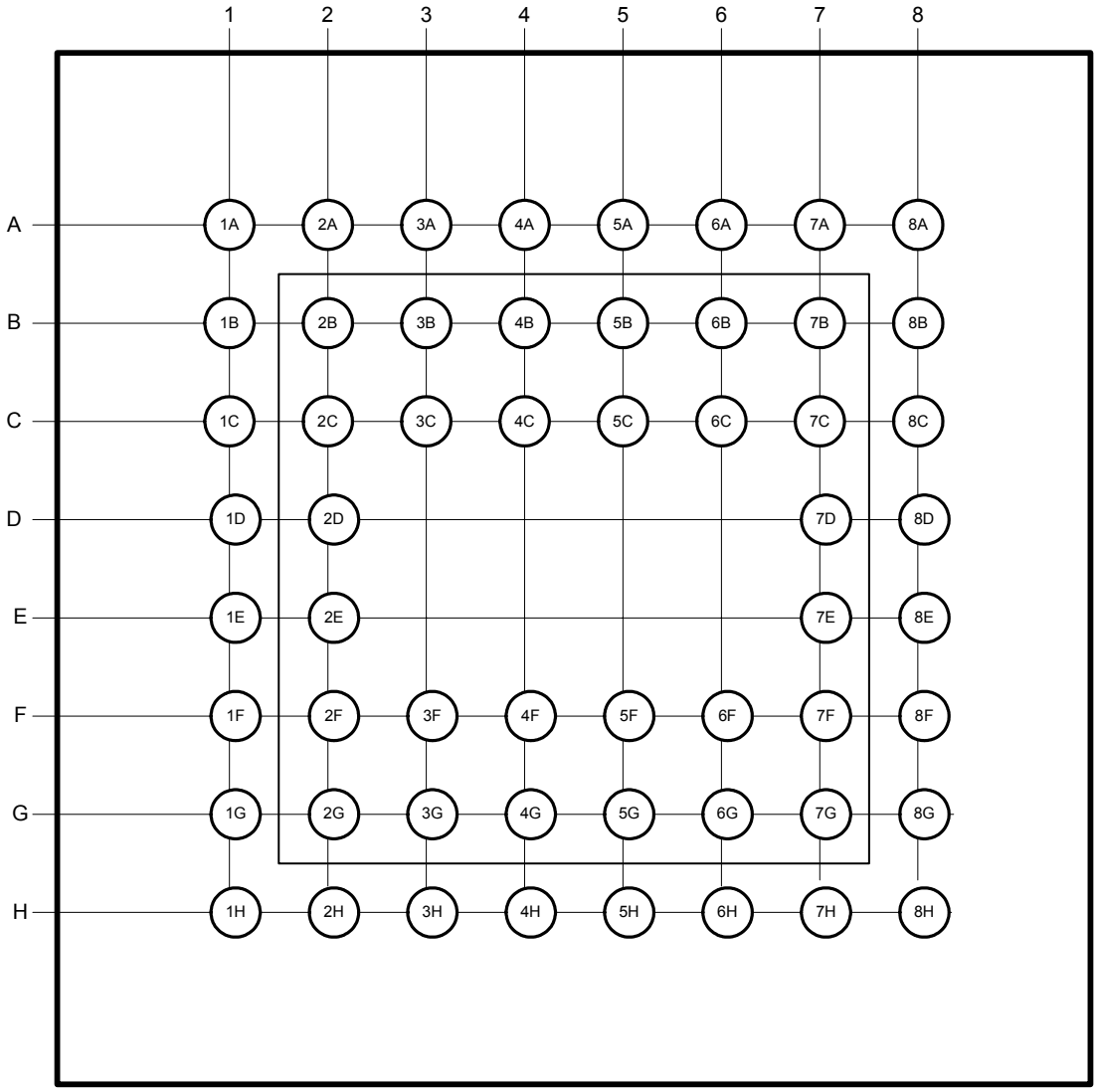


Figure 2. CY7C68000A 56-pin VFBGA Pin Assignment



CY7C68000A Pin Descriptions

Table 1. Pin Descriptions[1]

QFN	VFBGA	Name	Type	Default	Description
4	H1	AVCC	Power	N/A	**Analog V_{CC}** This signal provides power to the analog section of the chip.
8	H5	AVCC	Power	N/A	**Analog V_{CC}** This signal provides power to the analog section of the chip.
7	H4	AGND	Power	N/A	**Analog Ground** Connect to ground with as short a path as possible.
11	H8	AGND	Power	N/A	**Analog Ground** Connect to ground with as short a path as possible.
9	H6	DPLUS	I/O/Z	Z	**USB DPLUS Signal** Connect to the USB DPLUS signal.
10	H7	DMINUS	I/O/Z	Z	**USB DMINUS Signal** Connect to the USB DMINUS signal.

Note
1. Unused inputs should not be left floating. Tie either HIGH or LOW as appropriate. Outputs that are three-statable should only be pulled up or down to ensure signals at power-up and in standby.

Table 1. Pin Descriptions[1] (continued)

QFN	VFBGA	Name	Type	Default	Description
49	G8	D0	I/O		**Bidirectional Data Bus** This bidirectional bus is used as the entire data bus in the 8-bit bidirectional mode or the least significant eight bits in the 16-bit mode. Under the 8-bit unidirectional mode, these bits are used as inputs for data, selected by the RxValid signal.
48	G7	D1	I/O		
46	G5	D2	I/O		
44	G3	D3	I/O		
43	G2	D4	I/O		
41	F8	D5	I/O		
39	F6	D6	I/O		
38	F5	D7	I/O		
37	F4	D8	I/O		**Bidirectional Data Bus** This bidirectional bus is used as the upper eight bits of the data bus when in the 16-bit mode, and not used when in the 8-bit bidirectional mode. Under the 8-bit unidirectional mode these bits are used as outputs for data, selected by the TxValid signal.
36	F3	D9	I/O		
34	F1	D10	I/O		
33	G4	D11	I/O		
31	E1	D12	I/O		
29	D8	D13	I/O		
27	G1	D14	I/O		
26	E2	D15	I/O		
50	A1	CLK	Output		**Clock** This output is used for clocking the receive and transmit parallel data on the D[15:0] bus.
3	B2	Reset	Input	N/A	**Active HIGH Reset** Resets the entire chip. This pin can be tied to V_{CC} through a 0.1-µF capacitor and to GND through a 100 K resistor for a 10-ms RC time constant.
12	B3	XcvrSelect	Input	N/A	**Transceiver Select** This signal selects between the Full-Speed (FS) and the High-Speed (HS) transceivers: 0: HS transceiver enabled 1: FS transceiver enabled
13	B4	TermSelect	Input	N/A	**Termination Select** This signal selects between the between the Full Speed (FS) and the High Speed (HS) terminations: 0: HS termination 1: FS termination
2	B1	Suspend	Input	N/A	**Suspend** Places the CY7C68000A in a mode that draws minimal power from supplies. Shuts down all blocks not necessary for Suspend/Resume operations. While suspended, **TermSelect** must always be in FS mode to ensure that the 1.5 Kohm pull up on DPLUS remains powered. 0: CY7C68000A circuitry drawing suspend current 1: CY7C68000A circuitry drawing normal current
24	B8	Tri_state	Input		**Tri-state Mode Enable** Places the CY7C68000A into Tri-state mode which tri-states all outputs and IO's. Tri-state Mode can only be enabled while suspended. 0: Disables Tri-state Mode 1: Enables Tri-state Mode
19	C2	LineState1	Output		**Line State** These signals reflect the current state of the single-ended receivers. They are combinatorial until a "usable" CLK is available then they are synchronized to CLK. They directly reflect the current state of the DPLUS (LineState0) and DMINUS (LineState1). D– D+ Description 0 0 0: SE0 0 1 1: 'J' State 1 0 2: 'K' State 1 1 3: SE1

Table 1. Pin Descriptions[1] (continued)

QFN	VFBGA	Name	Type	Default	Description
18	C1	LineState0	Output		**Line State** These signals reflect the current state of the single-ended receivers. They are combinatorial until a 'usable' CLK is available then they are synchronized to CLK. They directly reflect the current state of the DPLUS (LineState0) and DMINUS (LineState1). D– D+ Description 00–0: SE0 01–1: 'J' State 10–2: 'K' State 11–3: SE1
15	B6	OpMode1	Input		**Operational Mode** These signals select among various operational modes. 10 Description 00–0: Normal Operation 01–1: Non-driving 10–2: Disable Bit Stuffing and NRZI encoding 11–3: Reserved
14	B5	OpMode0	Input		**Operational Mode** These signals select among various operational modes. 10 Description 00–0: Normal Operation 01–1: Non-driving 10–2: Disable Bit Stuffing and NRZI encoding 11–3: Reserved
54	A5	TXValid	Input		**Transmit Valid** This signal indicates that the data bus is valid. The assertion of Transmit Valid initiates SYNC on the USB. The negation of Transmit Valid initiates EOP on the USB. The start of SYNC must be initiated on the USB no less than one or no more that two CLKs after the assertion of TXValid. In HS (XcvrSelect = 0) mode, the SYNC pattern must be asserted on the USB between 8- and 16-bit times after the assertion of TXValid is detected by the Transmit State Machine. In FS (Xcvr = 1), the SYNC pattern must be asserted on the USB no less than one or more than two CLKs after the assertion of TXValid is detected by the Transmit State Machine.
1	A8	TXReady	Output		**Transmit Data Ready** If TXValid is asserted, the SIE must always have data available for clocking in to the TX Holding Register on the rising edge of CLK. If TXValid is TRUE and TXReady is asserted at the rising edge of CLK, the CY7C68000A will load the data on the data bus into the TX Holding Register on the next rising edge of CLK. At that time, the SIE should immediately present the data for the next transfer on the data bus.
21	A4	RXValid	Output		**Receive Data Valid** This signal indicates that the **DataOut** bus has valid data. The Receive Data Holding Register is full and ready to be unloaded. The SIE is expected to latch the **DataOut** bus on the clock edge.
22	B7	RXActive	Output		**Receive Active** This signal indicates that the receive state machine has detected SYNC and is active. RXActive is negated after a bit stuff error or an EOP is detected.
23	A6	RXError	Output		**Receive Error** 0 Indicates no error. 1 Indicates that a receive error has been detected.

Table 1. Pin Descriptions[1] (continued)

QFN	VFBGA	Name	Type	Default	Description
56	A7	ValidH	I/O		**ValidH** This signal indicates that the high-order eight bits of a 16-bit data word presented on the **Data** bus are valid. When **DataBus16_8** = 1 and **TXValid** = 0, **ValidH** is an output, indicating that the high-order receive data byte on the **Data** bus is valid. When **DataBus16_8** = 1 and **TXValid** = 1, **ValidH** is an input and indicates that the high-order transmit data byte, presented on the **Data** bus by the transceiver, is valid. When **DataBus16_8** = **0, ValidH** is undefined. The status of the receive low-order data byte is determined by **RXValid** and are present on D0–D7.
51	A2	DataBus16_8	Input		**Data Bus 16_8** This signal selects between 8- and 16-bit data transfers. 1–16-bit data path operation enabled. CLK = 30 MHz. 0–8-bit data path operation enabled. When Uni_Bidi = 0, D[8:15] are undefined. When Uni_Bidi =1, D[0:7] are valid on TxValid and D[8:15] are valid on RxValid. CLK = 60 MHz Note: **DataBus16_8** is static after Power-on Reset (POR) and is only sampled at the end of Reset.
6	H3	XTALIN	Input	N/A	**Crystal Input** Connect this signal to a 24 MHz parallel-resonant, fundamental mode crystal and 20 pF capacitor to GND. It is also correct to drive XTALIN with an external 24 MHz square wave derived from another clock source.
5	H2	XTALOUT	Output	N/A	**Crystal Output** Connect this signal to a 24 MHz parallel-resonant, fundamental mode crystal and 30 pF (nominal) capacitor to GND. If an external clock is used to drive XTALIN, leave this pin open.
52	A3	Uni_Bidi	Input		**Driving this pin HIGH enables the unidirectional mode when the 8-bit interface is selected**. Uni_Bidi is static after power-on reset (POR).
55	C6	V_{CC}	Power		V_{CC}. Connect to 3.3V power source.
17	C7	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
28	D7	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
32	E7	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
45	E8	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
53	C4	GND	Ground	N/A	Ground.
16	C5	GND	Ground	N/A	Ground.
20	C3	GND	Ground	N/A	Ground.
30	D1	GND	Ground	N/A	Ground.
42	D2	GND	Ground	N/A	Ground.
47	G6	Reserved	INPUT		Connect pin to Ground.
40	F7	Reserved	INPUT		Connect pin to Ground.
35	F2	Reserved	INPUT		Connect pin to Ground.
25	C8	Reserved	INPUT		Connect pin to Ground.

Absolute Maximum Ratings

Storage Temperature .....–65°C to +150°C
Ambient Temperature with Power Supplied .....0°C to +70°C
Supply Voltage to Ground Potential .....–0.5V to +4.0V
DC Input Voltage to Any Input Pin ..... 5.25 V
DC Voltage Applied to Outputs in High-Z State ..... –0.5V to V_{CC} + 0.5V
Power Dissipation .....630 mW
Static Discharge Voltage .....>2000V
Max Output Current, per IO pin ..... 4 mA
Max Output Current, all 21–IO pins .....84 mA

Operating Conditions

T_A (Ambient Temperature Under Bias) ..... 0°C to +70°C
Supply Voltage .....+3.0V to +3.6V
Ground Voltage 0V
F_{OSC} (Oscillator or Crystal Frequency) ... 24 MHz ± 100 ppm ..... Parallel Resonant

DC Characteristics

Table 2. DC Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.0	3.3	3.6	V
V_{IH}	Input High Voltage		2		5.25	V
V_{IL}	Input Low Voltage		–0.5		0.8	V
I_I	Input Leakage Current	0< V_{IN} < V_{CC}			±10	µA
V_{OH}	Output Voltage High	I_{OUT} = 4 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OUT} = –4 mA			0.4	V
I_{OH}	Output Current High				4	mA
I_{OL}	Output Current Low				4	mA
C_{IN}	Input Pin Capacitance	Except DPLUS/DMINUS/CLK			10	pF
		DPLUS/DMINUS/CLK			15	pF
C_{LOAD}	Maximum Output Capacitance	Output pins			30	pF
I_{SUSP}	Suspend Current	Connected[2]		228	273	µA
		Disconnected[2]		8	35	µA
I_{CC}	Supply Current HS Mode	Normal operation OPMOD[1:0] = 00			175	mA
I_{CC}	Supply Current FS Mode	Normal operation OPMOD[1:0] = 00			90	mA
t_{RESET}	Minimum Reset time		1.9			ms

USB 2.0 Transceiver

USB 2.0-compliant in FS and HS modes.

Note
2. Connected to the USB includes 1.5 Kohm internal pull up. Disconnected has the 1.5 Kohm internal pull up excluded.

AC Electrical Characteristics

USB 2.0 Transceiver

USB 2.0 certified in FS and HS.

Timing Diagram

HS/FS Interface Timing–60 MHz

Figure 3. 60-MHz Interface Timing Constraints

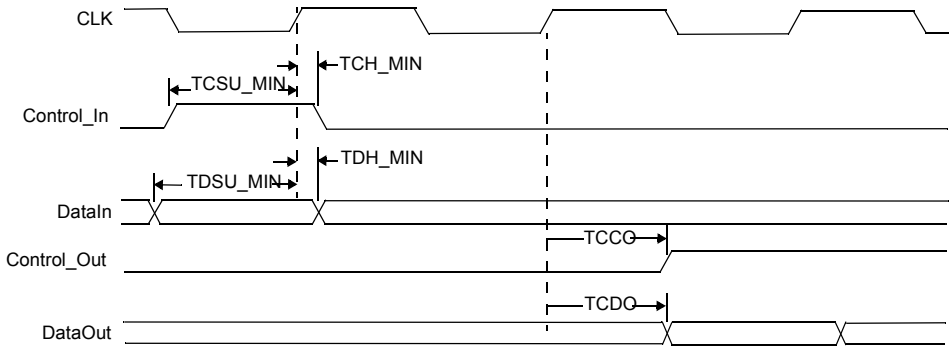


Table 3. 60-MHz Interface Timing Constraints Parameters

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
T_{CSU_MIN}	Minimum set-up time for TXValid	4			ns	
T_{CH_MIN}	Minimum hold time for TXValid	1			ns	
T_{DSU_MIN}	Minimum set-up time for Data (transmit direction)	4			ns	
T_{DH_MIN}	Minimum hold time for Data (transmit direction)	1			ns	
T_{CCO}	Clock to Control out time for TXReady, RXValid, RXActive and RXError	1		8	ns	
T_{CDO}	Clock to Data out time (Receive direction)	1		8	ns	

HS/FS Interface Timing–30 MHz

Figure 4. 30-MHz Timing Interface Timing Constraints

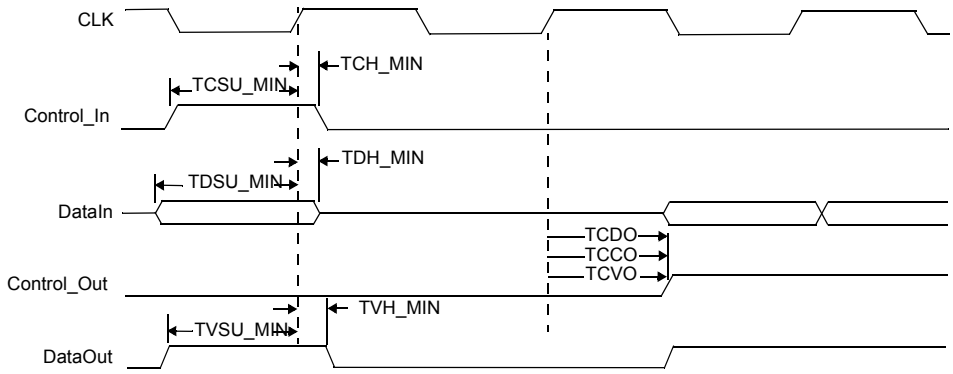


Table 4. 30 MHz Timing Interface Timing Constraints Parameters

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
T_{CSU_MIN}	Minimum set-up time for TXValid	16			ns	
T_{CH_MIN}	Minimum hold time for TXValid	1			ns	
T_{DSU_MIN}	Minimum set-up time for Data (Transmit direction)	16			ns	
T_{DH_MIN}	Minimum hold time for Data (Transmit direction)	1			ns	
T_{CCO}	Clock to Control Out time for TXReady, RXValid, RXActive and RXError	1		20	ns	
T_{CDO}	Clock to Data out time (Receive direction)	1		20	ns	
T_{VSU_MIN}	Minimum set-up time for ValidH (transmit Direction)	16			ns	
T_{VH_MIN}	Minimum hold time for ValidH (Transmit direction)	1			ns	
T_{CVO}	Clock to ValidH out time (Receive direction)	1		20	ns	

Figure 5. Tri-state Mode Timing Constraints

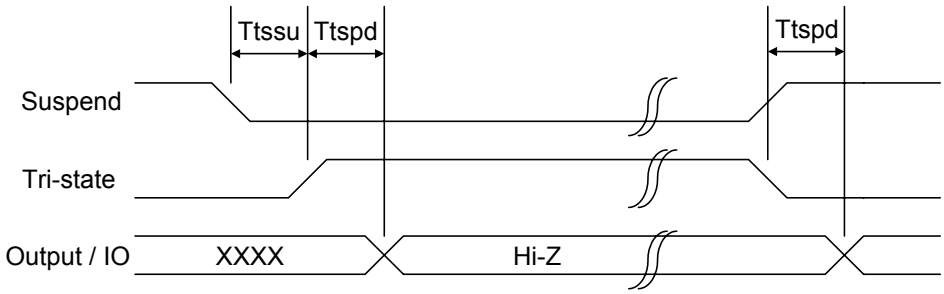


Table 5. Tri-state Mode Timing Constraints Parameters

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
T_{tssu}	Minimum set-up time for Tri-state	0			ns	
T_{tspd}	Propagation Delay for Tri-State mode			50	ns	

Ordering Information

Table 6. Ordering Information

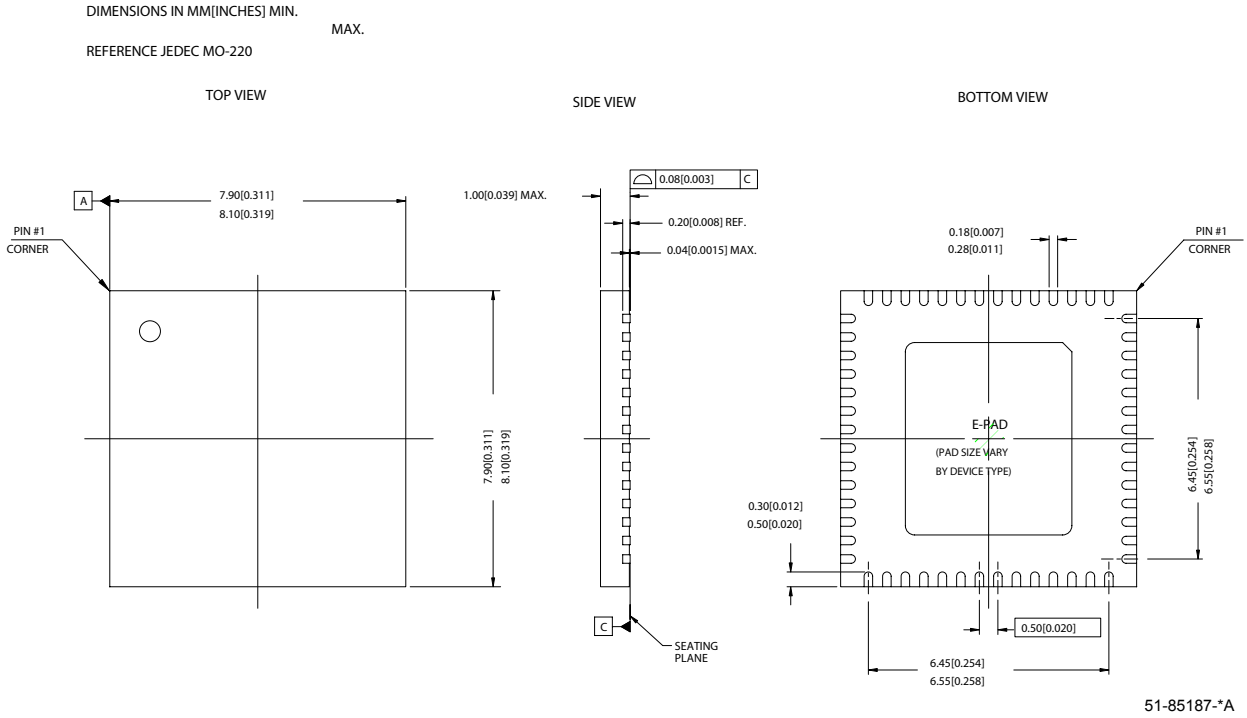
Ordering Code	Package Type
CY7C68000A-56LFXC	56 QFN
CY7C68000A-56BAXC	56 VFBGA
CY3683	MoBL-USB TX2 Development Board

Package Diagrams

The MoBL-USB TX2 is available in two packages:

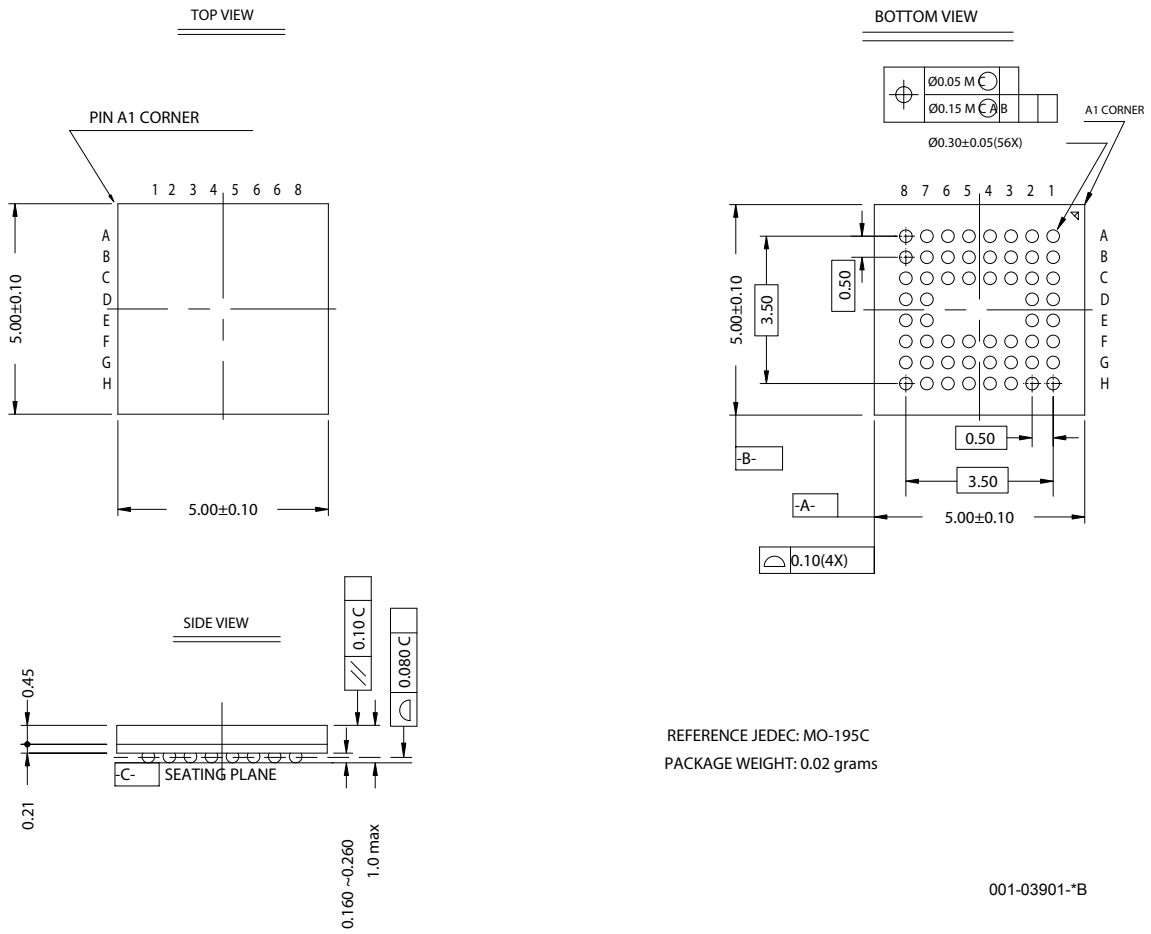
- 56-pin QFN
- 56-pin VFBGA

Figure 6. 56-Lead Quad Flatpack No Lead Package 8 x 8 mm (Sawn Version) LS56B



Package Diagrams (continued)

Figure 7. 56 VFBGA (5 x 5 x 1.0 mm) 0.50 Pitch, 0.30 Ball BZ56



PCB Layout Recommendations[3]

The following recommendations must be followed to ensure reliable high-performance operation.

- At least a four-layer impedance controlled board is required to maintain signal quality
- Specify impedance targets (ask your board vendor what they can achieve)
- To control impedance, maintain trace widths and trace spacing to within written specifications
- Minimize stubs to minimize reflected signals
- Connections between the USB connector shell and signal ground must be done near the USB connector
- Bypass/flyback capacitors on VBus, near the connector, are recommended
- DPLUS and DMINUS trace lengths must be kept to within 2 mm of each other in length, with preferred length of 20–30 mm
- Maintain a solid ground plane under the DPLUS and DMINUS traces. Do not allow the plane to be split under these traces
- It is best to have no vias placed on the DPLUS or DMINUS trace routing
- Isolate the DPLUS and DMINUS traces from all other signal traces by no less than 10 mm

Quad Flat Package No Leads (QFN) Package Design Notes

Electrical contact of the part to the Printed Circuit Board (PCB) is made by soldering the leads on the bottom surface of the

Note

3. Source for recommendations: *EZ-USB FX2™ PCB Design Recommendations*, http:///www.cypress.com/cfuploads/support/app_notes/FX2_PCB.pdf *High-Speed USB Platform Design Guidelines*, http://www.usb.org/developers/docs/hs_usb_pdg_r1_0.pdf.

package to the PCB. Hence, special attention is required to the heat transfer area below the package to provide a good thermal bond to the circuit board. A Copper (Cu) fill is to be designed into the PCB as a thermal pad under the package. Heat is transferred from the MoBL-USB TX2 through the device's metal paddle on the bottom side of the package. Heat from here, is conducted to the PCB at the thermal pad. It is then conducted from the thermal pad to the PCB inner ground plane by an array of via. A via is a plated through hole in the PCB with a finished diameter of 13 mil. The QFN's metal die paddle must be soldered to the PCB's thermal pad. Solder mask is placed on the board top side over each via to resist solder flow into the via. The mask on the top side also minimizes outgassing during the solder reflow process.

For further information on this package design, refer to the application note "Surface Mount Assembly of AMKOR's MicroLeadFrame (MLF) Technology." The application note can be downloaded from AMKOR's web site from the following URL http://www.amkor.com/products/notes_papers/MLFApp Note.pdf. The application note provides detailed information on board mounting guidelines, soldering flow, rework process, etc.

Figure 8 displays a cross-sectional area underneath the package. The cross section is of only one via. The solder paste template needs to be designed to allow at least 50% solder coverage. The thickness of the solder paste template should be 5 mil. It is recommended that 'No Clean', type 3 solder paste be used for mounting the part. Nitrogen purge is recommended during reflow.

Figure 9 is a plot of the solder mask pattern image of the assembly (darker areas indicate solder).

Figure 8. Crosssection of the Area Underneath the QFN Package

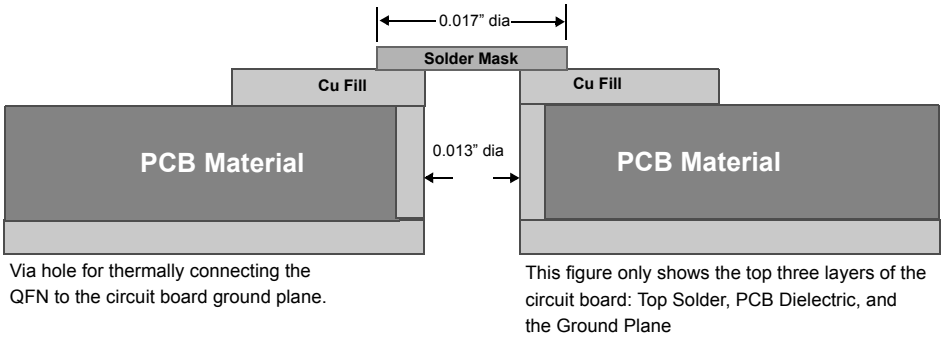
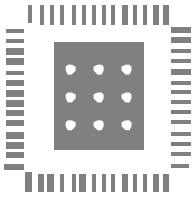


Figure 9. Plot of the Solder Mask (White Area)



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Document History Page

Document Title: CY7C68000A MoBL-USB™ TX2 USB 2.0 UTMI Transceiver Document Number: 38-08052				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	285592	See ECN	KKU	New data sheet
*A	427959	See ECN	TEH	Addition of VFBGA Package information and Pinout, Removal of SSOP Package. Edited text and moved figure titles to the top per new template
*B	470121	See ECN	TEH	Change from preliminary to final data sheet. Grammatical and formatting changes
*C	476107	See ECN	TEH	This data sheet needs to be posted to the web site under NDA
*D	491668	See ECN	TEH	Addition of Tri-state Mode
*E	498415	See ECN	TEH	Update power consumption numbers
*F	567869	See ECN	TEH	Remove NDA requirement