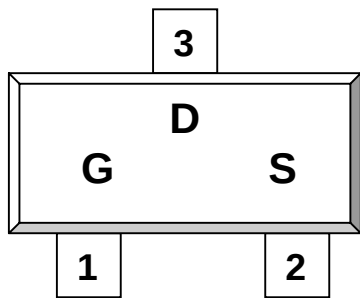


DESCRIPTION

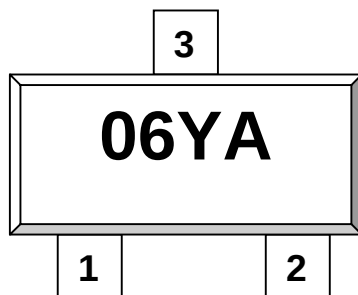
The ST2306 is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density, DMOS trench technology.

This high-density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other batter powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION**SOT-23-3L / SOT-23**

1.Gate 2.Source 3.Drain

**FEATURE**

- 30V/3.5A, $R_{DS(ON)} = 70\text{m-ohm}$ @VGS = 10V
- 30V/2.8A, $R_{DS(ON)} = 95\text{m-ohm}$ @VGS = 5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L /SOT-23 package design

S: Subcontractor Y: Year Code A: Process Code

**STANSON TECHNOLOGY**

120 Bentley Square, Mountain View, Ca 94040 USA

TEL: (650) 9389294 FAX: (650) 9389295

N Channel Enhancement Mode MOSFET ST2306

3.5A

ABSOLUTE MAXIMUM RATINGS (Ta = 25 Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		VDSS	30	V
Gate-Source Voltage		VGSS	±20	V
Continuous Drain Current (TJ=150 °C)	TA=25	ID	3.5	A
	TA=70		2.5	
Pulsed Drain Current		IDM	12	A
Continuous Source Current (Diode Conduction)		IS	1.25	A
Power Dissipation	TA=25	PD	1.25	W
	TA=70		0.8	
Operation Junction Temperature		TJ	150	
Storage Temperature Range		TSTG	-55/150	
Thermal Resistance-Junction to Ambient		R θ JA	100	/W

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3.5A

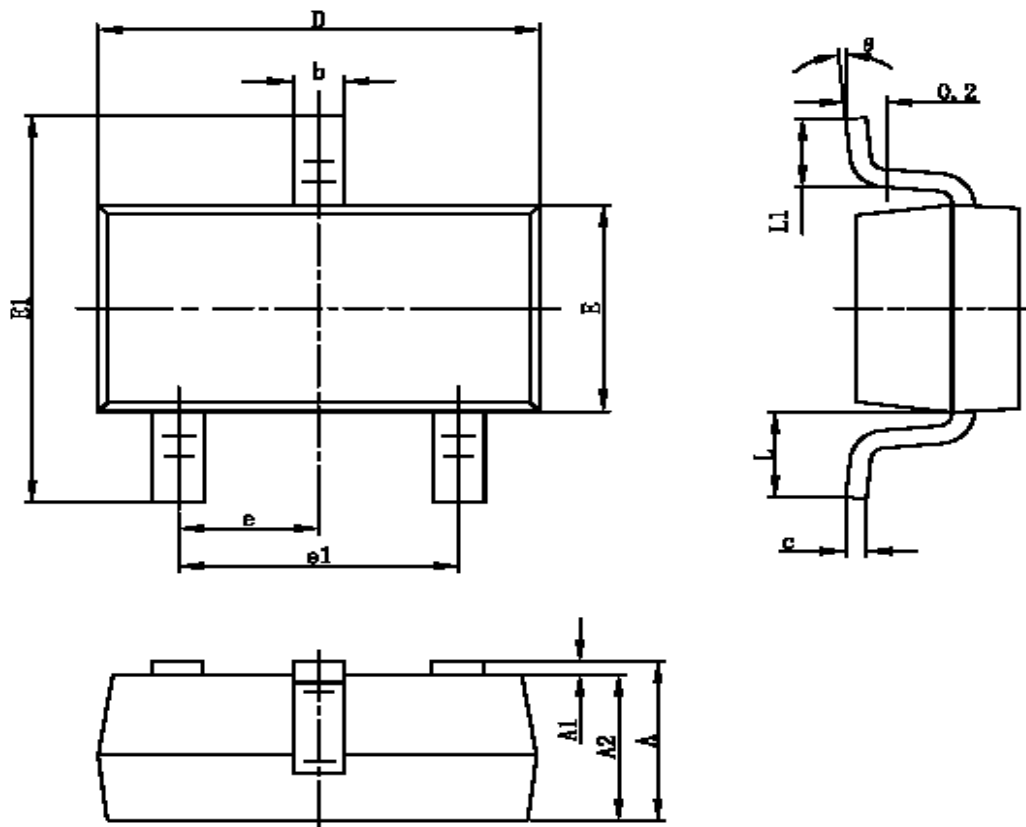
ELECTRICAL CHARACTERISTICS (Ta = 25 Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=20V$			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=1.0V$			1	uA
		$V_{DS}=30V, V_{GS}=0V$ $T_J=55$			10	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=3.5A$ $V_{GS}=5V, I_D=2.8A$		0.055 0.075	0.07 0.95	Ω
Forward Tran conductance	g_{fs}	$V_{DS}=4.5V, I_D=2.5V$		4.6		S
Diode Forward Voltage	V_{SD}	$I_S=-1.25A, V_{GS}=0V$		0.77	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=4.5V$ $I_D \equiv 2.5A$		12.5	16	nC
Gate-Source Charge	Q_{gs}			2.4		
Gate-Drain Charge	Q_{gd}			1.0		
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V$ $F=1MHz$		340		pF
Output Capacitance	C_{oss}			80		
Reverse Transfer Capacitance	C_{rss}			40		
Turn-On Time	$t_{d(on)}$	$V_{DD}=15V, R_L=15\Omega$ $I_D=1.0A, V_{GEN}=10V$ $R_G=6\Omega$		8	20	nS
	t_r			12	30	
Turn-Off Time	$t_{d(off)}$			17	35	
	t_f			8	20	

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3.5A

SOT-23-3L PACKAGE OUTLINE



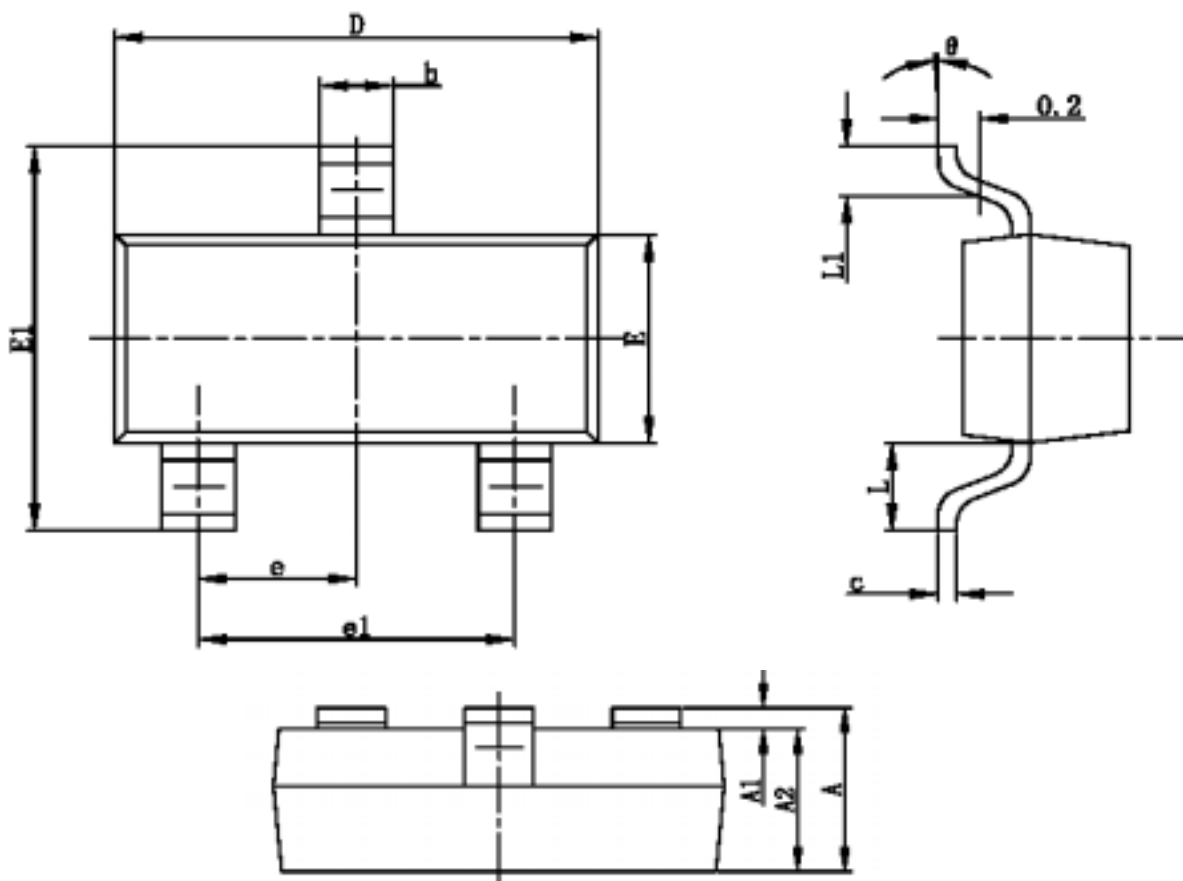
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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3.5A

SOT-23 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

**STANSON TECHNOLOGY**

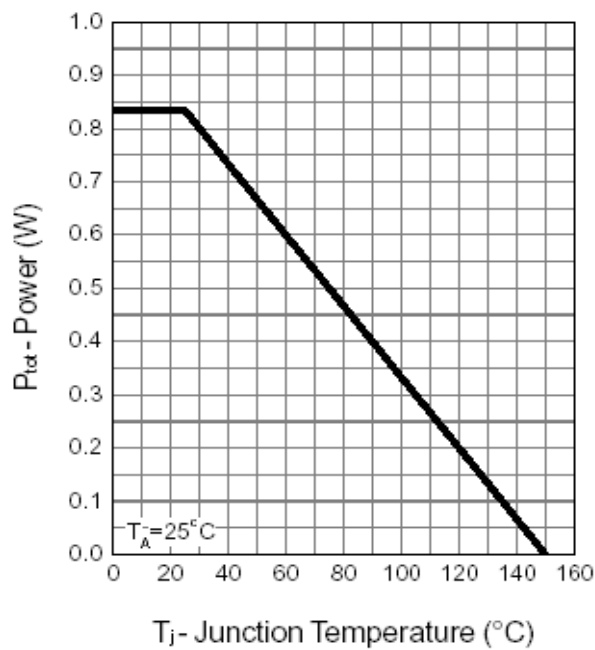
120 Bentley Square, Mountain View, Ca 94040 USA

TEL: (650) 9389294 FAX: (650) 9389295

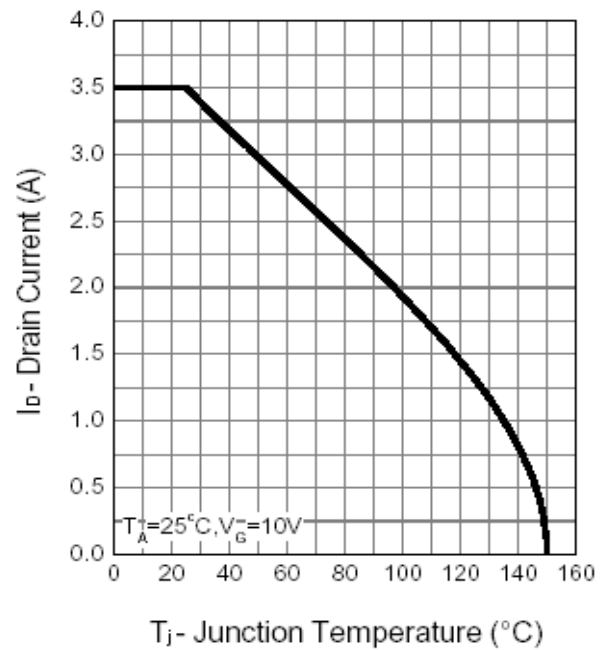
3.5A

TYPICAL CHARACTERISTICS (25 Unless noted)

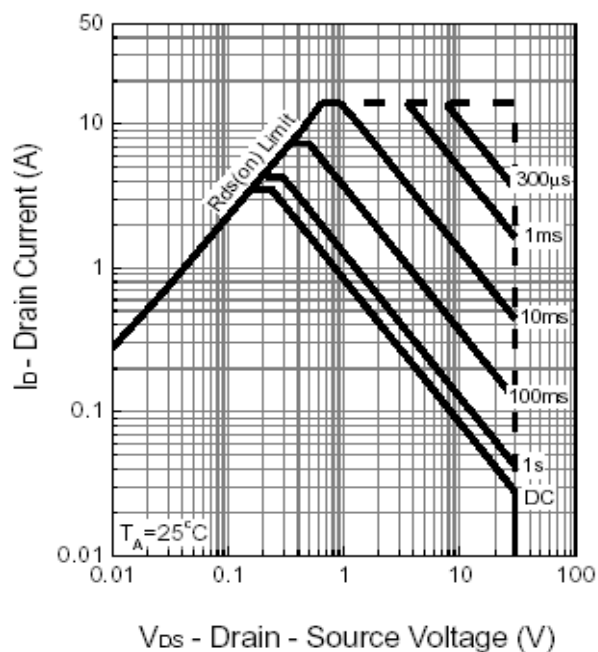
Power Dissipation



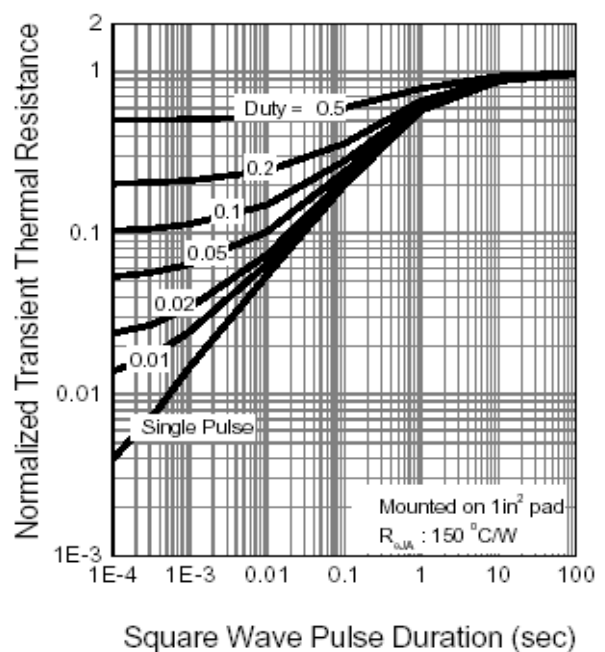
Drain Current



Safe Operation Area

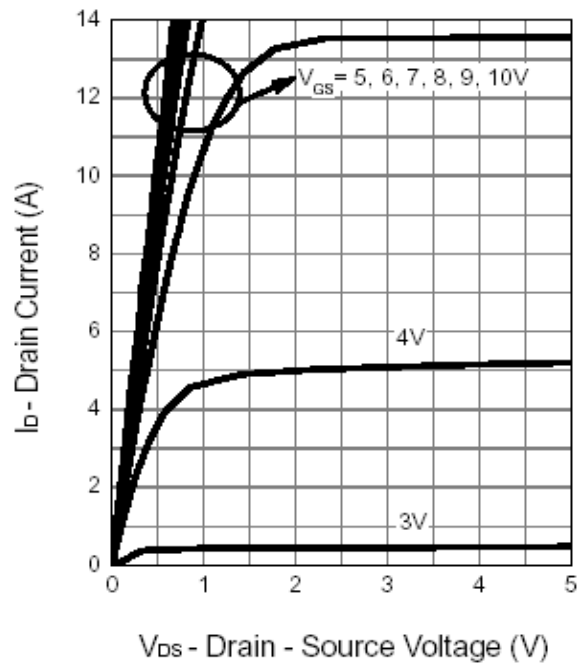


Thermal Transient Impedance

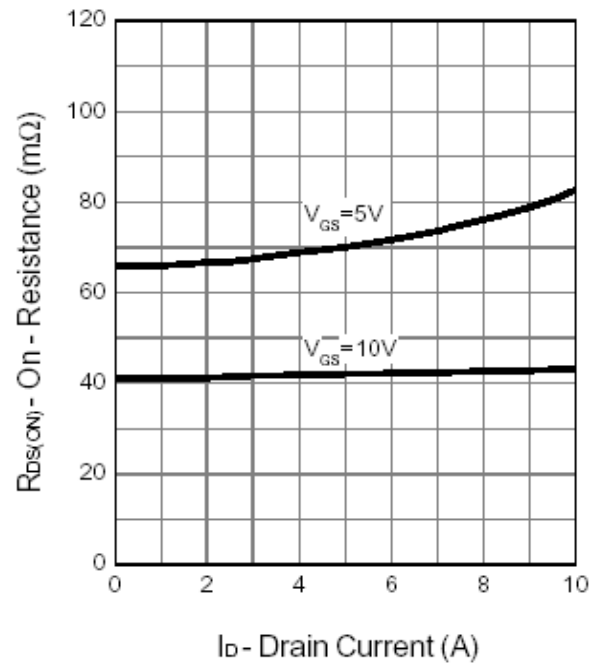


TYPICAL CHARACTERISTICS (25 Unless noted)

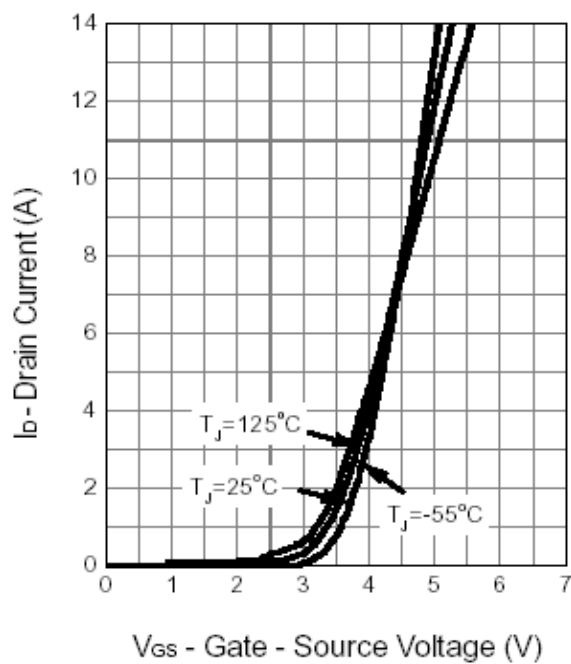
Output Characteristics



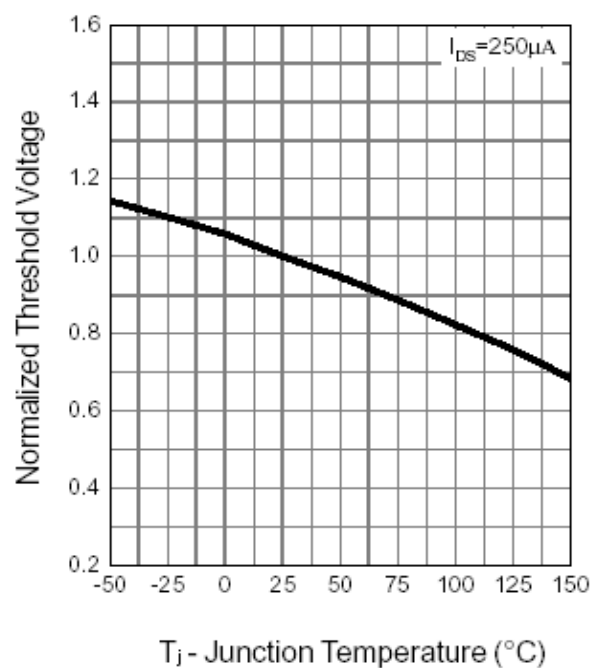
Drain-Source On Resistance



Transfer Characteristics

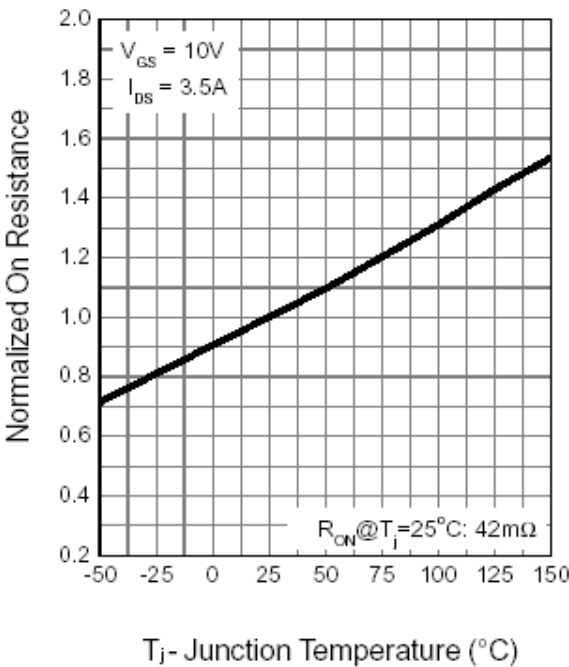


Gate Threshold Voltage

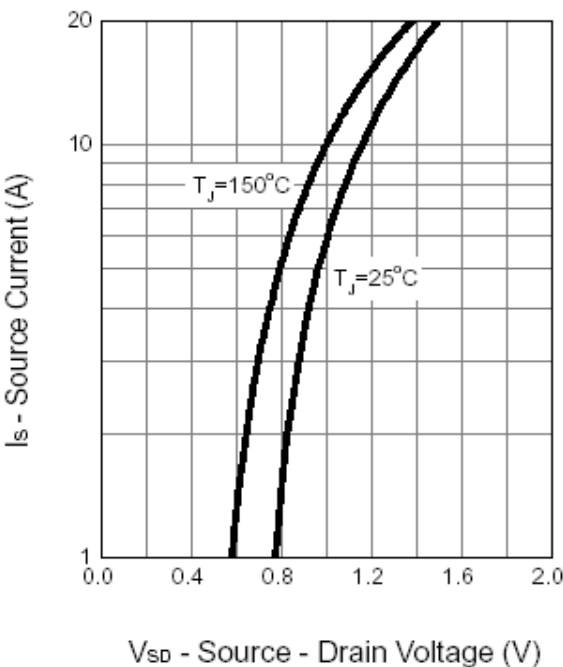


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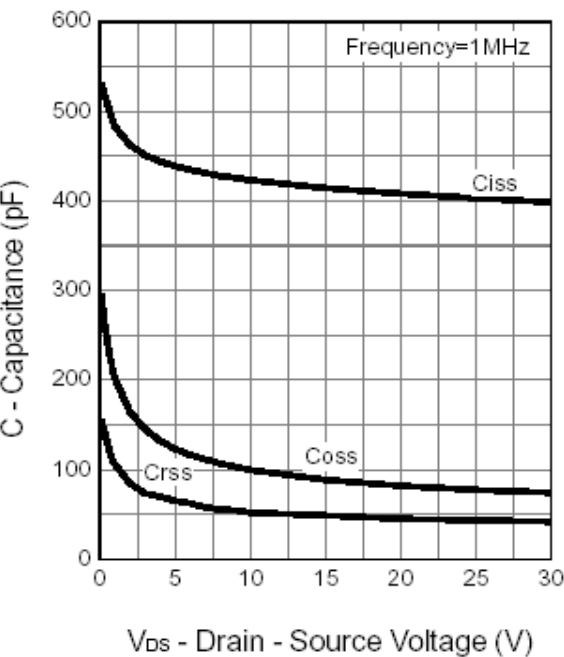
Drain-Source On Resistance



Source-Drain Diode Forward



Capacitance



Gate Charge

