Integrated
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ICS83021I
1-TO-1
2.5V, 3.3V DIFFERENTIAL-TO-LVCMOS/LVTTL TRANSLATOR

## GENERAL DESCRIPTION

ICS
HiPerClockS™

The ICS83021I is a 1-to-1 Differential-to-LVCMOS/LVTTL Translator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The differential input is highly flexible and can accept the following input types: LVPECL, LVDS, LVHSTL, SSTL, and HCSL. The small 8-lead SOIC footprint makes this device ideal for use in applications with limited board space.

FEATURES

- One LVCMOS / LVTTL output

- Differential CLK, nCLK input pair

- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL

- Maximum output frequency: 350MHz (typical)

- Part-to-part skew: 500ps (maximum)

- Additive phase jitter, RMS: 0.21ps (typical), 3.3V output

- Small 8 lead SOIC package saves board space

- Full 3.3V, 2.5V operating supply

- -40°C to 85°C ambient operating temperature

- Available in both standard and lead-free RoHS-compliant packages

BLOCK DIAGRAM
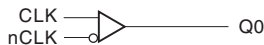
PIN ASSIGNMENT
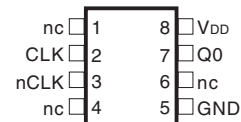
ICS83021I

8-Lead SOIC
3.8mm x 4.8mm, x 1.47mm package body
M Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 4, 6	nc	Unused		No connect.
2	CLK	Input	Pulldown	Non-inverting differential clock input.
3	nCLK	Input	Pullup	Inverting differential clock input.
5	GND	Power		Power supply ground.
7	Q0	Output		Single clock output. LVCMOS / LVTTL interface levels.
8	V_{DD}	Power		Positive supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	$V_{DD} = 3.6V$		23		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance		5	7	12	Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} — 4.6V

Inputs, V_I — -0.5V to V_{DD} + 0.5 V

Outputs, V_O — -0.5V to V_{DD} + 0.5 V

Package Thermal Impedance, θ_{JA} — 112.7°C/W (0 lfpm)

Storage Temperature, T_{STG} — -65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±0.3V or 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				20	mA

TABLE 3BC. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±0.3V or 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1	V_{DD} = 3.6V	2.6			V
		V_{DD} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information, Output Load Test Circuit Diagrams.

TABLE 3C. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±0.3V or 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	V_{IN} = V_{DD} = 3.6V or 2.625V			5	µA
		CLK	V_{IN} = V_{DD} = 3.6V or 2.625V			150	µA
I_{IL}	Input Low Current	nCLK	V_{IN} = 0V, V_{DD} = 3.6V or 2.625V	-150			µA
		CLK	V_{IN} = 0V, V_{DD} = 3.6V or 2.625V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4A. AC CHARACTERISTICS, V_{DD} = 3.3V±0.3V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			350		MHz
t_{PD}	Propagation Delay, NOTE 1	$f \leq 350\text{MHz}$	1.7	2.0	2.3	ns
$t$sk(pp)	Part-to-Part Skew; NOTE 2, 3				500	ps
$t$jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range (637kHz-10MHz)		0.21		ps
t_R / t_F	Output Rise/Fall Time	0.8V to 2V	100	250	400	ps
odc	Output Duty Cycle	$f \leq 166\text{MHz}$	45	50	55	%
		$166\text{MHz} < f \leq 350\text{MHz}$	40	50	60	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at V_{DD}/2.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages
and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DD}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4B. AC CHARACTERISTICS, V_{DD} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			350		MHz
t_{PD}	Propagation Delay, NOTE 1	$f \leq 350\text{MHz}$	1.9	2.2	2.5	ns
$t$sk(pp)	Part-to-Part Skew; NOTE 2, 3				500	ps
$t$jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range (637kHz-10MHz)		0.21		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		550	ps
odc	Output Duty Cycle	$f \leq 250\text{MHz}$	45	50	55	%
		$250\text{MHz} < f \leq 350\text{MHz}$	40	50	60	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at V_{DD}/2.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages
and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DD}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise.** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

Additive Phase Jitter @ 100MHz (12kHz to 20MHz) = 0.21ps typical
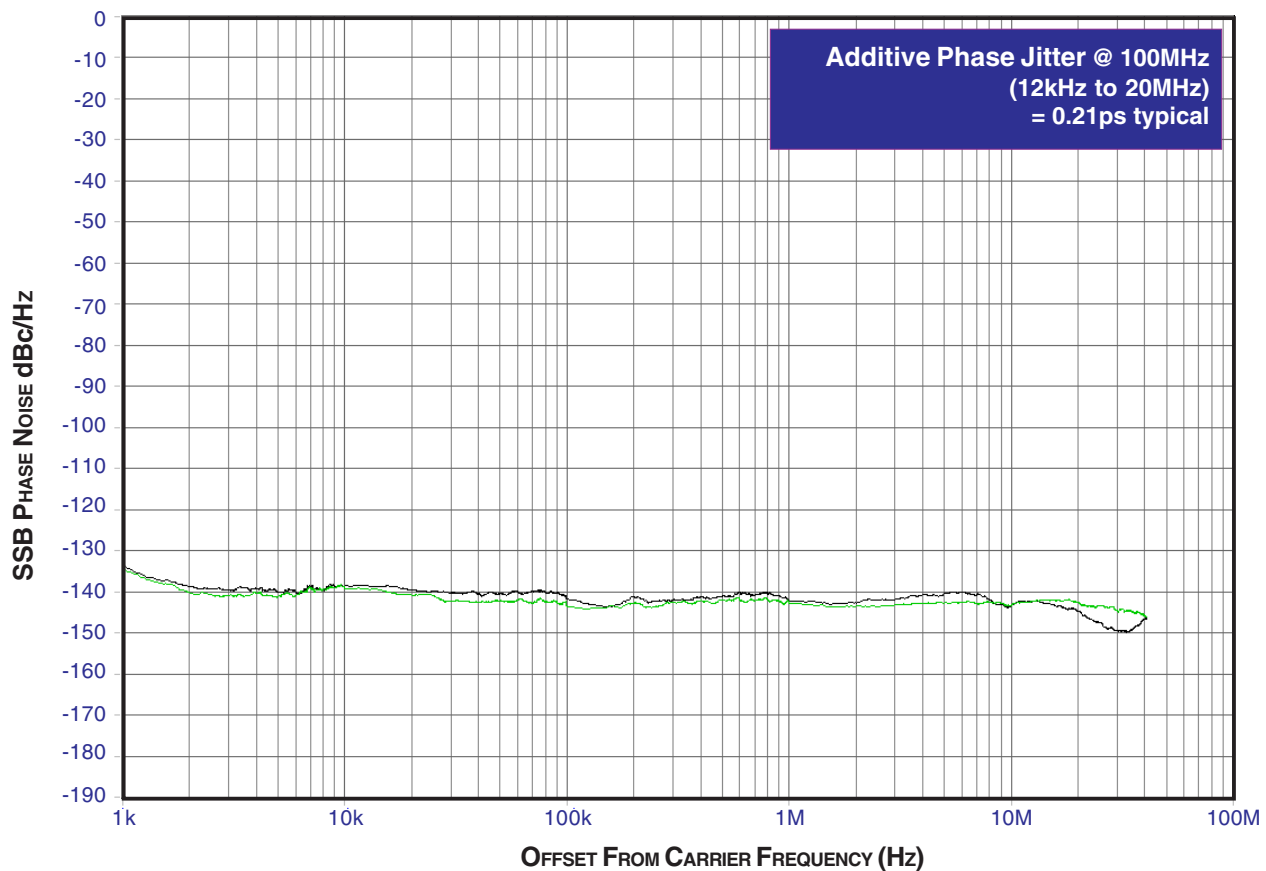
As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.
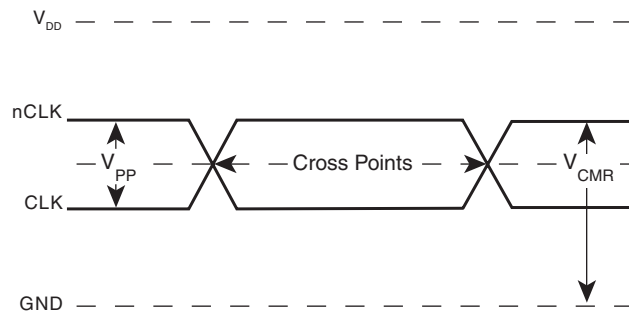
Integrated Circuit Systems, Inc.
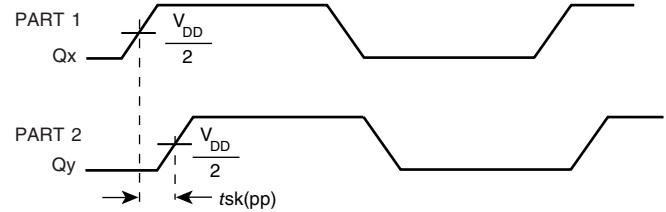
PARAMETER MEASUREMENT INFORMATION
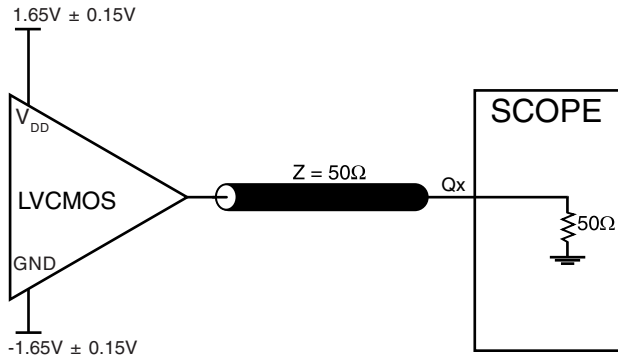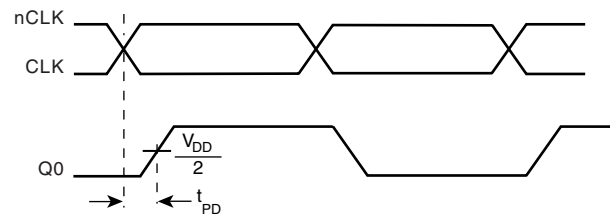
3.3V OUTPUT LOAD AC TEST CIRCUIT
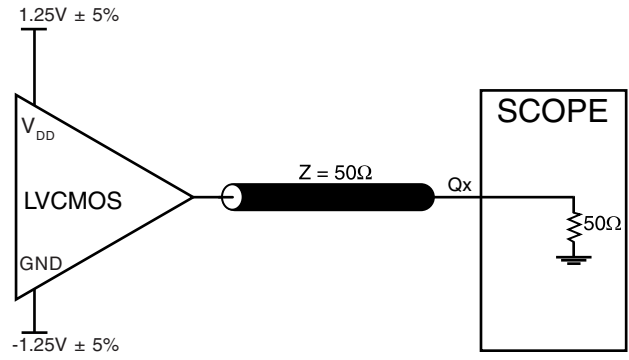
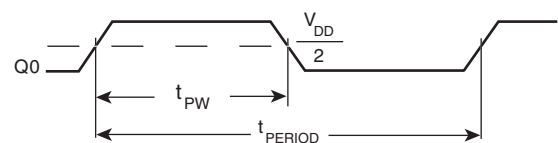**2.5V OUTPUT LOAD AC TEST CIRCUIT**

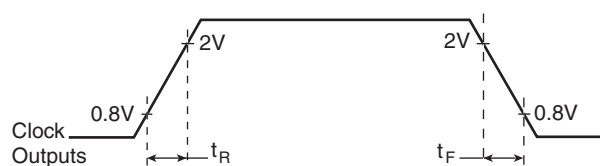**DIFFERENTIAL INPUT LEVEL**
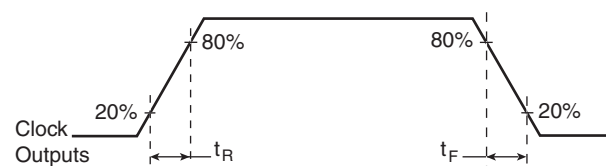
PART-TO-PART SKEW

PROPAGATION DELAY

$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

3.3V OUTPUT RISE/FALL TIME

2.5V OUTPUT RISE/FALL TIME

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APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.
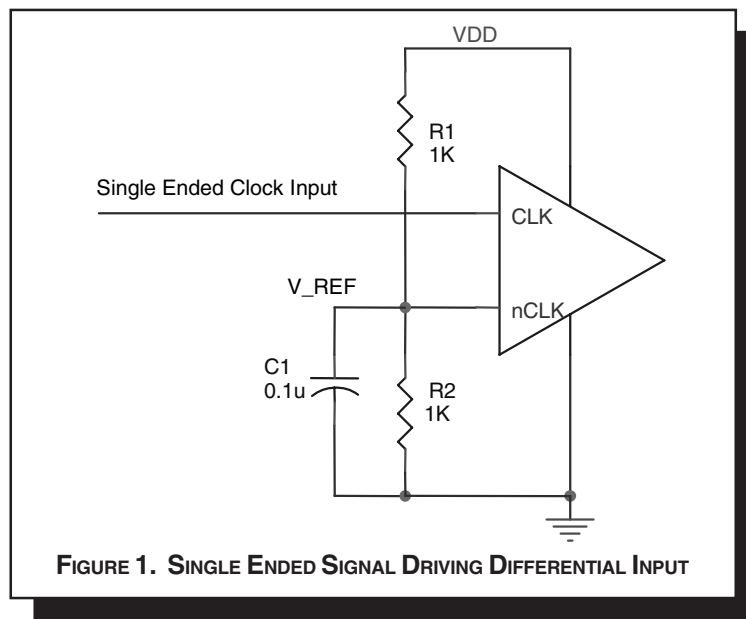

FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

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Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A*, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.
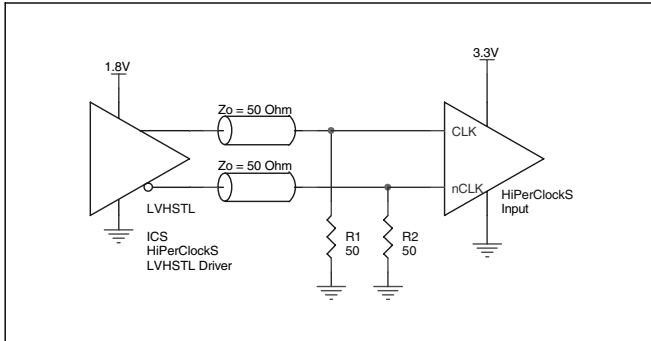

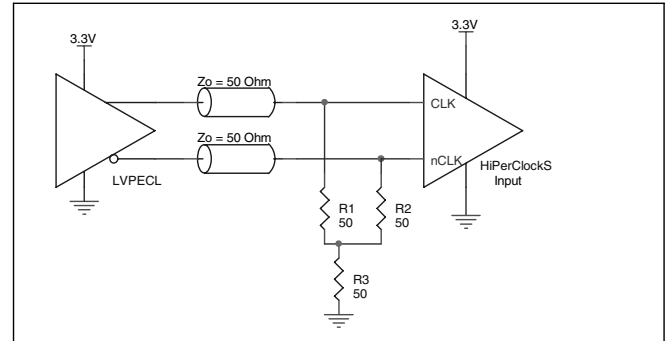**Figure 2A.** Hi**P**er**C**lock**S** CLK/nCLK Input Driven by ICS Hi**P**er**C**lock**S** LVHSTL Driver

Figure 2B. Hi**P**er**C**lock**S** CLK/nCLK Input Driven by 3.3V LVPECL Driver
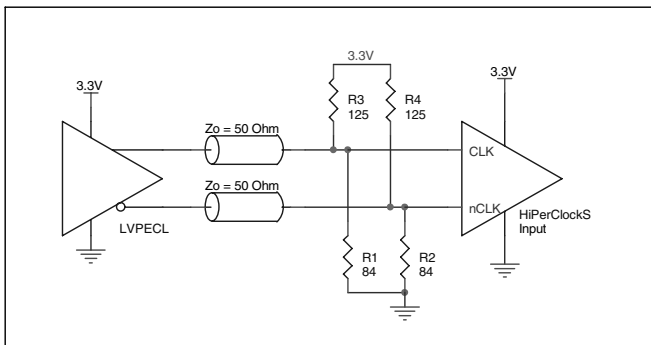
Figure 2C. Hi**P**er**C**lock**S** CLK/nCLK Input Driven by 3.3V LVPECL Driver
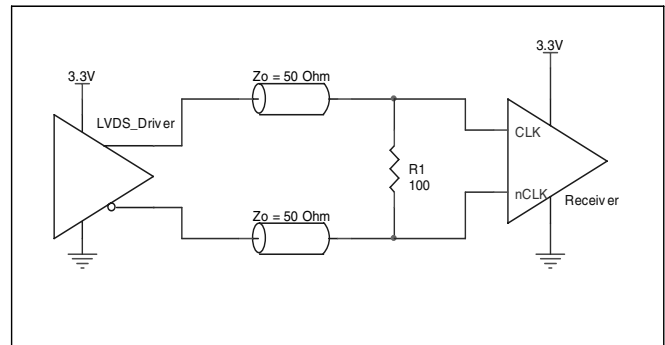
Figure 2D. Hi**P**er**C**lock**S** CLK/nCLK Input Driven by 3.3V LVDS Driver
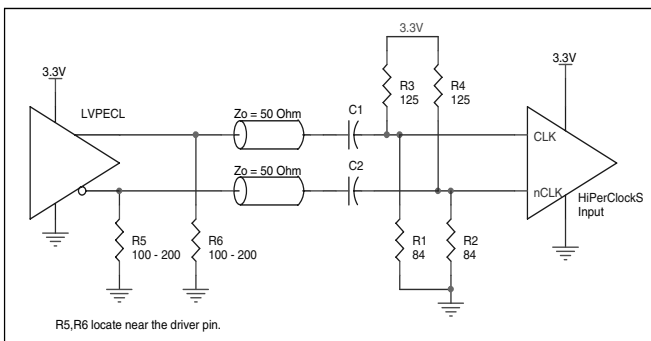
Figure 2E. Hi**P**er**C**lock**S** CLK/n**CLK** Input Driven by 3.3V LVPECL Driver with AC Couple

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RELIABILITY INFORMATION

TABLE 5. θ_{JA} **VS. AIR FLOW TABLE FOR 8 LEAD SOIC**

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT
The transistor count for ICS83021I is: 416

Pin-to-pin compatible with MC100EPT21

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PACKAGE OUTLINE - SUFFIX M FOR 8 LEAD SOIC
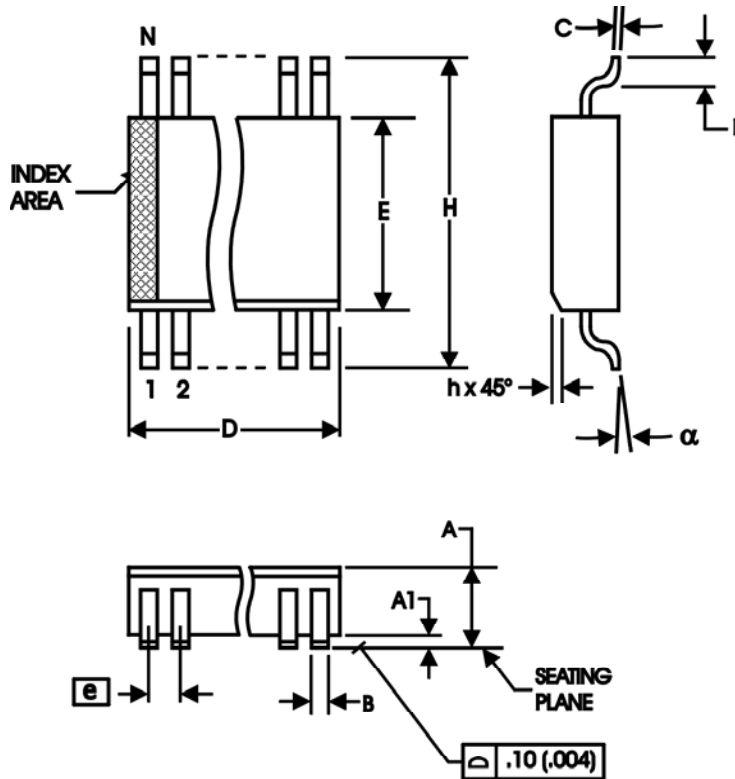
TABLE 6. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

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TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS83021AMI	83021AMI	8 lead SOIC	tube	-40°C to 85°C
ICS83021AMIT	83021AMI	8 lead SOIC	2500 tape & reel	-40°C to 85°C
ICS83021AMILF	83021AIL	8 lead "Lead-Free" SOIC	tube	-40°C to 85°C
ICS83021AMILFT	83021AIL	8 lead "Lead-Free" SOIC	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

			REVISION HISTORY SHEET	
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T2	2	Pin Characteristics table - added 2.5V C_{PD}.	6/3/04
	T3B	3	Added 2.5V Power Supply table.	
	T3C	3	LVCMOS table - added 2.5V V_{OH}.	
	T3D	3	Differential table - added 2.5V.	
	T4B	4	Added 2.5V AC Characteristics table.	
		5	Added 2.5V Output Load AC Test Circuit Diagram and 2.5V Output Rise/Fall Time Diagrams.	
		6	Updated Figure 1.	
		7	Added Differential Clock Input Interface section.	
B		2	Pin Characteristics Table - changed C_{IN} 4pF max. to 4pF typical.	6/30/04
	T4A	4	3.3V AC Characteristics Table - changed odc Test Conditions.	
B		1	Features Section - added Lead-Free bullet.	3/21/05
	T7	10	Ordering Information Table - Added Lead-Free part number.	
C		1	Features Section - added Additive Phase Jitter bullet.	12/12/05
	T4A, T4B	4	AC Characteristics Tables - added Additive Phase Jitter row.	
		5	Added Additive Phase Jitter Plot.	
	T7	11	Added Lead-Free Note.	