FEATURES

- High accuracy. Less than 0.1% error in active energy measurement and reactive measurement over a dynamic range of 3000:1.
- High stability, less than 0.1%error in the output frequency fluctuation.
- Measure the active power in the positive orientation and negative orientation, transform to fast pulse output (CF).
- Measure the reactive power transform to fast pulse output (CF_VAR).
- Measure the reactive power transform to fast pulse output (CF_VA).
- Measure instantaneous IRMS and VRMS over a dynamic range of 1500:1.
- On-chip SAG and zero-crossing detector.
- On-chip power supply detector.
- On-chip anti-creep protection with the programmable threshold set.
- Provide the pulse output with programmable frequency adjustment.
- Provide the programmable gain adjustment and phase compensation
- Measure the power factor (PF).
- Provide a programmable interrupt request signal (/IRQ).
- Provide a SPI/UART communication interface.
- On-chip voltage reference of 2.5V.
- With 3.58MHz external crystal oscillator.
- Single 5V supply, 30mW(typical)

Interrelated patents are pending

DESCRIPTION

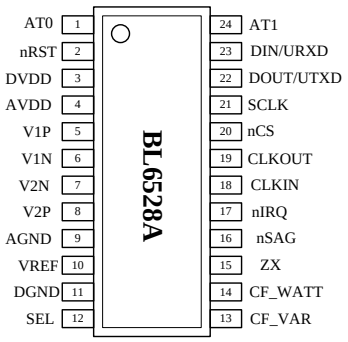
The BL6528 is a low cost, high accuracy, high stability, electrical energy measurement IC intended to single phase, multifunction applications.

The BL6528 incorporates two high accuracy Sigma-Delta ADC, voltage reference, power management and digital signal processing circuit using to calculates active energy , reactive energy ,apparent energy ,IRMS ,VRMS etc.

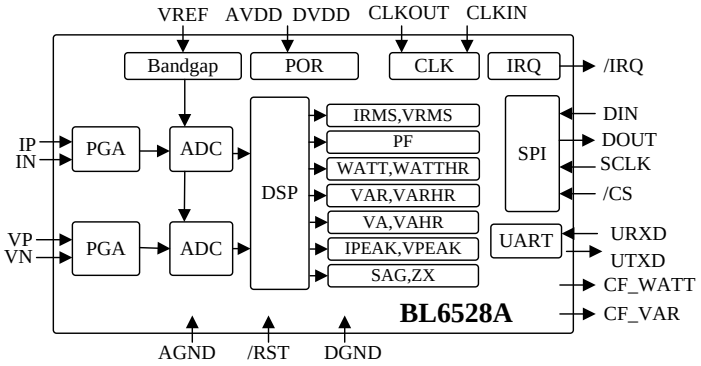
The BL6528 measures line voltage, current and calculates active ,reactive ,apparent energy, power factor, line frequency, detect SAG, overvoltage, overcurrent, PEAK, zero-crossing voltage.

The BL6528 provide access to on-chip meter registers via SPI communication interface.

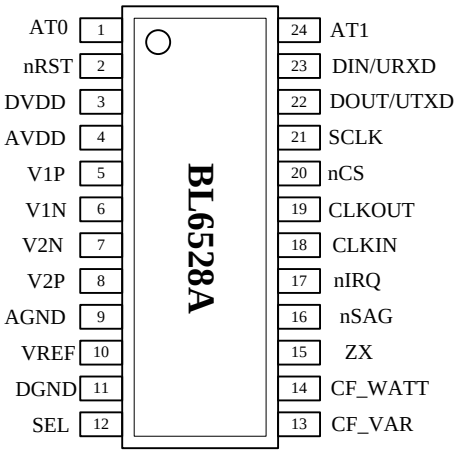
The BL6528 provide all-digital domain offset compensation, gain adjustment, phase compensation (maximum ±2.54 °adjustable).



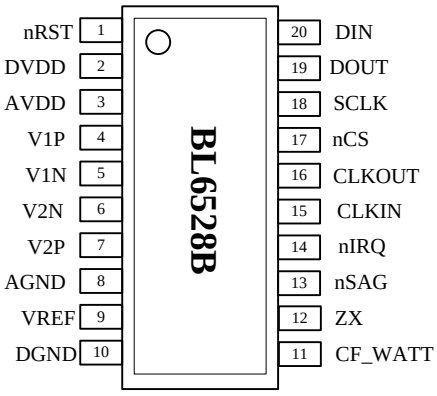
SSOP24



PIN CONFIGURATION



SSOP24



SSOP20

PIN DESCRIPTIONS (SSOP24)

Pin	Symbol	DESCRIPTIONS
1,24	AT0,AT1	Programmable digital output. See AT_SEL register section.
2	nRST	Reset Pin. Logic low on this pin will hold the ADCS and digital circuitry in a reset condition and clear internal registers.
3	DVDD	Digital Power Supply（+5V）,provides the supply voltage for the digital circuitry. It should be maintained at 5 V±5% for specified operation
4	AVDD	Power Supply (+5V). Provides the supply voltage for the circuitry. It should be maintained at 5 V±5% for specified operation.
5,6	V1P,V1N	Analog input for current channel, These inputs are fully differential voltage inputs with a maximum signal level of ±660 mV, Adjustable Gain.
7,8	V2N,V2P	Negative and Positive Inputs for Voltage Channel. These inputs provide a fully differential input pair. The maximum differential input voltage is ± 660 mV for specified operation. Adjustable Gain.

9	AGND	Ground Reference. Provides the ground reference for the circuitry.
10	VREF	On-Chip Voltage Reference. The on-chip reference has a nominal value of 2.5V ± 8% and a typical temperature coefficient of 30ppm/℃. An external reference source may also be connected at this pin. This pin should be decoupled to AGND with a 1uF ceramic capacitor.
11	DGND	Digital Ground.
12	SEL	Logic input to select SPI or UART. The default is 0, SPI mode; SEL=1,UART mode.
13	CF_VAR	Calibration frequency. The CF_VAR logic output gives instantaneous reactive power information. This output is intended to use for calibration purposes. The full-scale output frequency can be scaled by the value of CFDIV register. When the power is low, the pulse width is equal to 90ms. When the power is high and the output period less than 180ms, the pulse width equals to half of the output period.
14	CF_WATT	Calibration Frequency. The CF logic output gives instantaneous active power information. This output is intended to use for calibration purposes. The full-scale output frequency can be scaled by the value of CFDIV register. When the power is low, the pulse width is equal to 90ms. When the power is high and the output period less than 180ms, the pulse width equals to half of the output period
15	ZX	Voltage waveform Zero –cross output
16	nSAG	This logic output goes active low when either no zero- cross are detected or a low voltage threshold is crossed for a specified duration
17	nIRQ	Interrupt request output.
18	CLKIN	Clock In. An external clock can be provided at this logic input, Alternatively, a crystal (3.58MHz) can be connected across this pin and pin17 to provide a clock source. Ceramic load capacitors of between 22pF and 33pF should be used with the gate oscillator circuit.
19	CLKOUT	A crystal can be connected access this pin and PIN16 to provide a clock source for BL6528.
20	nCS	Chip select for SPI interface. This pin must be pulled low if using the SPI interface.
21	SCLK	Serial clock input for the synchronous serial interface. All serial communication data are synchronized to the clock.
22	DOUT/UTXD	When SEL=0, Data output for SPI interface. Data is shifted out at this pin on the rising edge of SCLK. This output is normally in a high impedance state, unless it is driving data out to the serial data bus. When SEL=1, Transmit Line for UART interface
23	DIN/URXD	When SEL=0, Data input for SPI interface. Data is shifted in at this pin on the rising edge of SCLK。When SEL=1, Receive Line for UART interface

PIN DESCRIPTIONS (SSOP20)

Pin	Symbol	DESCRIPTIONS

1	nRST	Reset Pin. Logic low on this pin will hold the ADCS and digital circuitry in a reset condition and clear internal registers.
2	DVDD	Digital Power Supply（+5V）,provides the supply voltage for the digital circuitry. It should be maintained at 5 V±5% for specified operation
3	AVDD	Power Supply (+5V). Provides the supply voltage for the circuitry. It should be maintained at 5 V±5% for specified operation.
4,5	V1P,V1N	Analog input for current channel, These inputs are fully differential voltage inputs with a maximum signal level of ±660 mV, Adjustable Gain.
6,7	V2N,V2P	Negative and Positive Inputs for Voltage Channel. These inputs provide a fully differential input pair. The maximum differential input voltage is ± 660 mV for specified operation. Adjustable Gain.
8	AGND	Ground Reference. Provides the ground reference for the circuitry.
9	VREF	On-Chip Voltage Reference. The on-chip reference has a nominal value of 2.5V ± 8% and a typical temperature coefficient of 30ppm/℃. An external reference source may also be connected at this pin. This pin should be decoupled to AGND with a 1uF ceramic capacitor.
10	DGND	Digital Ground.
11	CF_WATT	Calibration Frequency. The CF logic output gives instantaneous active power information. This output is intended to use for calibration purposes. The full-scale output frequency can be scaled by the value of CFDIV register. When the power is low, the pulse width is equal to 90ms. When the power is high and the output period less than 180ms, the pulse width equals to half of the output period
12	ZX	Voltage waveform Zero –cross output
13	nSAG	This logic output goes active low when either no zero- cross are detected or a low voltage threshold is crossed for a specified duration
14	nIRQ	Interrupt request output.
15	CLKIN	Clock In. An external clock can be provided at this logic input, Alternatively, a crystal (3.58MHz) can be connected across this pin and pin17 to provide a clock source. Ceramic load capacitors of between 22pF and 33pF should be used with the gate oscillator circuit.
16	CLKOUT	A crystal can be connected access this pin and PIN16 to provide a clock source for BL6528.
17	nCS	Chip select for SPI interface. This pin must be pulled low if using the SPI interface.
18	SCLK	Serial clock input for the synchronous serial interface. All serial communication data are synchronized to the clock.
19	DOUT	Data output for SPI interface. Data is shifted out at this pin on the rising edge of SCLK. This output is normally in a high impedance state, unless it is driving data out to the serial data bus.
20	DIN/URXD	Data input for SPI interface. Data is shifted in at this pin on the rising edge of SCLK.

ABSOLUTE MAXIMUM RATIONS

（T = 25 ℃）

Parameter	Symbol	Value	单位
Power Voltage AVDD、DVDD	AVDD、DVDD	-0.3 ~ +7	V
Analog Input Voltage to AGND	V1P、V2P	-6 ~ +6	V
Digital Input Voltage to DGND	DIN、SCLK、/CS	-0.3 ~ VDD+0.3	V
Digital Output Voltage to DGND	CF_WATT、CF_VAR、AT0、AT1、/IRQ、DOUT	-0.3 ~ VDD+0.3	V
Operating Temperature Range	Topr	-40 ~ +85	℃
Storage Temperature Range	Tstr	-55 ~ +150	℃
Power Dissipation（SSOP24）	P	80	mW

Electronic Characteristic Patameter

（AVDD = DVDD = 5V, AGND = DGND = 0V, CLKIN=3.58MHz, T=25℃）

Parameter	Symbol	Test Condition	Measure Pin	Min Value	Typical Value	Max Value	Unit
Measure Error on Active Power	$WATT_{err}$	Over a dynamic range 3000:1	CF		0.1	0.3	%
Phase error when PF=0.8 Capacitive	PF08err	Current lead 37°（PF=0.8）				0.5	%
Phase error when PF=0.5Inductive	PF05err	Current lags 60°（PF=0.5）				0.5	%
AC PSRR	ACPSRR	IP/N=100mV			0.01		%
DC PSRR	DCPSRR	VP/N=100mV			0.1		%
Vrms measurement Error	VRMSerr	1500:1 input DR			0.3		%
Irms measurement Error	IRMSerr	1500:1 input DR			0.3		%

Maximum Input voltage						± 1200	mV
DC Input Voltage				370			kΩ
Input Signal Bandwidth		(-3dB)			14		kHz
Gain Error		External 2.5V reference		-4		+4	%
Gain Error match		External 2.5V reference		-1.5		+1.5	%
On-chip reference	Vref		VREF		2.5		V
Reference Error	Vreferr					±200	mV
Temperature Coefficient	TempCoef				30		ppm/℃
Input High Voltage		DVDD=5V±5%		2.6			V
Input Low Voltage		DVDD=5V±5%				0.8	V
Output High Voltage		DVDD=5V±5%		4			V
Output Low Voltage		DVDD=5V±5%				1	V
Analog Power AVDD	VAVDD			4.75		5.25	V
Digital Power DVDD	VDVDD			4.75		5.25	V
AIDD	IAVDD	AVDD=5.25V			3		mA
DIDD	IDVDD	DVDD=5.25			2		mA

Theory of Operation

Principle of Energy Measure

In energy measure, the power information varying with time is calculated by a direct multiplication of the voltage signal and the current signal. Assume that the current signal and the voltage signal are cosine functions, V,I are the peak values of the voltage signal and the current signal; the phase difference between the current signal and the voltage signal is expressed as Φ,Then the power is given as follows:

$$p(t) = V\cos(wt) \times I\cos(wt + \Phi)$$

If Φ=0 时：

$$p(t) = \frac{VI}{2}(1 + \cos(2wt))$$

If $\Phi \neq 0$ 时：

$$p(t) = V\cos(wt) \times I\cos(wt + \Phi)$$
$$= V\cos(wt) \times [I\cos(wt)\cos(\Phi) + \sin(wt)\sin(\Phi)]$$
$$= \frac{VI}{2}(1 + \cos(2wt))\cos(\Phi) + VI\cos(wt)\sin(wt)\sin(\Phi)$$
$$= \frac{VI}{2}(1 + \cos(2wt))\cos(\Phi) + \frac{VI}{2}\sin(2wt)\sin(\Phi)$$

p(t) is called as the instantaneous power signal. The ideal p(t) consists of the DC component and AC component whose frequency is 2ω. The DC component is called as the average active power.

The current signal and voltage signal is converted to digital signals by high-precision ADCS, then through the drop sampling filter (SINC4), high-pass filter (HPF) filter out the high frequency noise and DC gain, get the required current and voltage sampling data.

Current sampling data multiplied by voltage sampling data gets instantaneous active power, then through the low pass filter (LPF), output average active power.

Current sampling data and voltage sampling data processed by Hilbert circuit, gets instantaneous reactive power, then through low-pass filter(LPF), output average reactive power.

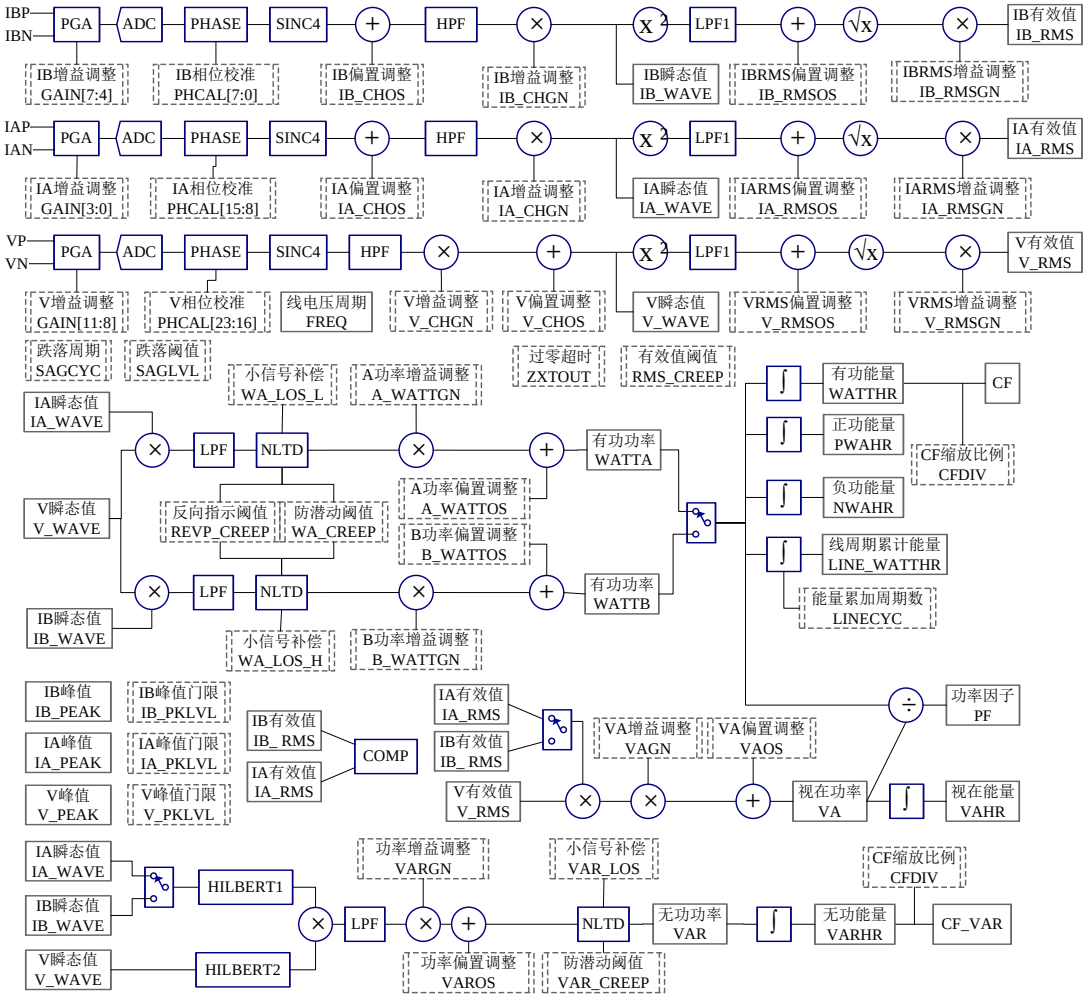
Current sampling data and voltage sampling data processed by square circuit, low-pass filter(LPF1), square root circuit, get the current RMS and voltage RMS.

Active power through a certain time integral, get active energy.

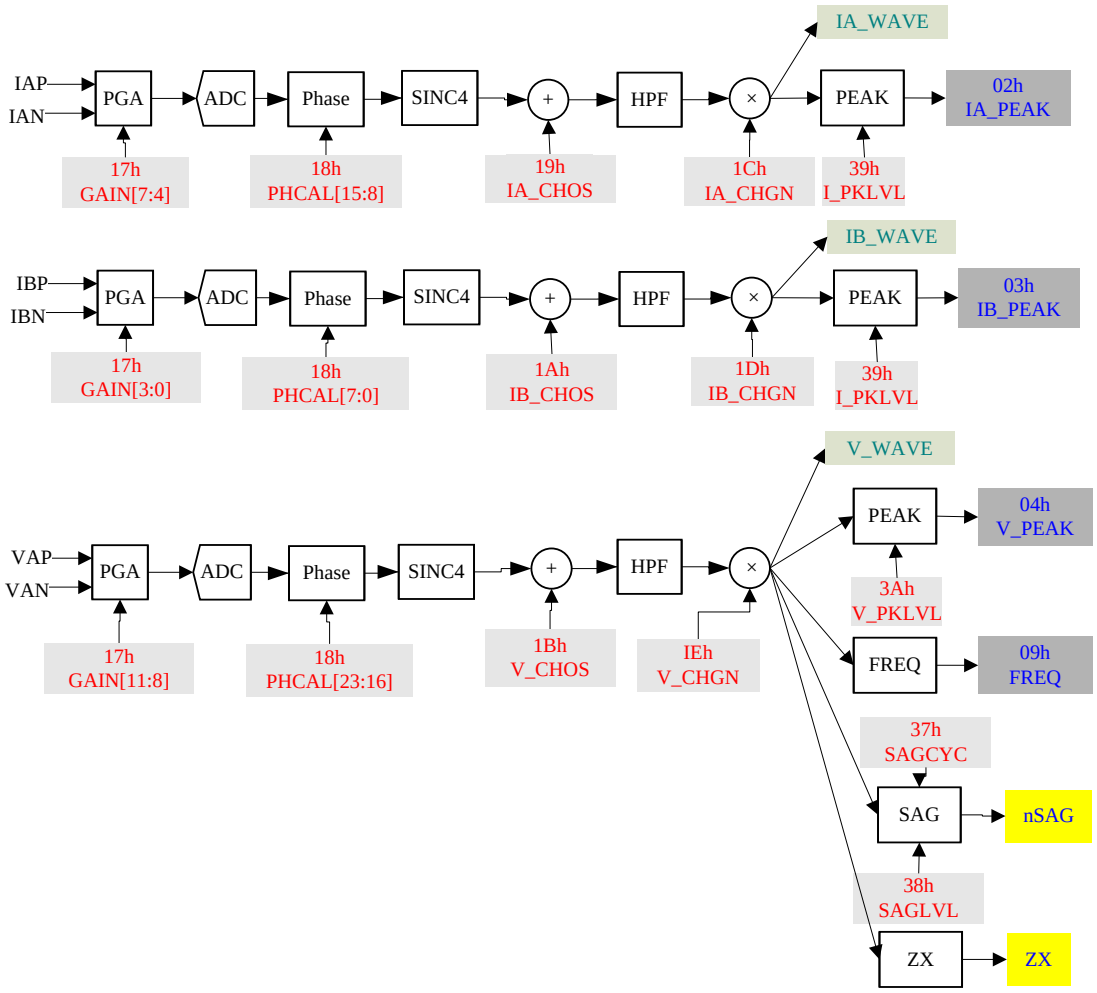
Reactive power through a certain time integral, get reactive energy.

System Block

BL6528 V10系统算法框图



Front-end wave process



Front-end gain adjustment

Every analog channel has a programmable gain amplifier (PGA), gain selection is achieved by the gain register (GAIN), the default value of the gain register (GAIN) is 00H.

Every 4-bit of the gain register used to select the current channel or voltage channel PGA. Gain[3:0] used to select Current A channel PGA,Gain[7:4] used to select Voltage channel PGA.

For example Gain [3:0]:

x000=1x
x001=2x
x010=4x
x011=8x
x100=16x
x101=24x
x110=32x
x111=32x

Phase compensation

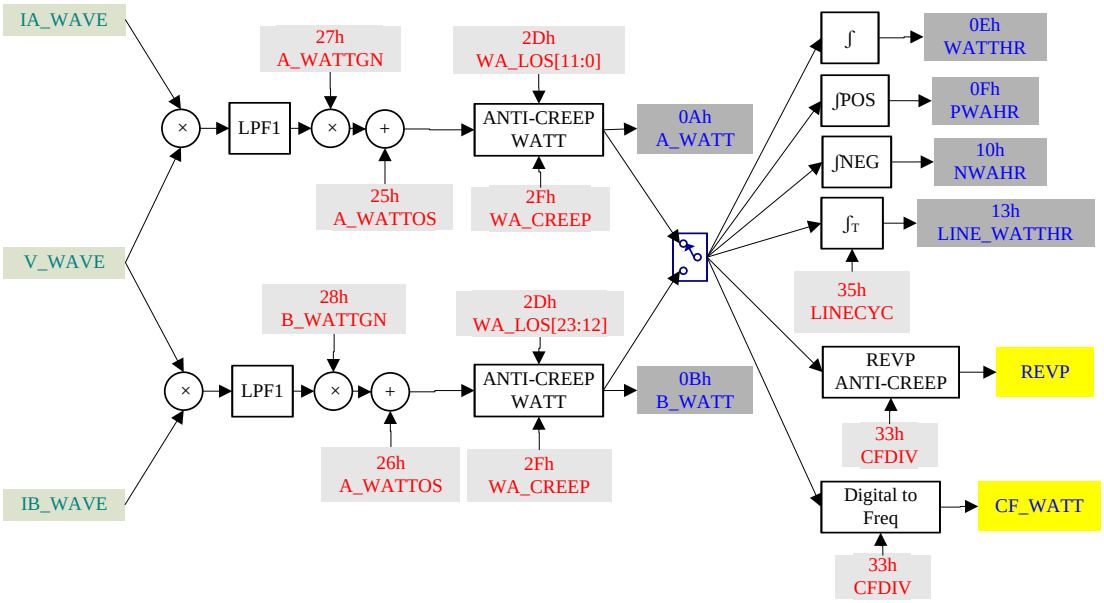
BL6528 provides the method of small phase error digital calibration. It will be a small time delay or advance into signal processing circuit in order to compensate for small phase error. Because this compensation should be promptly, so this method applies only to 0.1°~0.5° range of small phase error.

Phase calibration register(PHCAL_I,PHCAL_V) is a binary 8-bit register, corresponding to the compensation current A channel, current B channel and voltage channel phase. The default value is 00H. Bit[7] is enable bit, when Bit[7]＝0,disable compensation; Bit[7]＝1,enable compensation. Bit[6:0] used to adjust the delay time，1.1us/1LSB. With a line frequency of 50Hz, the resolution is 360°×（1/900KHz）×50Hz=0.02°, The adjustable range is 0°~2.54°.

- **Input channel offset calibration**

BL6528 contains the input channel offset calibration registers (I_CHOS, V_CHOS), these registers are in 12-bit sign magnitude format, the default value is 000H. The offset may result from the analog input and the analog-digital conversion circuit itself.

Active Power Signal Process



Active power offset calibration

BL6528 contains the active power offset calibration (WATTOS). This register is in 12-bit sign magnitude format, the default value is 000H. The offset can exist in the power calculations due to crosstalk between channels on the PCB and in the BL6528. The active power offset calibration allows these offsets to be removed to increase the accuracy of the measurement at low input power levels.

$$ActivePower = ActivePower_0 + \mathrm{WATTOS}$$

Active power gain adjustment

The gain register (WATTGN) is used to adjust the active power measurement range. This register is in 12-bit sign magnitude format, the default value is 000H. The following formula shows how to adjust the output active power:

$$Output \quad ActivePower = Active\ Power \times (1 + \frac{WATTWG}{2^{12}})$$

The minimum value that can be write to the WATTGN register is 801H(HEX), which represents a gain adjustment of -50%. The maximum value that can be write to the WATTGN register is 7FFH (HEX), which represents a gain adjustment of +50%.

Similar gain calibration registers are available for current channel and voltage channel (I_CHGN, V_CHGN).

No-load threshold of active power

BL6528 contains two no-load detection features that eliminate meter creep. BL6528 can set the no-load threshold on the active power (WA_CREEP1), this register is in 12-bit unsigned magnitude format. This register is used to set the active power threshold value, When the absolute value of the input power signal is less than this threshold, the output active power is set to zero. This can make the active power register to 0 in no-load conditions, even a small noise signal input .

$$WATT = \begin{cases} 0 & , \quad |WATT| < WA_CREEP1 \\ WATT, & |WATT| >= WA_CREEP1 \end{cases}$$

The WA_CREEP2 register is used to set the active power timer threshold value. The default value is 0xFFF. There have a internal TIME_CREEP register in BL6523B, when detect the CF pulse output , the TIME_CREEP register is set to the value of WA_CREEP2. If not detected the CF pulse output, the TIME_CREEP register value decrease. If the TIME_CREEP register decrease to 0, there is still no CF signal output, the BL6528 produce a reset signal used to reset the internal energy accumulated register of CF pulse and reload the value of WA_CREEP2 to the TOME_CREEP register. The resolution of the WA_CREEP_H is 4.6s / LSB, so the maxium timing anti-creep time is about 5h13m.

MODE [3]=1 enable timing anti-creep function.

MODE [3]=0 disable timing anti-creep function.

Active power compensation of small signal

BL6528 contains a small active power signal compensation register (WA_LOS), this register is in 12-bit sign magnitude format. The default value is 000H。

Reverse indicator threshold

BL6528 contains a reverse indicator threshold register(WA_REVP), this register is in 12-bit unsigned magnitude format, When the input power signal is negative and the absolute value is greater than the power threshold， the BL6528 output the REVP indicator.

Active energy calculation

The relationship between power and energy can be expressed as：

$$Power = \frac{dEnergy}{dt}$$

Conversely, energy is given as the integral of power.

$$Energy = \int Power\ dt$$

In BL6528, the active power signals are accumulated in a 53 internal registers continuously to get active energy, Active energy register WATTHR [23:0] take out this internal register[52:29] as active energy output. This discrete time accumulation is equivalent to integration in continuous time.

$$E = \int p(t)dt = Lim_{T\to 0}\{\sum_{n=0}^{\infty} P(nT)\times T\}$$

Where:

n is the discrete time-sample number; T is the sampling period; the sampling period of BL6528 is 1.1us.

The BL6528 include a interrupt (PEHF) that is triggered When the active energy register(WATTHR) is half full. If the enable PEHF bit in the interrupt mask register set to logic high, the / IRQ output Pin goes logic low.

The BL6528 include line cycle energy register(LINE_WATTHR). The number of cycles is written to the LINECYC register, the LSB of the LINECYC register is 0.1S. At the end of a line cycle accumulation cycle, the LINE_WATTHR register is updated. The LINE_WATTHR register hold its current value until the end of the next line cycle period, when the content is replaced with the new reading. If a new value is written to the LINECYC register midway through a line cycle accumulation, the new value is not internally loaded until the end of a line cycle period.

Positive active energy calculation

As same as active energy calculation.

Negative active energy calculation

As same as active energy calculation.

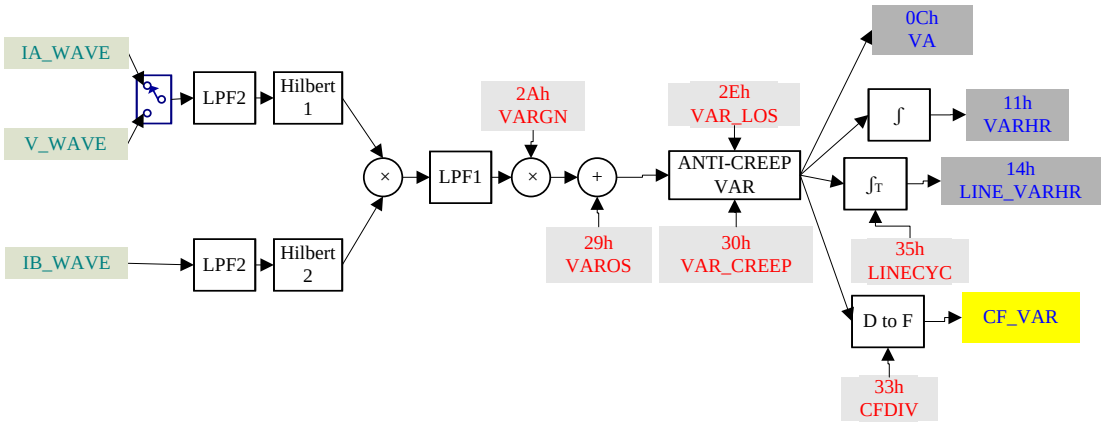
Frequency output

The BL6528 provides two energy-to-frequency conversion for calibration purpose. After initial calibration at manufacturing, the manufacturer or end customer is often required to verify the meter accuracy. One convenient way to do this is to provide an output frequency that is proportional to the reactive power. This output frequency provides a simple single-wire interface that can be optically isolated to interface to external calibration equipment.

BL6528 includes two programmable calibration frequency output PINs (CF_WATT, CF_VAR). The digital-to-frequency converters are used to generate the pulse output. The pulse output stays high for 90ms if the pulse period is longer than 180ms. If the pulse period is shorter than 180ms, the duty cycle of de pulse output is 50%. The maximum output frequency with ac inputs at full scale and with CFDIV=010H is approximately 0.5 kHz.

The BL6528 can set the CF frequency through the CF_DIV register. The default value of the CFDIV register is 001H (HEX). When set CFDIV[x]=1, the CF frequency is $2^{(x-4)}*CF_{CFDIV=010H}$.

Reactive Power Signal Process



Reactive power offset calibration

BL6528 contains the reactive power offset calibration (VAROS). This register is in 12-bit sign magnitude format, the default value is 000H. The offset can exist in the power calculations due to crosstalk between channels on the PCB and in the BL6528. The reactive power offset calibration allows these offsets to be removed to increase the accuracy of the measurement at low input power levels.

$$\mathrm{Re}activePower = \mathrm{Re}activePower_0 + \mathrm{VAROS}$$

Reactive power gain adjustment

The gain register (VARGN) is used to adjust the active power measurement range. This register is in 12-bit sign magnitude format, the default value is 000H. The following formula shows how to adjust the output reactive power:

$$Output\ \ \mathrm{VARGN} = \mathrm{Re}\,Active\ Power \times (1 + \frac{\mathrm{VARGN}}{2^{12}})$$

The minimum value that can be write to the VARGN register is 801H(HEX), which represents a gain adjustmen of -50%. The maximum value that can be write to the VARGN register is 7FFH (HEX), which represents a gain adjustmen of +50%.

No-load Threshold of Reactive Power

BL6528 contains two no-load detection features that eliminate meter creep. BL6528 can set the no-load threshold on the reactive power (VAR_CREEP1), this register is in 12-bit unsigned magnitude format. This register is used to set the reactive power threshold value, when the absolute value of the input power signal is less than this threshold, the output reactive power is set to zero. This can make the reactive power register to 0 in no-load conditions, even a small noise signal input.

$$VAR = \begin{cases} 0 \quad , & |VAR| < VAR_CREEP1 \\ VAR, & |VAR| >= VAR_CREEP1 \end{cases}$$

The VAR_CREEP2 register is used to set the reactive power timer threshold value. The default value is 0xFFF. There have a internal TIME_CREEP register in BL6523B, when detect the CF_VAR pulse output, the TIME_CREEP register is set to the value of VAR_CREEP2. If not detected the CF_VAR pulse output, the TIME_CREEP register value decrease. If the TIME_CREEP register decrease to 0, there is still no CF_VAR signal output, the BL6528 produce a reset signal used to reset the internal energy accumulated register of CF_VAR pulse and reload the value of VAR_CREEP2 to the TOME_CREEP register. The resolution of the VAR_CREEP2 is 4.6s / LSB, so the maximum timing anti-creep time is about 5h13m.

MODE [3] =1 enable timing anti-creep function.

MODE [3] =0 disable timing anti-creep function.

Reactive power compensation of small signal

BL6528 contains a small reactive power signal compensation register (VAR_LOS), this register is in 12-bit sign magnitude format. The default value is 000H。

Reactive energy calculation

The relationship between power and energy can be expressed as：

$$REActive\ \ Energy = \int \mathrm{Re}\,active\ Power(t)\ dt$$

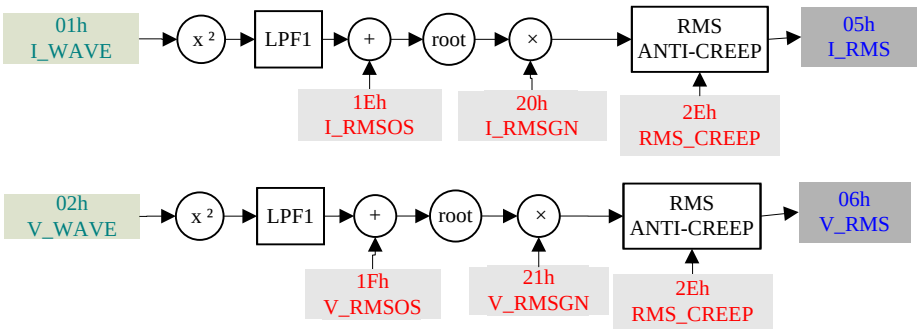
In BL6528, the reactive power signals are accumulated in a 53 internal registers continuously to get reactive energy, Reactive energy register VARHR [23:0] take out this internal register[52:29] as reactive energy output. This discrete time accumulation is equivalent to integration in continuous time.

$$\text{Re } Active\ Energy = Lim_{T\to 0}\{\sum_{n=0}^{\infty} \text{Re } Active\ Power(nT)\times T\}$$

Where:

n is the discrete time-sample number; T is the sampling period; the sampling period of BL6528 is 1.1us.

Root mean square measurement



The rms is expressed mathematically as:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2(t)dt}$$

For time-sampled signals:

$$V_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} V^2(i)}$$

RMS offset calibration

BL6528 contains the rms offset calibration (I_RMSOS, V_RMSOS). These registers are in 12-bit sign magnitude format, the default value is 000H. The offset can exist in the rms calculations due to input noise that is integrated in the dc component of square calculation. The rms offset calibration allows these offsets to be removed to increase the accuracy of the measurement at low input power levels.

$$I_{ARMS} = \sqrt{I_{ARMS0}{}^2 + I_RMSOS \times 2^{17}}$$

RMS gain calibration

The gain registers (I_RMSGN, V_RMSGN) are used to adjust the rms measurement range. Both registers are in 12-bit sign magnitude format, the default value is 000H. The following formula shows how to adjust the rms:

$$Output\ \ rms = rms \times (1 + \frac{X_RMSGN}{2^{12}})$$

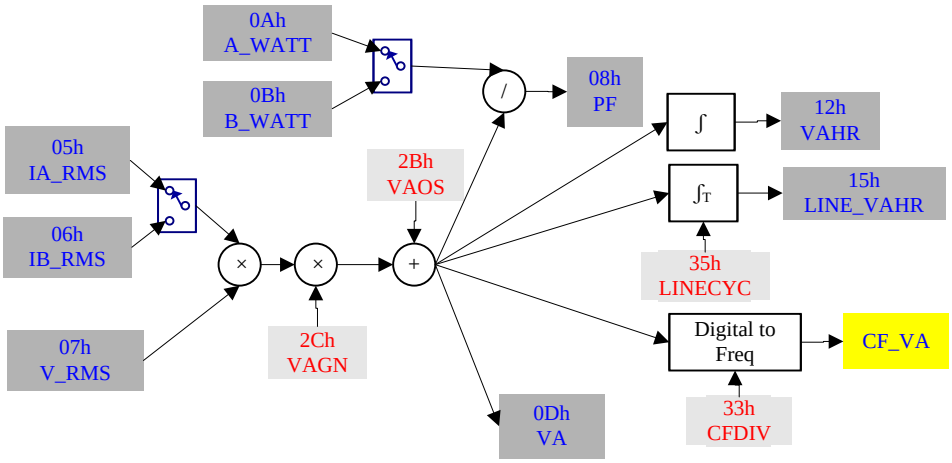
The minimum value that can be write to the X_RMSGN register is 801H(HEX), which represents a gain adjustment of -50%. The maximum value that can be write to the X_RMSGN register is 7FFH (HEX), which represents a gain adjustment of +50%.

No-load threshold of RMS

BL6523B can set the no-load threshold on the RMS_CREEP register, this register is in 12-bit unsigned magnitude format. When the value of the RMS register is less than this threshold, the RMS register is set to zero. This can make the RMS register to 0 in no-load conditions, even a small noise signal input .

$$\mathrm{RMS} = \begin{cases} 0 & |RMS| < RMS_CREEP \times 2 \times 1.3655 \\ \mathrm{RMS}, & |RMS| >= RMS_CREEP \times 2 \times 1.3655 \end{cases}$$

Apparent Power and Apparent Energy Calculation



In BL6528, the apparent power is defined as the product of V_RMS and I_RMS.

VA＝I_RMS×V_RMS

The apparent energy is given as the integral of the apparent power. The apparent power signals are accumulated in an internal 49-bit register, apparent energy register VAHR [23:0] take out this internal register [48:25] as apparent energy output. The BL6528 include a interrupt (VAPEHF) that is triggered When the apparent energy register(VAHR) is half full. If the enable VAPEHF bit in the interrupt mask register set to logic high, the / IRQ output Pin goes logic low.

Apparent power offset calibration

BL6528 contains the apparent power offset calibration (VAOS). This register is in 12-bit sign magnitude format, the default value is 000H. The offset can exist in the power calculations due to crosstalk between channels on the PCB and in the BL6528. The apparent power offset calibration allows these offsets to be removed to increase the accuracy of the measurement at low input power levels.

$$VA = VA_0 + \text{VAOS}$$

Apparent power gain adjustment

The gain register (VAGN) is used to adjust the apparent power measurement range. This register is in 12-bit sign magnitude format, the default value is 000H. The following formula shows how to adjust the output apparent power:

$$Output \quad \text{VA} = VA_0 \times (1 + \frac{\text{VAGN}}{2^{12}})$$

The minimum value that can be write to the VAGN register is 801H(HEX), which represents a gain adjustmen of -50%. The maximum value that can be write to the VAGN register is 7FFH (HEX), which represents a gain adjustmen of +50%.

Power Factor

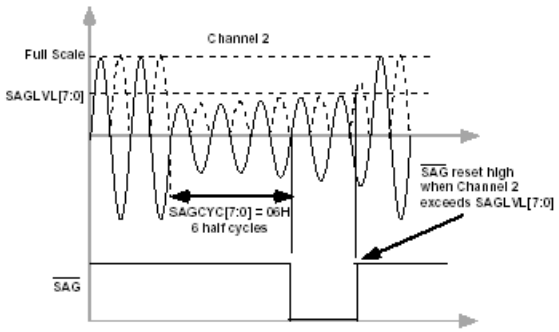
PF＝ (WATT/VA)

PF register is in 24-bit sign magnitude format. Power factor =(sign bit)*((PF[22]×2^－1）＋（PF[21]×2^－2）＋。。。), the register value of 0x7FFFFF(HEX) corresponds to a power factor value of 1, the register value of 0x800000(HEX) corresponds to a power factor of -1, the register value of 0x400000(HEX) corresponds to a power factor of 0.5.

Electric parameters monitor

Voltage Sag Detection

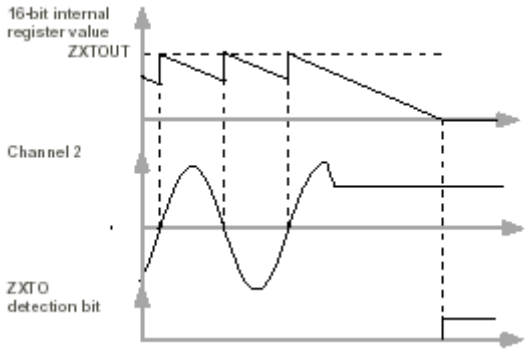
The BL6528 includes a sag detection features that warns the user when the absolute value of the line voltage falls below the programmable threshold for a programmable number of half line cycles. The voltage sag feature is controlled by two registers: SAGLVL and SAGCYC. These registers control the sag voltage threshold and the sag period, respectively.



The 12-bit SAGLVL register contains the amplitude that the voltage channel must fall below before SAG event occurs. The sag threshold is the number of half line cycles below which the voltage channel must remain before a sag condition occurs. Each LSB of the SAGCYC register corresponds to one half line cycle period. The default value is 0xFF (HEX). At 50Hz, the maximum sag cycle time is 2.55 seconds.

Zero-Crossing Timeout

The BL6528 includes a zero-crossing timeout feature that is designed to detect when no zero crossings are obtained over a programmable time period. The duration of the zero-crossing timeout is programmed in the 16-bit ZXTOUT register. The value in the ZXTOUT register is decremented by 1LSB every 70.5us. If a zero-crossing is obtained, the ZXTOUT register is reloaded. If the ZXTOUT register reaches 0, a zero-crossing timeout event is issued. The maximum programmable timeout period is 4.369 secs. A interrupt is associated with the zero-crossing timeout feature. If enabled, a zero-crossing timeout event causes the external IRQ pin to go low.



Zero-Crossing Detection

The BL6528 includes a zero-crossing detection on voltage channel. The ZX output pin goeshigh on positive-going edge of the voltage channel zero crossing.

Peak Detection

The BL6528 continuously records the maximum value of the current and voltage channels. The three registers that record the peak values on current channel A, current channel B, and the voltage channel, respectively, are IAPEAK, IBPEAK, VPEAK.

Peak monitor

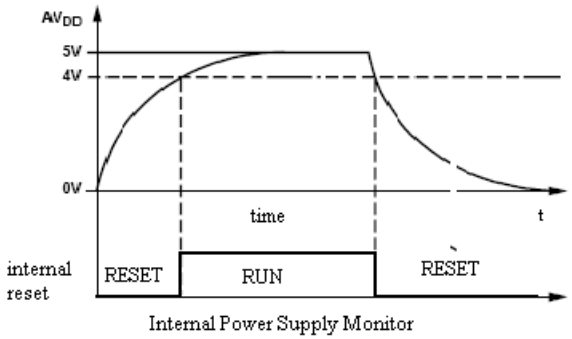
The BL6528 include an overcurrent and overvoltage feature that detects whether the absolute value of the current or voltage waveform exceeds a programmable threshold. Three peak threshold register (I_PKLVL, V_PKLVL) are used to set the current or voltage channel peak threshold, respectively.

If the BL6528 detects an overvoltage condition, the PKV bit of the interrupt status register is set to 1. If the PKV bit of the interrupt mask register is enable, the IRQ output go low. The

overcurrent detection feature works in the similar manner.

Power Supply Monitor

The BL6528 contains an on-chip power supply monitor. The analog supply (AVDD) is continuously monitored by the BL6528. if the supply is less than 4V±5%, the BL6528 will be reset. This is useful to ensure correct device startup at power-up and power-down. The power supply monitor has built in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies. The power supply and decoupling for the part should be such that the ripple at AVDD does not exceed 5V±5% as specified for normal operation.



Internal Power Supply Monitor

Communication Interface

SPI interface

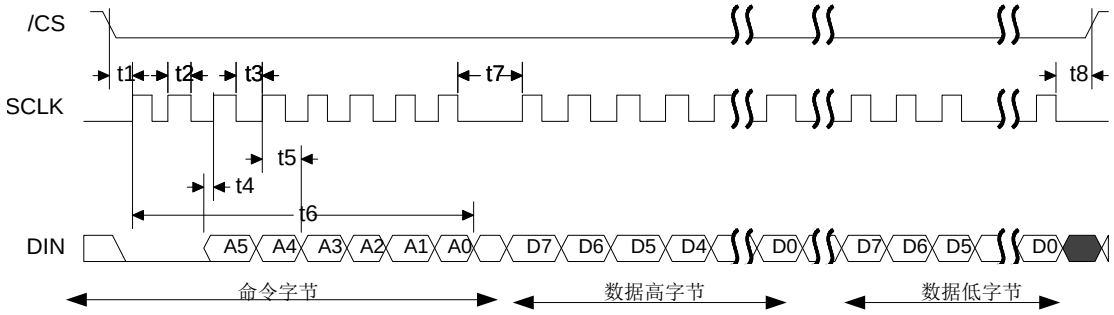
The SPI communication packet consists of an initial byte, The Bit [7:6] of this byte dictates whether a read or a write is being issued. The Bit [7:6] of this byte should be set to 00 for a read operation and to 01 for a write operation. The Bit [5:0] of this byte is the address of the register that is to be read from or written to. This byte should be transmitted MSB first. When this initial byte transmission is complete, the register data is either sent from the BL6528 on the DOUT pin (in the case of a read) or is written to the BL6528 DIN Pin by the external microcontroller (in the case of a write). All data is sent or received MSB first. The length of the data transfer is 24 bits long.

The serial peripheral interface of BL6528 uses four communication pins: SCLK, DIN, DOUT and /CS. The SPI communication operates in slave mode, a clock must be provided on the SCLK pin. This clock synchronizes all communication. The DIN pin is an input to the BL6528; data is sampled by BL6528 on the rising edge of SCLK. The DOUT pin is an output from the BL6528; data is shifted out on the rising edge of SCLK. The /CS (chip select) input must be driven low to initialize the communication and driven high at the end of the communication. Driving the /CS input high before the completion of a data transfer ends the communication.

- **SPI Write operation**

Serial write sequence is shown in the figure. The Bit[7:6] of the first bytes in DIN is 01,

indicate a write operation. The Bit[5:0] of this byte indicate the address of register. The last three bytes is the data that will be write to the register. The data written to the BL6528 should be ready before the rising edge of SLCK. The SPI interface will shift the data in the BL6528 on the rising edge of SCLK.

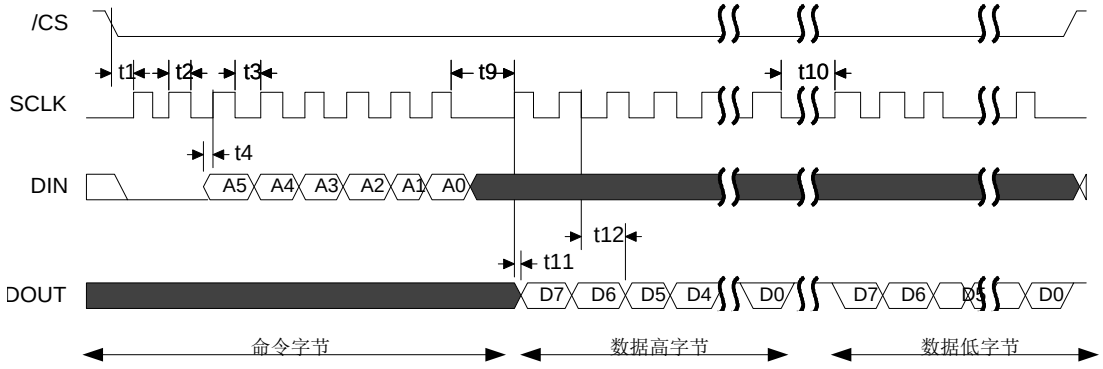


（DVDD＝5V± 5%，DGND＝0V，CLKIN＝3.58MHz XTAL，25℃）

		min	type	max	unit
t1	/CS to the rising edge of SCLK	5000			ns
t2	The high pulse width of SCLK	5000			ns
t3	The low pulse width of SCLK	5000			ns
t4	Data setup time before the rising edge of SCLK	3000			ns
t5	Data hold time after the rising edge of SCLK	2000			ns
t6	Transmission time between two bytes	80			us
t7	The minimum time interval between two bytes of data	5000			ns
t8	The minimu hold time of /CS after the falling edge of SCLK	5000			ns

◆ **SPI read operation**

Serial write sequence is shown in the figure. The Bit[7:6] of the first bytes in DIN is 00, indicate a read operation. The Bit[5:0] of this byte indicate the address of register. The data written to the BL6528 should be ready on DIN before the rising edge of SLCK. After the BL6528 receive the address of register, the BL6528 will shift out the data of the register on DOUT pin on the rising edge of SCLK.



（DVDD＝5V± 5%，DGND＝0V，CLKIN＝3.58MHz XTAL，25℃）

		min	type	max	unit
t9	The shortest interval from the End of the read command to the start of read data read	5000			ns
t10	The shortest interval between two bytes of data	5000			ns
t11	Data setup time after the rising edge of SCLK			10000	ns
t12	Data hold time after the falling edge of SCLK	5000			ns

UART

The BL6528 provides a universal asynchronous receiver/transmitter(UART) interface that allows the registers of BL6528 to be accessed using only two PIN. The UART interface operates at affixed baud rate of 4800bps. When PIN12(SEL) is logic high,PIN20(nCS) and PIN21(SCLK) are logic low, the BL6528 use the UART interface. All communication is initiated by the sending of a valid frame by the microcontroller to the BL6528.

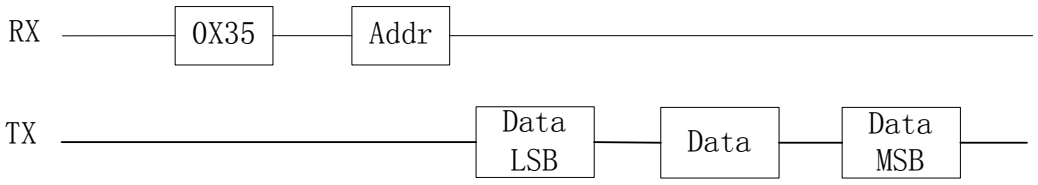
The set of UART: 4800bps, No parity, 1 stop bit.

The format of the byte:

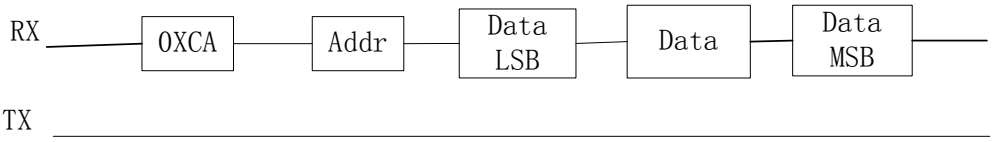
Start bit	D0	D1	D2	D3	D4	D5	D6	D7	Stop bit

The format of the frame is shown:

UART Read:



UART Write:



UART 接口参数：
通信波特率：4800bps±10%
帧错误复位时间：73.2mS

REGISTERS

Register list

ADDRESS	NAME	EXTERNAL R/W	INTERNAL R/W	BITS	DEFAULT	DESCRIPTION
ELECTRIC PARAMETERS REGISTER（INTERNAL WRITE）						
00H	VERSION	R	W	24	6528A 1H	Version No 6528A_V1
01H	I_WAVE	R	W	24	0	Wave register of current channel
02H	V_WAVE	R	W	24	0	Wave register of voltage channel
03H	I_PEAK	R	W	24	0	Current Peak register
04H	V_PEAK	R	W	24	0	Voltage Peak register
05H	I_RMS	R	W	24	0	Irms register
06H	V_RMS	R	W	24	0	Vrms register
07H	PF	R	W	24	0	Power Factor
08H	FREQ	R	W	24	0	Period of voltage channel
09H	WATT	R	W	24	0	Average active power register
0AH	VAR	R	W	24	0	Average reactive power register
0BH	VA	R	W	24	0	Average apparent power register
0CH	WATTHR	R	W	24	0	Active energy register
0DH	PWAHR	R	W	24	0	Positive active energy register
0EH	NWAHR	R	W	24	0	Negative active energy register
0FH	VARHR	R	W	24	0	Reactive energy register
10H	VAHR	R	W	24	0	Apparent energy register
11H	LINE_ WATTHR	R	W	24	0	Line accumulation active energy register
12H	LINE_ VARHR	R	W	24	0	Line accumulation reactive energy register
13H	LINE_ VAHR	R	W	24	0	Line accumulation apparent energy register
14H	STATUS	R	W	16	0	Interrupt status register
15H	Reversed					Reversed

Calibration registers (External write， Except 3AH）						
16H	BG_CTRL	R/W	R	16	9333H	Reversed
17H	GAIN	R/W	R	8	0	Channel gain register Bit[7:4] :the gain of channel voltage Bit[0:4] :the gain of channel current
18H	PHCAL_I	R/W	R	8	0	Phase calibration register(bit[7]) are enable bit,1.1us/1LSB,） Bit[6:0]:phase calibration of current
19H	PHCAL_V	R/W	R	8	0	Phase calibration register(bit[7]) are enable bit,1.1us/1LSB,） Bit[6:0]:phase calibration of voltage
1AH	I_CHOS	R/W	R	12	0	Current channel offset adjustment register
1BH	V_CHOS	R/W	R	12	0	Voltage channel offset adjustment register
1CH	I_CHGN	R/W	R	12	0	Current channel gain adjustment register
1DH	V_CHGN	R/W	R	12	0	Voltage channel gain adjustment register
1EH	I_RMSOS	R/W	R	12	0	Current RMS offset calibration register
1FH	V_RMSOS	R/W	R	12	0	Voltage RMS offset calibration register
20H	I_RMSGN	R/W	R	12	0	Current RMS gain adjust register
21H	V_RMSGN	R/W	R	12	0	Voltage RMS gain adjust register
22H	WATTOS	R/W	R	12	0	Active power offset correction register
23H	WATTGN	R/W	R	12	0	Active power gain adjustment register
24H	VAROS	R/W	R	12	0	Reactive power offset correction register
25H	VARGN	R/W	R	12	0	Reactive power gain adjustment register
26H	VAOS	R/W	R	12	0	Apparent power offset correction register
27H	VAGN	R/W	R	12	0	Apparent power gain adjustment register
28H	WA_LOS	R/W	R	12	0	Active power offset calibration register
29H	VAR_LOS	R/W	R	12	0	Reactive power offset calibration register
2AH	WA_CREEP1	R/W	R	12	02BH	Active power no-load threshold register
2BH	WA_CREEP2	R/W	R	12	FFFH	Active power no-load timer threshold register
2CH	VAR_CREPP 1	R/W	R	12	02BH	Reactive power no-load threshold register
2DH	VAR_CREEP 2	R/W	R	12	FFFH	Reactive power no-load timer threshold register

2EH	RMS_CREEP	R/W	R	12	0	RMS no-load threshold register
2FH	REVP_CREEP	R/W	R	12	087H	Reverse no-load threshold register
30H	CFDIV	R/W	R	12	001H	CF frequency divider register
31H	MODE	R/W	R	16	000H	Mode register, see the Mode register section
32H	LINECYC	R/W	R	12	000H	Line energy accumulation cycles register
33H	ZXTOUT	R/W	R	16	FFFFH	Zero-crossing timeout
34H	SAGCYC	R/W	R	8	FFH	Sag line cycle register
35H	SAGLVL	R/W	R	12	0	Sag voltage level
36H	I_PKLVL	R/W	R	12	FFFH	Current channel peak level threshold register
37H	V_PKLVL	R/W	R	12	FFFH	Voltage channel peak level threshold register
38H	MASK	R/W	R	12	0	Interrupt mask register, see the MASK register section
39H	Reversed					Reversed
3AH	Reversed					Reversed
3BH	SOFT_nrst	W	/	24		When send 5A5A5AH to this register, reset the BL6528.
Special register						
3CH	READ	R	R	24	0	Contains the data from the last read operation of SPI
3DH	WRITE	R	R	24	0	Contains the data from the last write operation of SPI
3EH	CHKSUM	R	R	24	01D50BH	Checksum. The sum of register 16H~38 value
3FH	WRPROT	R/W	R	8	0	Write protection register. write 55H, it means that allows write to writable register

Mode register（MODE[15:0]）

Bit location	Bit mnemonic	Default value	Description
0~1	WAHR_SEL	00	Energy accumulation mode selection MODE[1:0]=00, absolute energy accumulation. MODE[1:0]=01,positive-only energy accumulation. MODE[1:0]=10,arithmetical energy accumulation. MODE[1:0]=11,reserved.
2	CF2_SEL	0	CF2 output selection CF2_SEL=0, CF_VAR PIN output the pulse of reactive energy (VAR_CF).

			CF2_SEL=1, CF_VAR PIN output the pulse of apparent energy (VA_CF).
3	AntiCreep_ Sel	0	Creep mode select. AntiCreep_Sel=0, disable Time Creep mode; AntiCreep_Sel=1, enable Time Creep mode.
4	Disable_CF VAR	0	=0, Enable CF_VAR output =1,Disable CF_VAR output
5	Disable _CFWA	0	=0, Enable CF_WA output =1,Disable CF_WA output
6	I_HPF_SEL	0	=0, Enable HPF of current channel =1, Disable HPF of current channel
7	V_HPF_SE L	0	=0, Enable HPF of voltage channel =1, Disable HPF of voltage channel
8	Reversed	0	Reversed
9~11	AT0,AT1 output Sel	00	
12~13	Reversed		Reversed
14~15	Reversed	0	Reversed

MODE[11:9] is used to set the logic output function of AT0~AT1 PINs.

MODE [11：9]	**AT0 OUTPUT**	**DEFAULT**	**DESCRIPTION**
000	PKIA	0	=1, current channel peak has exceeded I_PKLVL
001	SAG	0	=1, Sag event has occurred.
010	REVP	0	=1, sign of active power has changed to negative
011	PDM_I	0	Output the current channel PDM signal
100	VAREHF	0	=1, reactive energy register(VARHR) is half full.
101	ZX	0	Voltage channel zero crossing
110	VREF_LOW	0	=1, indicate the Reference Voltage is lower than 2V
111	Reversed		Reversed

MODE [11：9]	**AT0 OUTPUT**	**DEFAULT**	**DESCRIPTION**
000	PKV	0	=1, voltage channel peak has exceeded V_PKLVL
001	ZXTO	0	=1, Zero-crossing overtime
010	REVP_VAR	0	=1, sign of reactive power has changed to negative
011	PDM_V		Output the voltage channel PDM signal
100	APEHF	0	=1, active energy register(WATTHR) is half full.
101	VAPEHF	0	=1, apparent energy register(VAHR) is half full
110	Reversed		Reversed
111	Reversed		Reversed

Interrupt mask register(MASK)

BIT LOCATION	INTERRUPT FLAG	DEFAULT	DESCRIPTION
0	SAG	0	Enable the interrupt that sag event has occurred
1	ZXTO	0	Enable the interrupt of ZXTO
2	ZX	0	Enable the interrupt of ZX
3	PKI	0	Enable the interrupt of PKI
4	PKV	0	Enable the interrupt of PKV
5	REVP	0	Enable the interrupt of REVP
6	REVP_VAR	0	Enable the interrupt of REVP_VAR
7	APEHF	0	Enable the interrupt of APEHF
8	VAREHF	0	Enable the interrupt of VARHR
9	VAPEHF	0	Enable the interrupt of VAHR
10	VREF_LOW	0	Enable the interrupt of VREF_LOW
11	Reversed		Reversed

Interrupt status register (STATUS)

BIT LOCATION	INTERRUPT FLAG	DEFAULT	DESCRIPTION
0	SAG	0	Indicates that an interrupt was caused by a Sag event
1	ZXTO	0	Indicates that zero crossing has been missing on the voltage channel for the length of time specified in the ZXTOUT register
2	ZX	0	Voltage channel zero crossing
3	PKI	0	Current channel peak has exceeded I_PKLVL
4	PKV	0	Voltage peak has exceeded V_PKILVL
5	REVP	0	Indicates the active power has gone from positive to negative
6	REVP_VAR	0	Indicates the reactive power has gone from positive to negative
7	APEHF	0	Indicates that an interrupt was caused because WATTHR register is more than half full
8	VAREHF	0	Indicates that an interrupt was caused because WARHR register is more than half full
9	VAPEHF	0	Indicates that an interrupt was caused because WAHR register is more than half full
10	VREF_LOW	0	Indicates that the reference voltage is lower than 2V

11	Reversed		Reversed