

MM54HCT76/MM74HCT76/ MM54HCT112/MM74HCT112

Dual J-K Flip-Flops with Preset and Clear

General Description

These flip-flops utilize advanced silicon-gate CMOS technology. They have input threshold and output drive similar to LS-TTL with the low standby power of CMOS.

These flip-flops have independent J, K, preset, clear and clock inputs and Q and $\bar{Q}$ outputs. The flip-flops are edge-triggered and change state on the negative-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low logic level on the corresponding input.

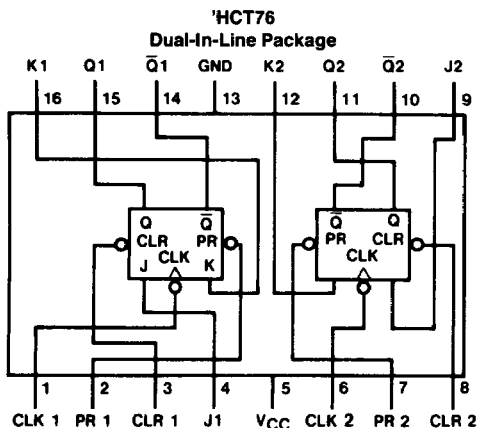
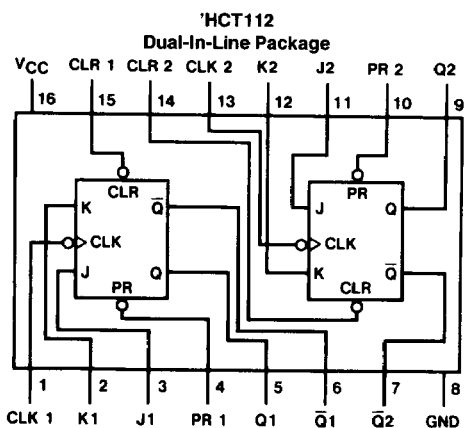
All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

MM54HCT/MM74HCT devices are intended to interface TTL and NMOS components to CMOS components. When there is a LS-TTL equivalent, these parts can be used as plug-in replacements to reduce system power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 80 μ A maximum (74HCT series)
- Fanout of 10 LS-TTL loads

Connection Diagram



TL/F/5762-1

TL/F/5762-3

Order Number **MM54HCT76/T112*** or **MM74HCT76/T112***

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	$\downarrow$	L	L	Q0	$\bar{Q}0$
H	H	$\downarrow$	H	L	H	L
H	H	$\downarrow$	L	H	L	H
H	H	$\downarrow$	H	H	Toggle	
H	H	H	X	X	Q0	$\bar{Q}0$

Note: Q0 = the level of Q before the indicated input conditions were established.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Absolute Maximum Ratings (Notes 1 and 2)

if Military/Aerospace specified devices are required,
contact the National Semiconductor Sales Office/
Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	−0.5V to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ unless otherwise specified

Symbol	Parameter	Conditions	T _A = 25°C		74HCT	54HCT	Units
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V _{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V _{OH}	Minimum High Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} = 20 μA I _{OUT} = 4.0 mA, V _{CC} = 4.5V I _{OUT} = 4.8 mA, V _{CC} = 5.5V	V _{CC} 4.2 5.2	V _{CC} − 0.1 3.98 4.98	V _{CC} − 0.1 3.84 4.84	V _{CC} − 0.1 3.7 4.7	V V V
V _{OL}	Maximum Low Level Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} = 20 μA I _{OUT} = 4.0 mA, V _{CC} = 4.5V I _{OUT} = 4.8 mA, V _{CC} = 5.5V	0 0.2 0.2	0.1 0.26 0.26	0.1 0.33 0.33	0.1 0.4 0.4	V V V
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND, V _{IH} or V _{IL}		± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA V _{IN} = 2.4V or 0.5V (Note 4)		4.0 0.3	40 0.4	80 0.5	μA mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics $V_{CC} = 5V, T_A = 25^\circ\text{C}, C_L = 15 \text{ pF}, t_r = t_f = 6 \text{ ns}$

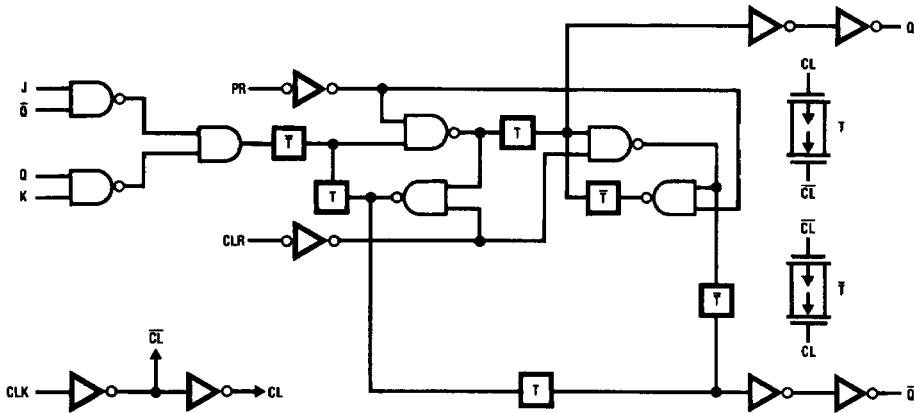
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\bar{Q}$		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\bar{Q}$		18	30	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			20	ns
t_S	Minimum Set-Up Time J or K Clock		10	20	ns
t_H	Minimum Hold Time Clock to J or K		−3	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $C_L = 50\text{ pF}$, $t_r = t_f = 6\text{ ns}$ unless otherwise specified

Symbol	Parameter	Conditions	T _A = 25°C		74HCT T _A = −40°C to 85°C	54HCT T _A = −55°C to 125°C	Units
			Typ	Guaranteed Limits			
f _{MAX}	Maximum Operating Frequency			27	22	18	MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay from Clock to Q or $\bar{Q}$		22	35	44	52	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\bar{Q}$		22	35	44	52	ns
t _{REM}	Minimum Removal Time Preset or Clear to Clock			20	25	30	ns
t _S	Minimum Setup Time J or K to Clock		10	20	25	30	ns
t _H	Minimum Hold Time Clock to J or K		−3	0	0	0	ns
t _W	Minimum Pulse Width Clock, Preset or Clear			16	20	24	ns
t _r , t _f	Maximum Clock Input Rise and Fall Time			500	500	500	ns
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C _{PD}	Power Dissipation Capacitance (Note 5)	(Per Flip-Flop)	35				pF
C _{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



TL/F/5762-2