

MH4M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 150994944-BIT (4194304-WORD BY 36-BIT) DYNAMIC RAM

DESCRIPTION

The MH4M365CXJ/CNXJ is 4194304-word x 36-bits dynamic RAM. This consists of eight industry standard 4M x 4 dynamic RAMs in SOJ and four industry 4M x 1 dynamic RAMs in SOJ.

The mounting of SOJ on a single in-line package provides any application where high densities and large quantities of memory are required. This is a socket-type memory module, suitable for easy interchange or addition of modules.

FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
MH4M365CXJ/CNXJ-5	50	13	25	90	7240
MH4M365CXJ/CNXJ-6	60	15	30	110	5920
MH4M365CXJ/CNXJ-7	70	20	35	130	5200

- 72pin single in-line package
- Single 5.0V $\pm$ 10% supply
- Low stand-by power dissipation
44mW (Max) ----- CMOS Input level
- Low operating power dissipation
MH4M365CXJ/CNXJ- 5 ----- 9.15W (Max)
MH4M365CXJ/CNXJ- 6 ----- 7.48W (Max)
MH4M365CXJ/CNXJ- 7 ----- 6.51W (Max)
- Hyper-page mode , $\overline{\text{RAS}}$ -only refresh , $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh capabilities
- All inputs and output directly TTL compatible
2048 refresh cycles every 32ms ($A_0 \sim A_{10}$)
- MH4M365CXJ ----- Gold plating
- MH4M365CNXJ ----- Nickel+solder plating

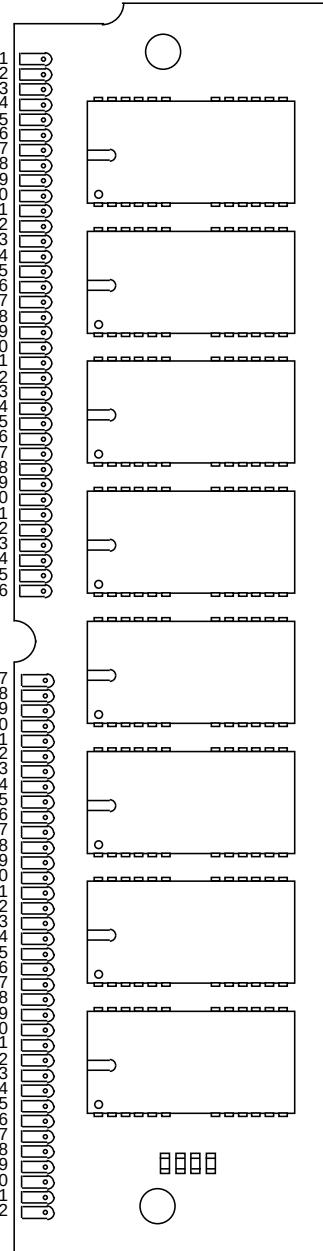
APPLICATION

Main memory unit for computers, Microcomputer memory,
Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)

[Double side]

1.Vss	37.MP1
2.DQ0	38.MP3
3.DQ16	39.Vss
4.DQ1	40.CAS0
5.DQ17	41.CAS2
6.DQ2	42.CAS3
7.DQ18	43.CAS1
8.DQ3	44.RAS0
11.NC	45.NC
10.Vcc	46.NC
11.NC	47.W
12.A0	48.NC
13.A1	49.DQ8
14.A2	50.DQ24
15.A3	51.DQ9
16.A4	52.DQ25
17.A5	53.DQ10
18.A6	54.DQ26
19.A10	55.DQ11
20.DQ4	56.DQ27
21.DQ20	57.DQ12
22.DQ5	58.DQ28
23.DQ21	59.Vcc
24.DQ6	60.DQ29
25.DQ22	61.DQ13
26.DQ7	62.DQ30
27.DQ23	63.DQ14
28.A7	64.DQ31
29.NC	65.DQ15
30.Vcc	66.NC
31.A8	67.PD1
32.A9	68.PD2
33.NC	69.PD3
34.RAS2	70.PD4
35.MP2	71.NC
36.MP0	72.Vss



Outline 72N9D-C

	- 5	- 6	- 7
PD1	Vss	Vss	Vss
PD2	NC	NC	NC
PD3	Vss	NC	Vss
PD4	Vss	NC	NC

NC: NO CONNECTION

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FUNCTION

in addition to normal read, write, a number of other functions, e.g., hyper page mode, RAS only refresh,

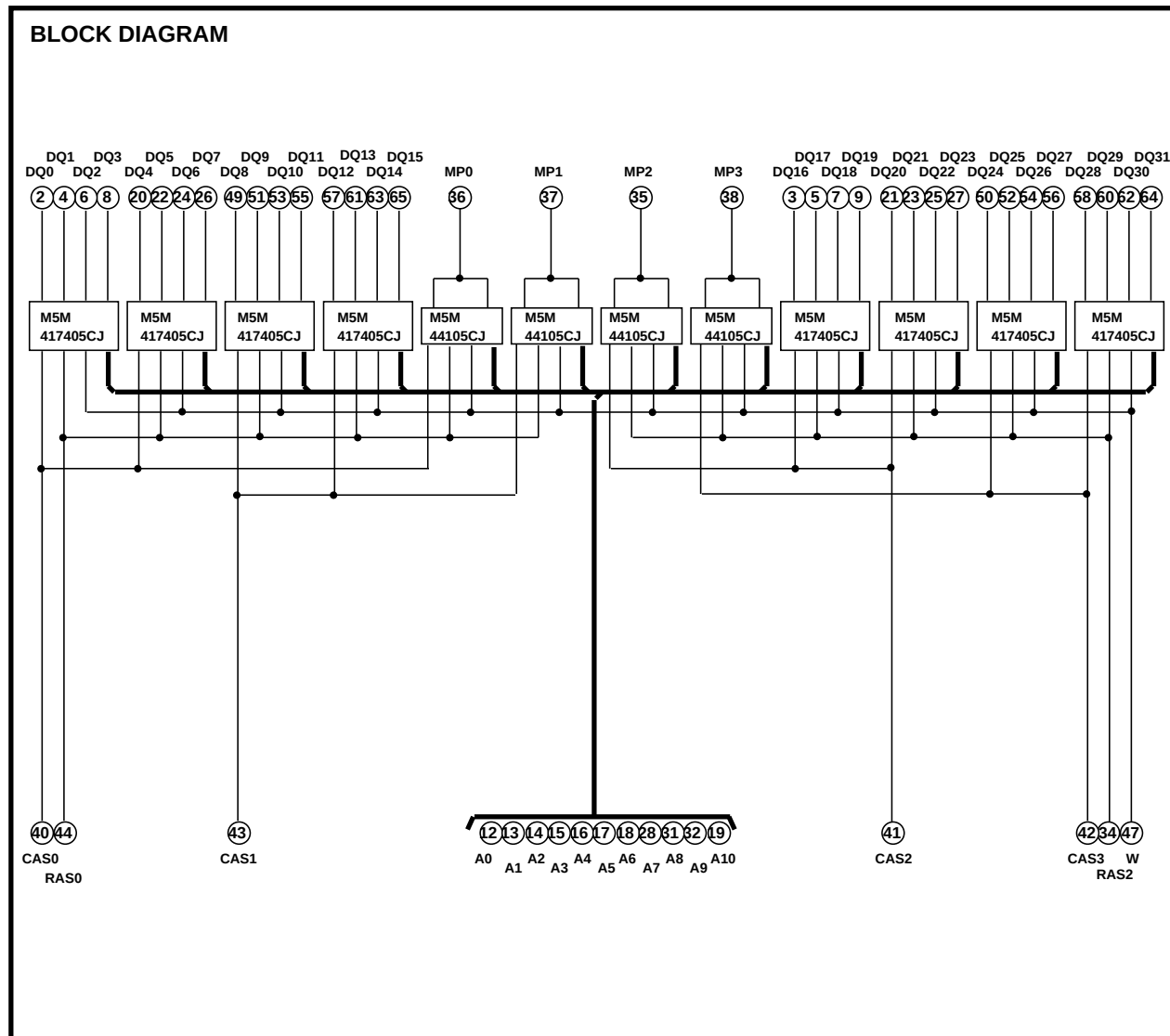
The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	RAS	CAS	W	Row address	Column address	Input	Output
Read	ACT	ACT	NAC	APD	APD	OPN	VLD
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN
RAS-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN
Hidden refresh	ACT	ACT	NAC	APD	DNC	OPN	VLD
CAS before RAS refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-1 ~ 7	V
V _I	Input voltage		-1 ~ 7	V
V _O	Output voltage		-1 ~ 7	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a =25°C	12	W
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg}	Storage temperature		-40 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS (T_a=0 ~ 70 °C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		5.5	V
V _{IL}	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (T_a=0 ~ 70°C, V_{CC}=5.0V ± 10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V _{OH}	High-level output voltage		I _{OH} =-5.0mA	2.4		V _{CC}	V
V _{OL}	Low-level output voltage		I _{OL} =4.2mA	0		0.4	V
I _{OZ}	Off-state output current		Q floating 0V ≤ V _{OUT} ≤ 5.5V	-20		20	μA
I _I	Input current		0V ≤ V _{IN} ≤ 6 V, Other inputs pins=0V	-120		120	μA
I _{CC1} (AV)	Average supply current from V _{CC} operating (Note 3,4,5)	MH4M365C -5	RAS, CAS cycling trc=twc=min. output open			1660	mA
		MH4M365C -6				1360	
		MH4M365C -7				1180	
I _{CC2}	Supply current from V _{CC} , stand-by (Note 6)		RAS= CAS =V _{IH} , output open			24	mA
			RAS= CAS ≥ V _{CC} - 0.2 V			8	
I _{CC3} (AV)	Average supply current from V _{CC} refreshing (Note 3,5)	MH4M365C -5	RAS cycling, CAS= V _{IH} trc=min. output open			1660	mA
		MH4M365C -6				1360	
		MH4M365C -7				1180	
I _{CC4} (AV)	Average supply current from V _{CC} Hyper-Page-Mode (Note 3,4,5)	MH4M365C -5	RAS=V _{IL} , CAS cycling tpc=min. output open			1620	mA
		MH4M365C -6				1320	
		MH4M365C -7				1060	
I _{CC6} (AV)	Average supply current from V _{CC} CAS before RAS refresh mode (Note 3)	MH4M365C -5	CAS before RAS refresh cycling trc=min. output open			1580	mA
		MH4M365C -6				1300	
		MH4M365C -7				1140	

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while RAS=V_{IL} and CAS=V_{IH}.

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CAPACITANCE (Ta=0 ~ 70 °C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{I(A)}	Input capacitance, address inputs	V _I =V _{SS} f=1MHz V _I =25mVrms			78	pF
C _{I(W)}	Input capacitance, write control input				84	pF
C _{I(RAS)}	Input capacitance, RAS input				42	pF
C _{I(CAS)}	Input capacitance, CAS input				42	pF
C _{I/O}	Input/Output capacitance, data ports				22	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70 °C, Vcc = 5V ± 10%, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter	Limits						Unit
		MH4M365C -5		MH4M365C -6		MH4M365C -7		
		Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{\text{CAS}}$ (Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{\text{RAS}}$ (Note 7,9)		50		60		70	ns
tAA	Column address access time (Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{\text{CAS}}$ precharge (Note 7,11)		30		35		40	ns
tOHC	Output hold time from $\overline{\text{CAS}}$	5		5		5		ns
tOHR	Output hold time from $\overline{\text{RAS}}$ (Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{\text{CAS}}$ low (Note 7)	5		5		5		ns
tWEZ	Output disable time after $\overline{\text{WE}}$ high (Note 12)		13		15		20	ns
tOFF	Output disable time after $\overline{\text{CAS}}$ high (Note 12,13)		13		15		20	ns
tREZ	Output disable time after $\overline{\text{RAS}}$ high (Note 12,13)		13		15		20	ns

Note 6: An initial pause of 500μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a RAS clock such as RAS-Only refresh).

Note the RAS may be cycled during the initial pause. And any 8 RAS or RAS/CAS cycles are required after prolonged periods (greater than 32 ms) of RAS inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V_{OH}=2.4V(I_{OH}=-5mA) / V_{OL}=0.4V(I_{OL}=-4.2mA) load 100pF.

The reference levels for measuring of output signal are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that t_{RCD} ≥ t_{RCD(max)} and t_{ASC} ≥ t_{ASC(max)} and t_{CP} ≥ t_{CP(max)}.

9: Assumes that t_{RCD} ≥ t_{RCD(max)} and t_{RAD} ≥ t_{RAD(max)}. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that t_{RAD} ≥ t_{RAD(max)} and t_{ASC} ≥ t_{ASC(max)}.

11: Assumes that t_{CP} ≥ t_{CP(max)} and t_{ASC} ≥ t_{ASC(max)}.

12: t_{WEZ(max)}, t_{OFF(max)} and t_{REZ(max)} defines the time at which the output achieves the high impedance state (I_{OUT} ≤ I ± 10 μA) and is not reference to V_{OH(min)} or V_{OL(max)}.

13: Output is disabled after both RAS and CAS go to high.

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TIMING REQUIREMENTS (For Read, Write, Refresh, and Hyper-Page Mode Cycles)

(Ta=0 ~ 70°C, Vcc = 5V ± 10%, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits						Unit
		MH4M365C -5		MH4M365C -6		MH4M365C -7		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		32		32		32	ms
tRP	RAS high pulse width	30		40		50		ns
tRCD	Delay time, RAS low to CAS low (Note16)	18	37	20	45	20	50	ns
tCRP	Delay time, CAS high to RAS low	5		5		5		ns
tRPC	Delay time, RAS high to CAS low	0		0		0		ns
tCPN	CAS high pulse width	8		10		13		ns
tRAD	Column address delay time from RAS low (Note17)	13	25	15	30	15	35	ns
tASR	Row address setup time before RAS low	0		0		0		ns
tASC	Column address setup time before CAS low (Note18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after RAS low	8		10		10		ns
tCAH	Column address hold time after CAS low	8		10		10		ns
tT	Transition time (Note19)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed $t_r = 3\text{ns}$.

15: $V_{IH(\text{min})}$ and $V_{IL(\text{max})}$ are reference levels for measuring timing of input signals.

16: $t_{RCD(\text{max})}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(\text{max})}$, access time is t_{RAC} . If t_{RCD} is greater than $t_{RCD(\text{max})}$, access time is controlled exclusively by t_{CAC} or t_{AA} .

17: $t_{RAD(\text{max})}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(\text{max})}$ and $t_{ASC} \geq t_{ASC(\text{max})}$, access time is controlled exclusively by t_{AA} .

18: $t_{ASC(\text{max})}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(\text{max})}$ and $t_{ASC} \geq t_{ASC(\text{max})}$, access time is controlled exclusively by t_{CAC} .

19: t_r is measured between $V_{IH(\text{min})}$ and $V_{IL(\text{max})}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		MH4M365C -5		MH4M365C -6		MH4M365C -7		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	8	10000	10	10000	13	10000	ns
tCSH	CAS hold time after RAS low	40		48		55		ns
tRSH	RAS hold time after CAS low	13		15		20		ns
tRCS	Read Setup time before CAS low	0		0		0		ns
tRCH	Read hold time after CAS high (Note 20)	0		0		0		ns
tRRH	Read hold time after RAS high (Note 20)	0		0		0		ns
tRAL	Column address to RAS hold time	25		30		35		ns
tCAL	Column address to CAS hold time	13		18		23		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

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Write Cycle (Early Write)

Symbol	Parameter	Limits						Unit
		MH4M365C -5		MH4M365C -6		MH1M365C -7		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	8	10000	10	10000	13	10000	ns
tCSH	CAS hold time after RAS low	40		48		55		ns
tRSH	RAS hold time after CAS low	13		15		20		ns
tWCS	Write setup time before CAS low	0		0		0		ns
tWCH	Write hold time after CAS low	8		10		13		ns
tWP	Write pulse width	8		10		13		ns
tDS	Data setup time before CAS low or W low	0		0		0		ns
tDH	Data hold time after CAS low or W low	8		10		13		ns

Hyper page Mode Cycle (Read, Early Write, Hi-Z control by $\overline{W}$) (Note 21)

Symbol	Parameter	Limits						Unit
		MH4M365C -5		MH4M365C -6		MH4M365C -7		
		Min	Max	Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time	20		25		30		ns
tDOH	Output hold time from $\overline{\text{CAS}}$ low	5		5		5		ns
tRAS	RAS low pulse width for read write cycle (Note22)	65	100000	77	100000	92	100000	ns
tCP	CAS high pulse width (Note23)	8	13	10	16	13	16	ns
tCPRH	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ precharge	28		33		38		ns
tWPE	$\overline{\text{W}}$ Pulse Width (Hi-Z control)	7		7		7		ns

Note 21: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

22: tRAS(min) is specified as two cycles of $\overline{CAS}$ input are performed.

23: tCP(max) is specified as a reference point only.

$\overline{CAS}$ before RAS Refresh Cycle (Note 24)

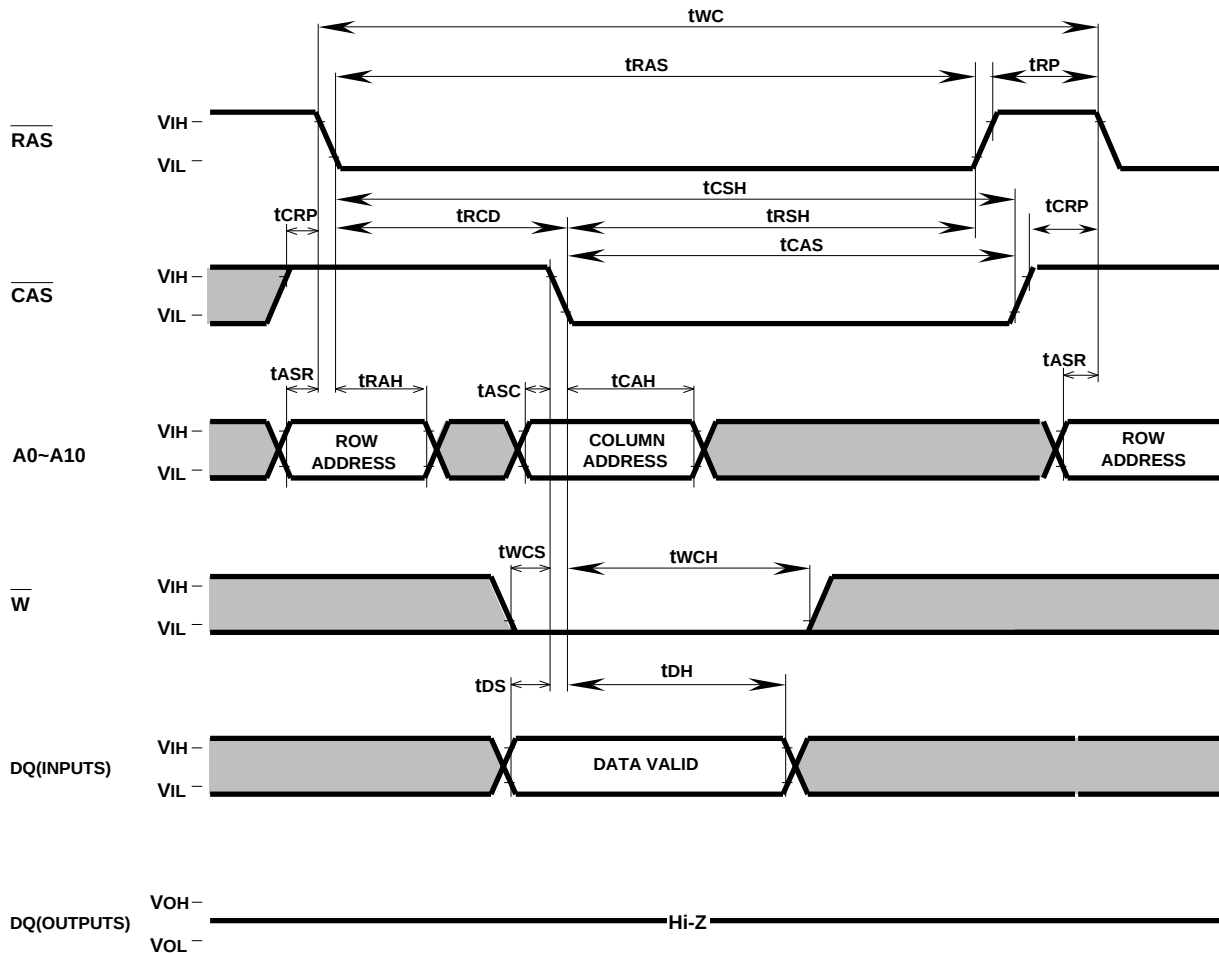
Symbol	Parameter	Limits						Unit
		MH1M365C -5		MH1M365C -6		MH1M365C -7		
		Min	Max	Min	Max	Min	Max	
tCSR	CAS setup time before RAS low	5		5		5		ns
tCHR	CAS hold time after RAS low	10		10		15		ns

Note 24: Eight or more $\overline{CAS}$ before RAS cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before RAS refresh mode.

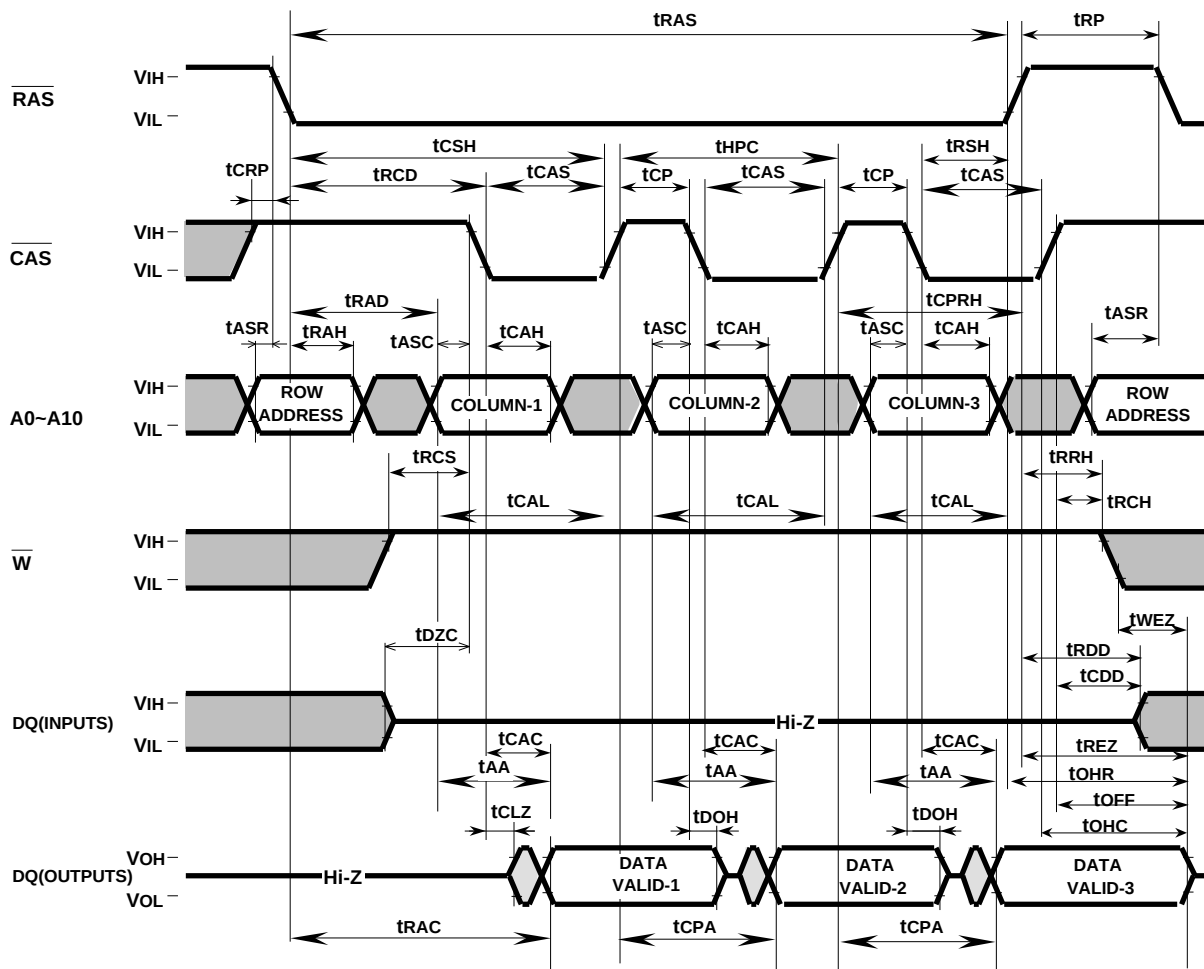
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Early Write Cycle



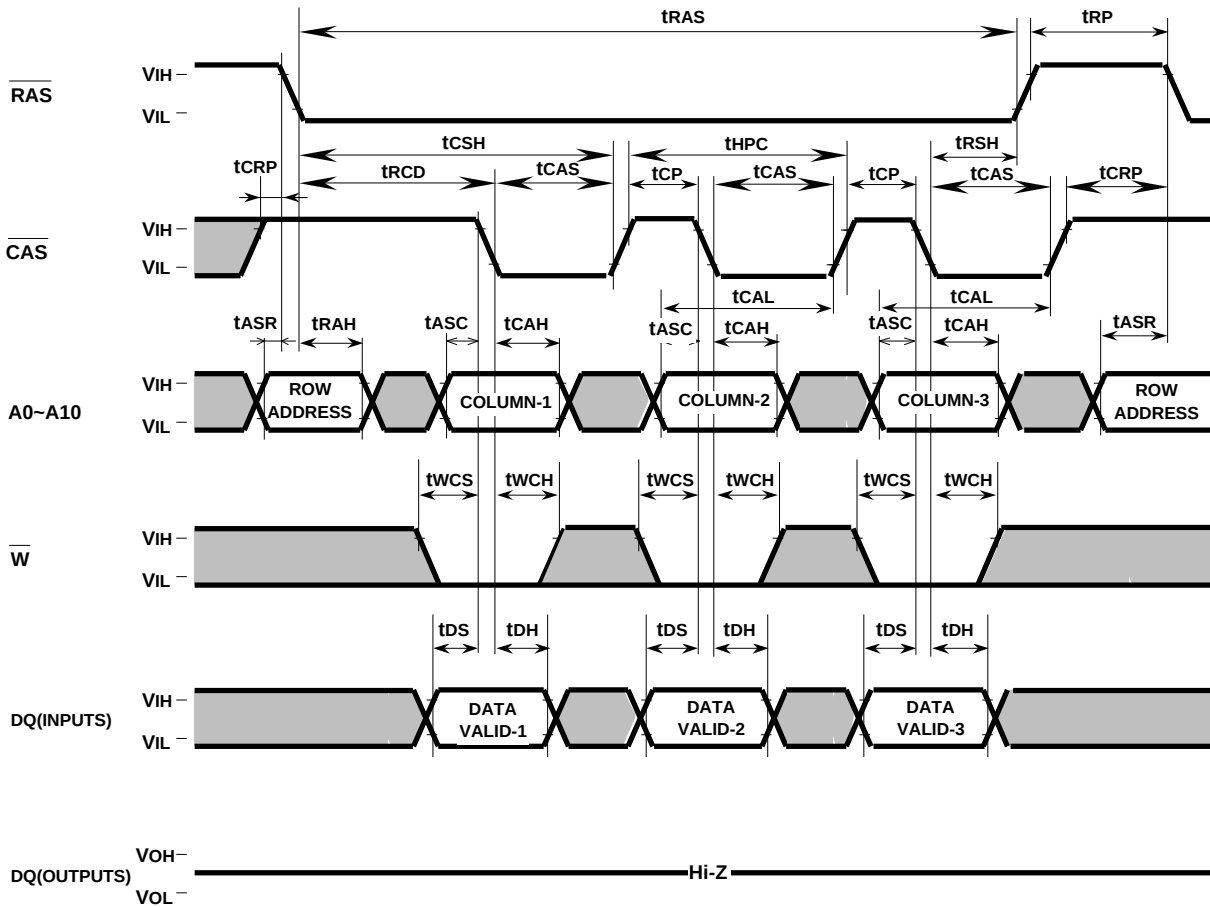
Hyper Page Mode Read Cycle



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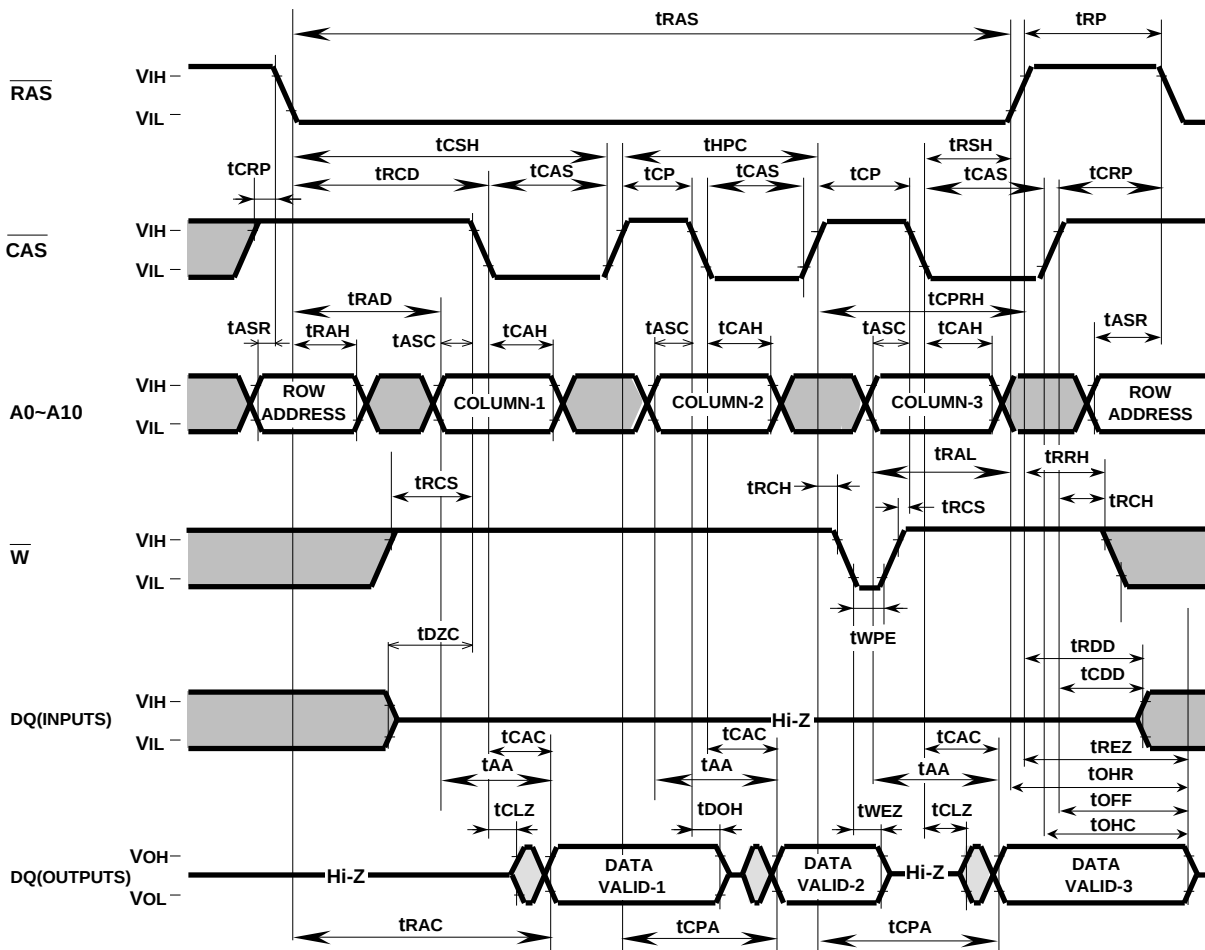
Hyper Page Mode Early Write Cycle



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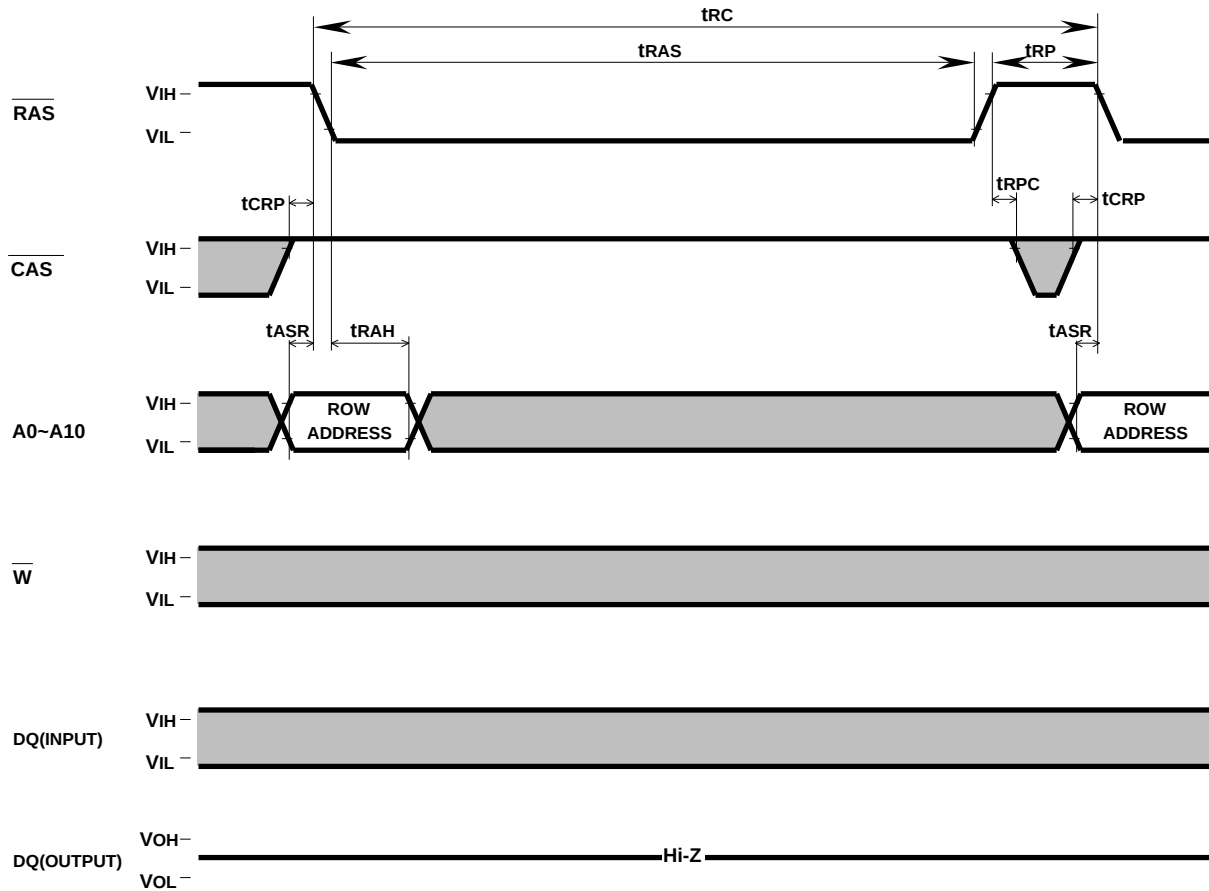
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



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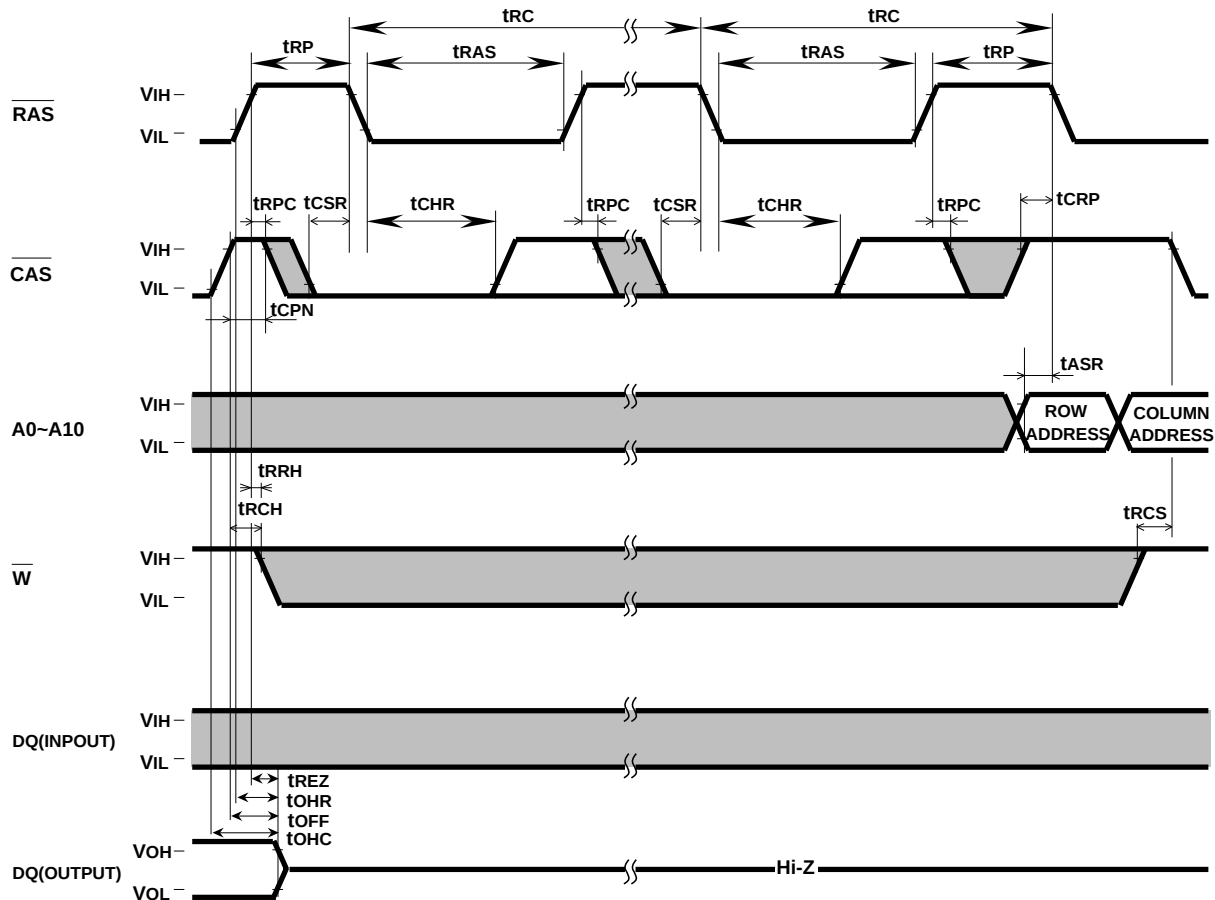
RAS-only Refresh Cycle



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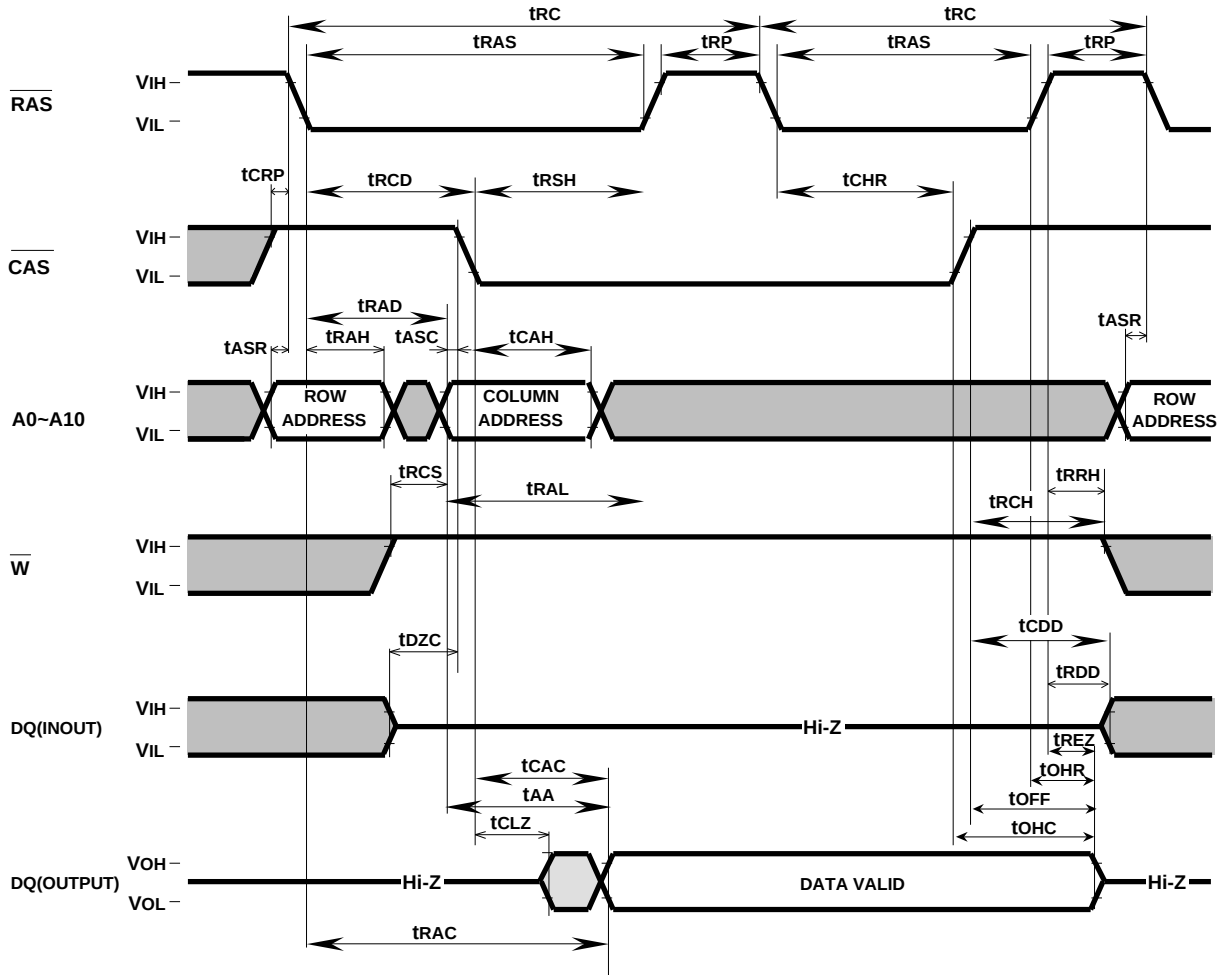
CAS before RAS Refresh Cycle



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Hidden Refresh Cycle (Read) (Note 26)



Note 26: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

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72pin DRAM Module Outline

