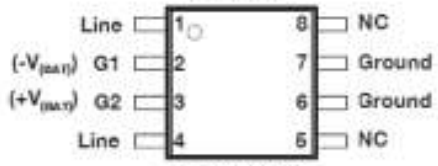
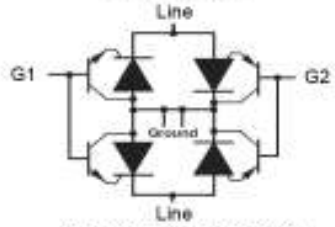
Feature

- High Performance Protection for SLICs with +ve and –ve Battery Supplies
- Wide -110 V to +110 V Programming Range
- Low 5 mA max. Gate Triggering Current
- Dynamic Protection Performance Specified for International Surge Waveshapes

8-SOIC



Pin Define



Schematic Diagram

Application

- Wireless Local Loop
- Access Equipment
- Regenerated POTS
- VOIP Applications
- VoIP

Description

The SVG110S is a programmable overvoltage protection device designed to protect modern dual polarity supply rail ringing SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line. Overvoltages can be caused by lightning, a.c. power contact and induction. Four separate protection structures are used, two positive and two negative to provide optimum protection during Metallic(Differential) and Longitudinal (Common Mode) protection conditions in both polarities. Dynamic protection performance is specified under typical international surge waveforms from Telcordia GR-1089-CORE, ITU-T K.44 and YD/T 950.

Absolute Maximum Ratings

(T_A=25℃, Unless otherwise specified.)

Parameter	Symbol	Value	Unit
Non-repetitive peak impulse current [1, 2, 3, 4] 10/1000μS (Telcordia GR-1089-CORE) 5/310μS (ITU-T K.20, K.21 ,K.45, K.44 wave shape 10/700s) 2/10μS (Telcordia GR-1089-CORE)	I_{PPSM}	±30 ±45 ±100	A
Non-repetitive peak on-state current, 50 Hz / 60 Hz [1, 2, 3, 5] 0.2s 1s 900s	I_{TSM}	9.0 5.0 1.7	A
Repetitive peak off-state voltage $V_{G1(Line)}$ = 0, V_{G2} ≥ +5 V $V_{G2(Line)}$ = 0, V_{G1} ≥ -5 V	V_{DRM}	-120 +120	V
Maximum negative battery supply voltage	V_{G1M}	-110	V
Maximum positive battery supply voltage	V_{G2M}	+110	V
Maximum differential battery supply voltage	△V(BAT)M	220	V
Junction temperature	T_J	-40 to +150	℃
Storage temperature range	T_{STG}	-65 to +150	℃
Junction to ambient thermal resistance [6]	$R_{\theta JA}$	55 (Typ.)	℃/W

Notes:

1. Initially the device must be in thermal equilibrium with TJ = 25 °C. The surge may be repeated after the device returns to its initial conditions.
2. The rated current values may be applied to either of the Line to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of a single terminal pair).
3. Rated currents only apply if pins 6 & 7 (Ground) are connected together.
4. Applies for the following bias conditions: VG1 = -20 V to -110 V, VG2 = 0 V to +110 V.
5. EIA/JESD51-2 environment and EIA/JESD51-7 high effective thermal conductivity test board (multi-layer) connected with 0.6 mm printed wiring track widths.
6. EIA/JESD51-2 Environment, P_{TOT} = 4W ,EIA/JESD51-7 high effective thermal conductivity test board (multi-layer) connected with 0.6 mm printed wiring track widths.

Electrical Characteristics

(T_A=25℃, Unless otherwise specified.)

Parameter	Symbols	Conditions	Min	Typ	Max	Units
Off-state current	I_D	VD = V_{DRM}, $V_{G1(Line)}$ = 0, V_{G2} ≥ +5 V; T_A = 25℃			-5	µA
		VD = V_{DRM}, $V_{G1(Line)}$ = 0, V_{G2} ≥ +5 V; T_A = 85℃			-50	µA
		VD = V_{DRM}, $V_{G2(Line)}$ = 0, V_{G1} ≥ -5 V; T_A = 25℃			+5	µA
		VD = V_{DRM}, $V_{G2(Line)}$ = 0, V_{G1} ≥ -5 V; T_A = 85℃			+50	µA
Negative-gate leakage current	$I_{G1(Line)}$	$V_{G1(Line)}$ = -220 V			-5	µA
Positive-gate leakage current	$I_{G2(Line)}$	$V_{G2(Line)}$ = +220 V			+5	µA
Gate-Line impulse breakover voltage	$V_{G1L(BO)}$	V_{G1}= -100V, I_T= -100 A [7] 2/10 µs			-15	V
		V_{G1}= -100V, I_T= -30 A 10/1000µs			-11	V
Gate-Line impulse breakover voltage	$V_{G2L(BO)}$	V_{G1}= +100V, I_T= +100 A [7] 2/10 µs			+15	V
		V_{G1}= +100V, I_T= +30 A 10/1000µs			+11	V
Negative holding current	I_H	V_{G1}= -60 V, I_T= -1A, di/dt= 1A/ms	-150			mA
Negative-gate trigger current	I_{G1T}	I_T = -5A, tp(g) ≥ 20µs, V_{G1} = -60V			+5	mA
Positive-gate trigger current	I_{G2T}	I_T = 5A, tp(g) ≥ 20µs, V_{G2} = 60V			-5	mA
Line - Ground off-state capacitance	C_O	f = 1MHz, VD = -3V, G1 & G2 open circuit		32		pF

Typical Characteristic Curves

Fig.1 Off-state capacitance vs off-state voltage

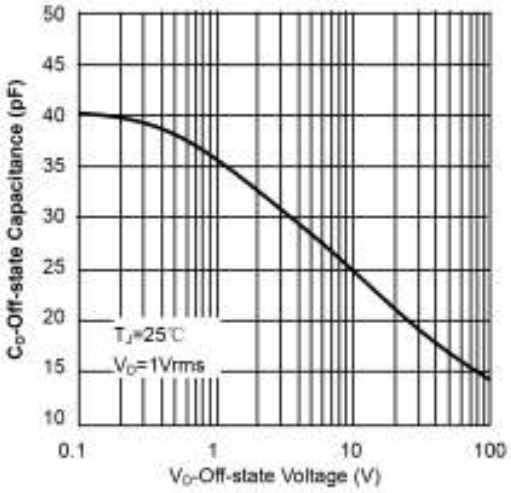
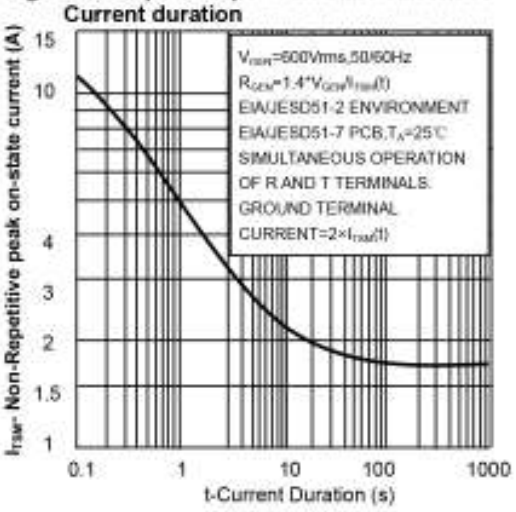
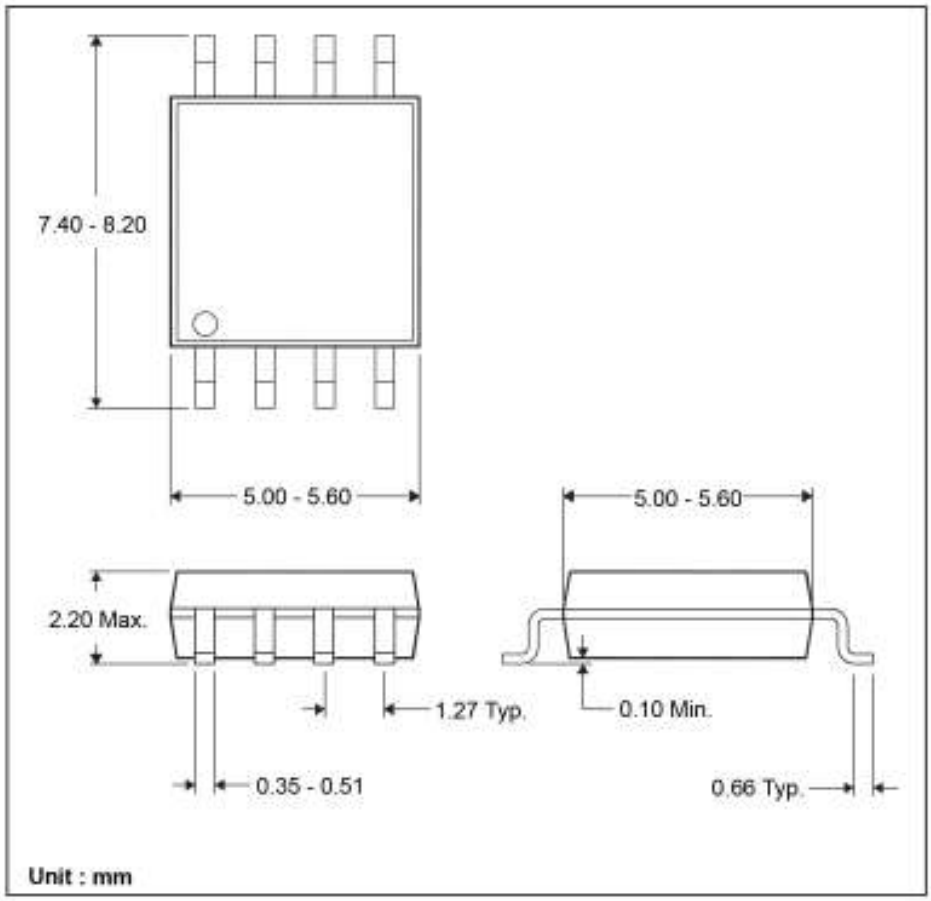


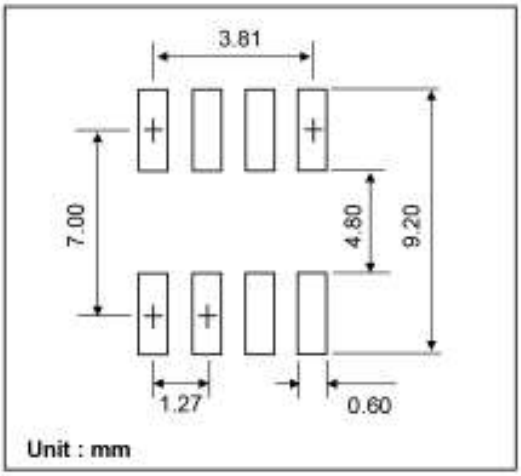
Fig.2 Non-Repetitive peak on-state current vs Current duration



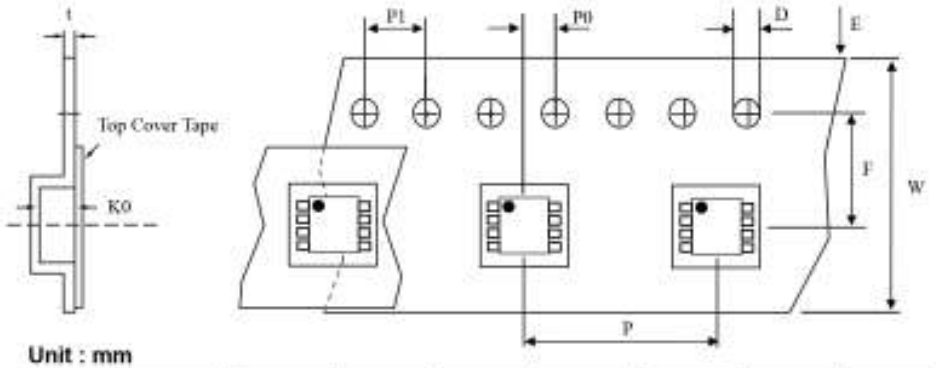
Product Dimension



PAD Dimension



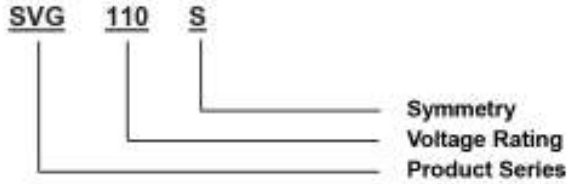
Package Informations



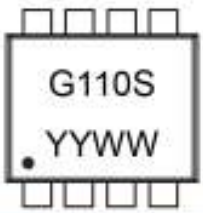
Unit : mm

K0	D	E	F	W	P0	P1	P	t
2.40±0.10	1.55± 0.05	1.75± 0.10	7.50±0.10	16.00±0.30	2.00± 0.10	4.00±0.10	12.00± 0.10	0.30± 0.10

Part Number System



Marking



YYWW : Date Code