INA27x Voltage Output, Unidirectional Measurement Current-Shunt Monitor

1 Features

- Wide Common-Mode Range: –16 V to +80 V
- CMRR: 120 dB
- Accuracy:
  ±0.5-mV Offset (typ)
  ±0.2% Gain Error (typ)
  2.5 µV/°C Offset Drift (typ)
  50 ppm/°C Gain Drift (max)
- Bandwidth: Up to 130 kHz
- Two Gain Options Available:
  14 V/V (INA270)
  20 V/V (INA271)
- Quiescent Current: 700 µA (typ)
- Power Supply: +2.7 V to +18 V
- Provision for Filtering

2 Applications

- Power Management
- Automotive
- Telecom Equipment
- Notebook Computers
- Battery Chargers
- Cell Phones
- Welding Equipment

3 Description

The INA270 and INA271 family of voltage-output, current-sense amplifiers can sense drops across shunt resistors at common-mode voltages from –16 V to +80 V, independent of the supply voltage. The INA270 and INA271 pinouts readily enable filtering.

The INA270 and INA271 are available with two gain options: 14 V/V and 20 V/V. The 130-kHz bandwidth simplifies use in current-control loops.

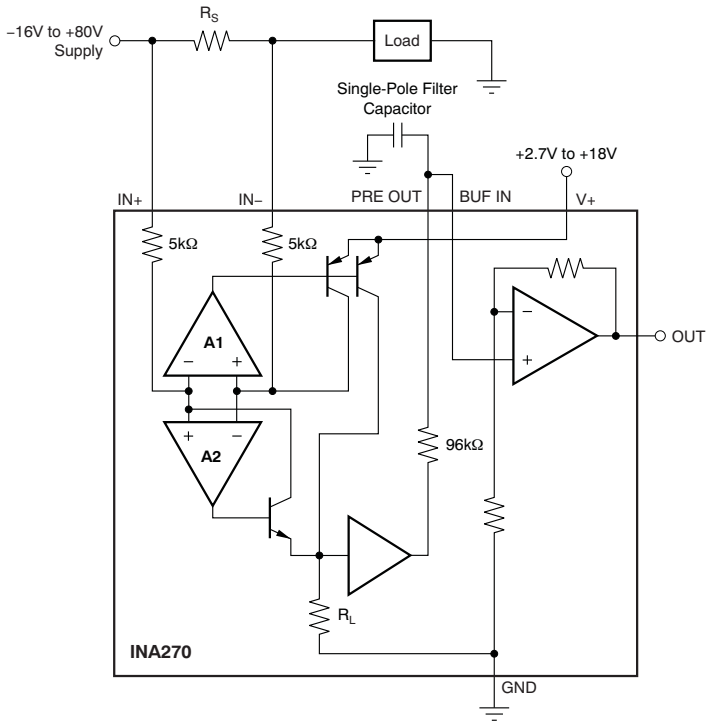
The INA270 and INA271 operate from a single +2.7-V to +18-V supply, drawing 700 µA (typical) of supply current. The devices are specified over the extended operating temperature range of –40°C to +125°C and are offered in an SOIC-8 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA27x	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (November 2014) to Revision E	Page
• Added title to page 1 figure	1
• Updated *ESD Ratings* table to current standards	4
• Changed Figure 16: changed op amp input to BUF IN pin from negative to positive	12
• Added *Community Resources* section	19

Changes from Revision C (May 2010) to Revision D	Page
• Changed format to meet latest data sheet standards	1
• Added *Handling Rating*, *Pin Descriptions*, and *Recommended Operating Conditions* tables and *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1
• Changed *Accuracy* and *Quiescent Current* Features bullets: changed from max specifications and values to typical	1
• Changed wording in *Two Gain Options Available* Features bullet	1
• Changed *Description* section for clarification	1
• Added Device Information table	1
• Deleted Ordering Information table	3
• Changed Input, *Full-Scale Input Voltage* parameter conditions in Electrical Characteristics table	5
• Changed title of *First- or Second-Order Filtering* section	12
• Changed title of *Power Supply Recommendations* section	17

Changes from Revision B (July 2008) to Revision C	Page
• Corrected Figure 17 y-axis	14
• Corrected Figure 18 y-axis	14

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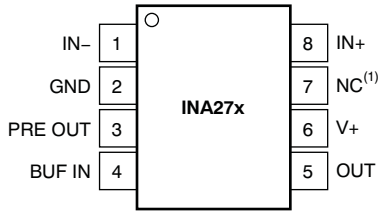
5 Device Comparison Table

DEVICE	GAIN
INA270	14 V/V
INA271	20 V/V

6 Pin Configuration and Functions

D Package
SOIC-8
Top View



NOTE (1): NC denotes no internal connection.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BUF IN	4	Analog input	Connect to output of filter from PRE OUT
GND	2	Analog	Ground
IN–	1	Analog input	Connect to load side of shunt resistor
IN+	8	Analog input	Connect to supply side of shunt resistor
NC	7	—	Connect to ground
OUT	5	Analog output	Output voltage
PRE OUT	3	Analog output	Connect to input of filter to BUF IN
V+	6	Analog input	Power supply, +2.7 V to +18 V

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Supply voltage (V_S)			+18	V
Analog inputs, V_{IN+}, V_{IN-}:	Differential, (V_{IN+}) – (V_{IN-})	–18	+18	V
	Common-mode	–16	+80	V
Analog output: OUT and PRE OUT pins		GND – 0.3	(V+) + 0.3	V
Input current into any pin			5	mA
Operating temperature		–55	+150	°C
Junction temperature			+150	°C
Storage temperature, T_{stg}		–65	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	–16	12	80	V
V_S	Operating supply voltage	2.7	5	18	V
T_A	Operating free-air temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		INA27x D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

At T_A = +25°C, V_S = +5 V, V_{CM} = +12 V, V_{SENSE} = 100 mV, and PRE OUT connected to BUF IN, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V_{SENSE}	Full-scale input voltage		$V_{SENSE} = (V_{IN+}) – (V_{IN–})$		0.15	(V_S – 0.2) / Gain	V
V_{CM}	Common-mode input range		T_A = –40°C to +125°C	–16		+80	V
CMRR	Common-mode rejection ratio		V_{IN+} = –16 V to +80 V	80	120		dB
	CMRR over temperature		V_{IN+} = +12 V to +80 V, T_A = –40°C to +125°C	100	120		dB
V_{OS}	Offset voltage, RTI(1)				±0.5	2.5	mV
	V_{OS} over temperature		T_A = –40°C to +125°C			±3	mV
dV_{OS}/dT	V_{OS} vs temperature		T_A = –40°C to +125°C		2.5	20	µV/°C
PSR	V_{OS} vs power-supply		V_S = +2.7 V to +18 V, V_{CM} = +18 V, T_A = –40°C to +125°C		5	100	µV/V
I_B	Input bias current, $V_{IN–}$ pin		T_A = –40°C to +125°C		±8	±16	µA
	PRE OUT output impedance(2)				96		kΩ
	Buffer input bias current				–50		nA
	Buffer input bias current temperature coefficient				±0.03		nA/°C
OUTPUT (V_{SENSE} ≥ 20mV)(3)							
G	Gain	INA270 total gain			14		V/V
		INA271 total gain			20		V/V
G_{BUF}	Output buffer gain				2		V/V
	Total gain error		V_{SENSE} = 20 mV to 100 mV		±0.2%	±1%	
	Total gain error Over temperature		T_A = –40°C to +125°C			±2%	
	Total gain error vs temperature		T_A = –40°C to +125°C			50	ppm/°C
	Total output error(4)				±0.75%	±2.2%	
	Total output error		T_A = –40°C to +125°C		±1.0%	±3.0%	
	Nonlinearity error		V_{SENSE} = 20 mV to 100 mV		±0.002%		
R_O	Output impedance, pin 5				1.5		Ω
	Maximum capacitive load		No sustained oscillation		10		nF
VOLTAGE OUTPUT(5) (R_L = 10 kΩ to GND)							
	Swing to V+ power-supply rail		T_A = –40°C to +125°C		(V+) – 0.05	(V+) – 0.2	V
	Swing to GND(6)		T_A = –40°C to +125°C		V_{GND} + 0.003	V_{GND} + 0.05	V
FREQUENCY RESPONSE							
BW	Bandwidth		C_{LOAD} = 5 pF		130		kHz
	Phase margin		C_{LOAD} < 10 nF		40		Degrees
SR	Slew rate				1		V/µs
t_S	Settling time (1%)		V_{SENSE} = 10 mV to 100 mV_{PP}, C_{LOAD} = 5 pF		2		µs

(1) RTI means *Referred-to-Input*.
(2) Initial resistor variation is ±30% with an additional –2200-ppm/°C temperature coefficient.
(3) For output behavior when V_{SENSE} < 20 mV, see the *Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage* section.
(4) Total output error includes effects of gain error and V_{OS}.
(5) See typical characteristic curve *Output Swing vs Output Current* and the *Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage* section.
(6) Ensured by design; not production tested.

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Electrical Characteristics (continued)

At T_A = +25°C, V_S = +5 V, V_{CM} = +12 V, V_{SENSE} = 100 mV, and PRE OUT connected to BUF IN, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NOISE, RTI[(1)]						
e_n	Voltage noise density			40		nV/√Hz
POWER SUPPLY						
V_S	Operating range	T_A = –40°C to +125°C	+2.7		+18	V
I_Q	Quiescent current	V_{OUT} = 2 V		700	900	µA
	I_Q over temperature	V_{SENSE} = 0 mV, T_A = –40°C to +125°C		350	950	µA
TEMPERATURE RANGE						
	Specified temperature range		–40		+125	°C
	Operating temperature range		–55		+150	°C
θ_{JA}	Thermal resistance, SO-8			150		°C/W

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7.6 Typical Characteristics

At T_A = +25°C, V_S = +12 V, V_{CM} = 12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

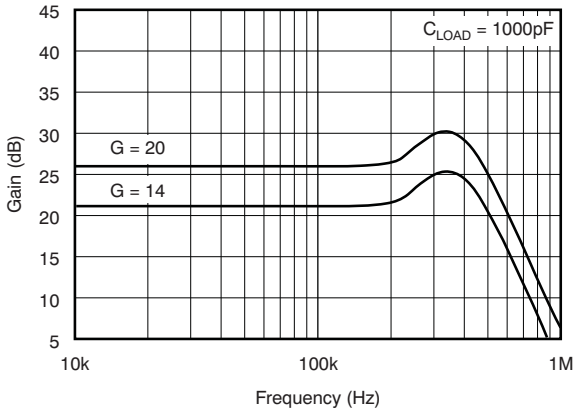

Figure 1. Gain vs Frequency

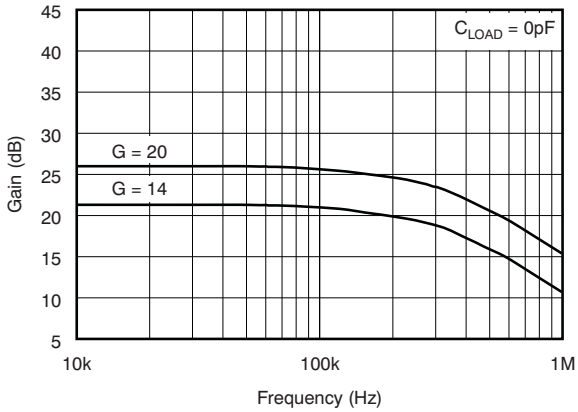

Figure 2. Gain vs Frequency

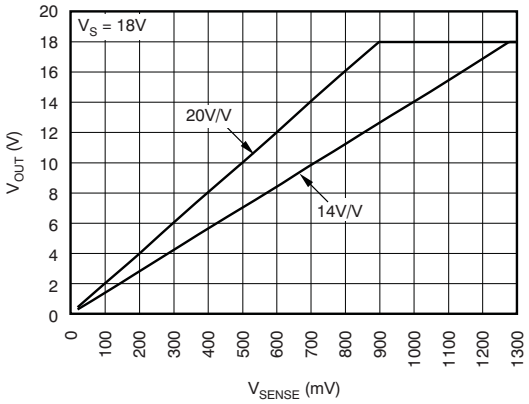

Figure 3. Gain Plot

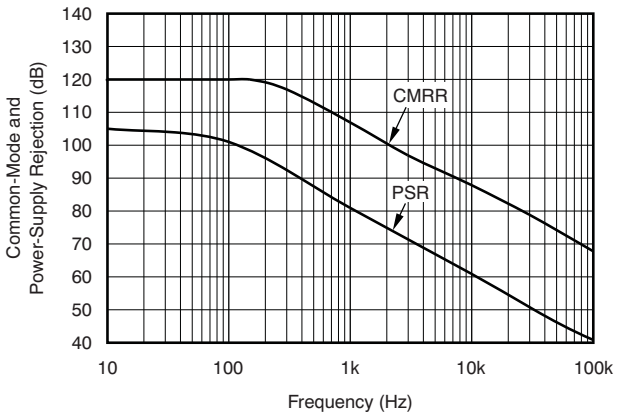

Figure 4. Common-Mode and Power-Supply Rejection vs Frequency

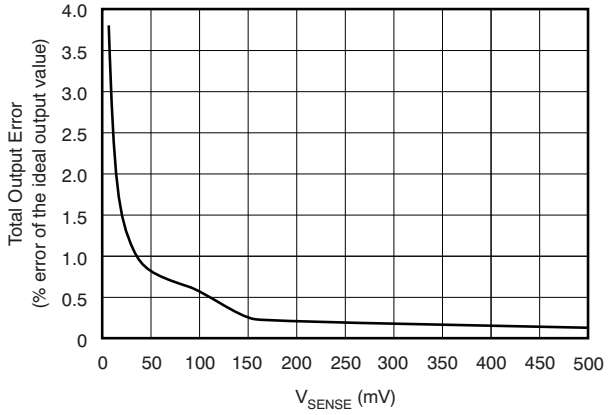

Figure 5. Total Output Error vs V_{SENSE}

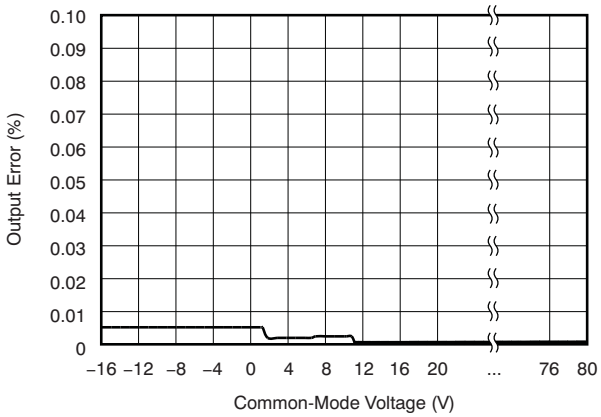

Figure 6. Output Error vs Common-Mode Voltage

Typical Characteristics (continued)

At T_A = +25°C, V_S = +12 V, V_{CM} = 12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

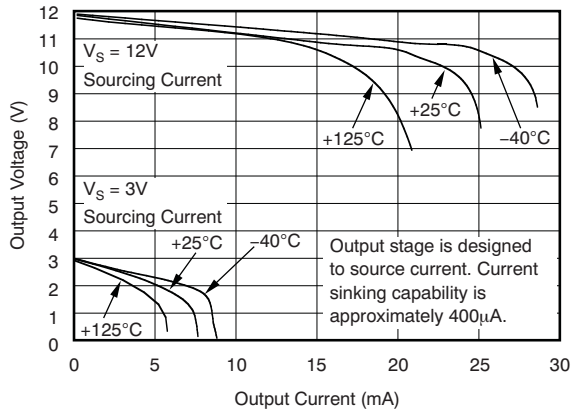

Figure 7. Positive Output Voltage Swing vs Output Current

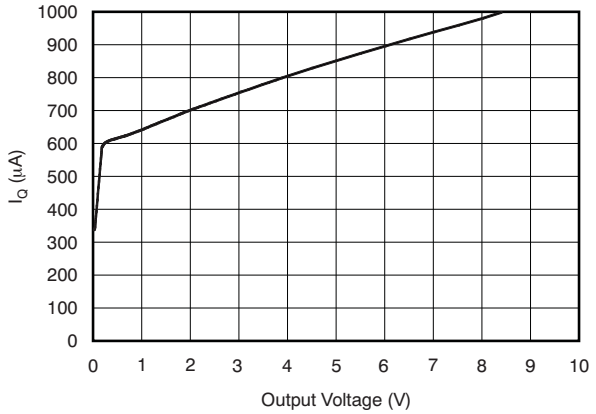

Figure 8. Quiescent Current vs Output Voltage

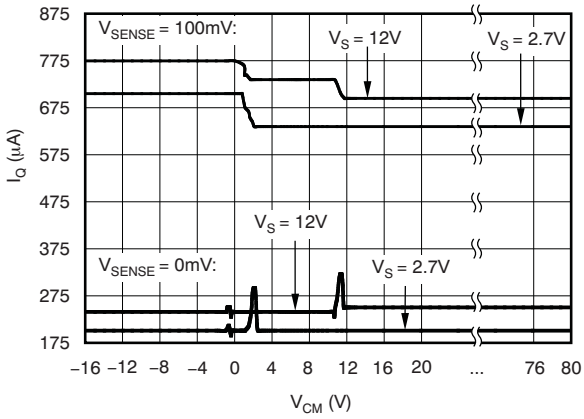

Figure 9. Quiescent Current vs Common-Mode Voltage

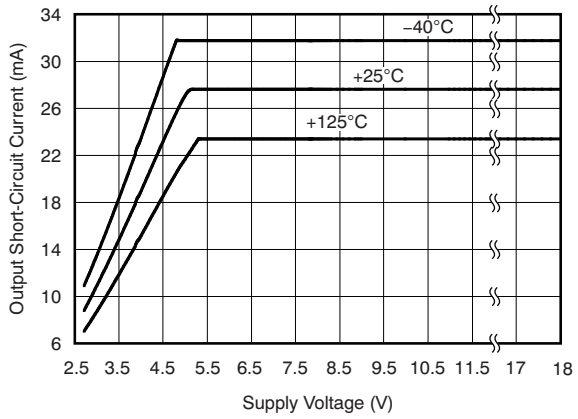

Figure 10. Output Short-Circuit Current vs Supply Voltage

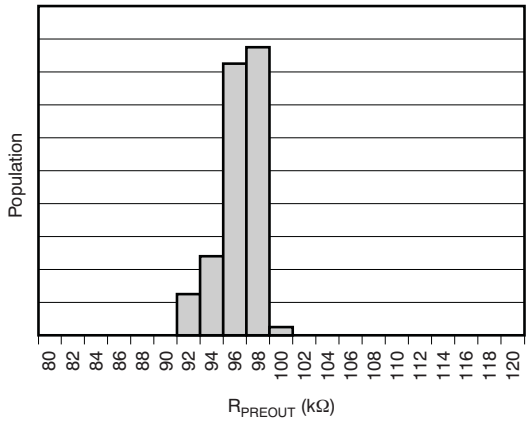

Figure 11. PRE OUT Output Resistance Production Distribution

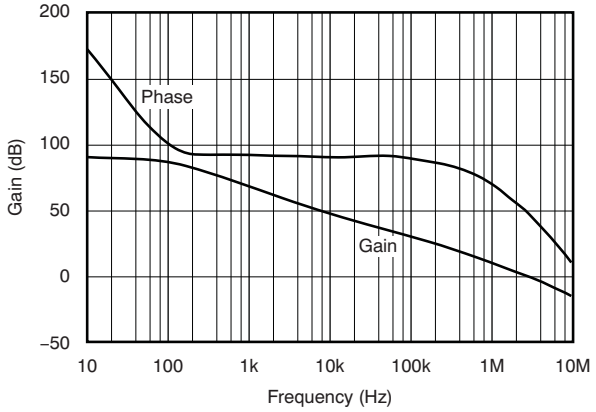

Figure 12. Buffer Gain vs Frequency

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Typical Characteristics (continued)

At T_A = +25°C, V_S = +12 V, V_{CM} = 12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

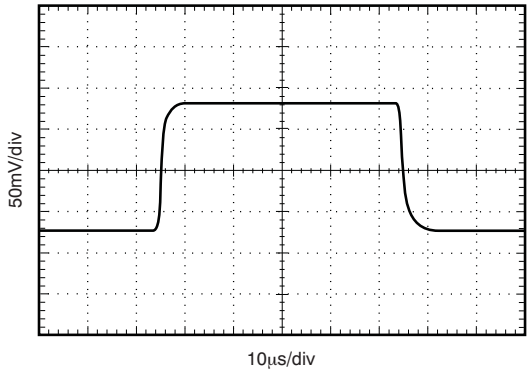


Figure 13. Small-Signal Step Response (10-mV to 20-mV Input)

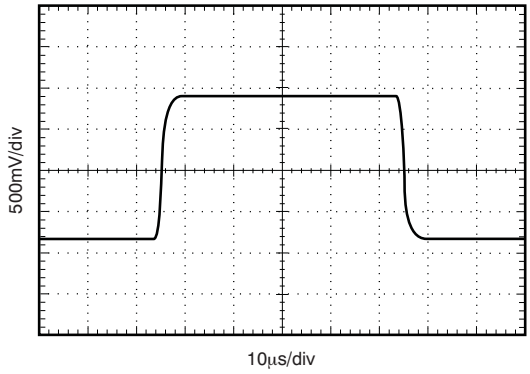


Figure 14. Large-Signal Step Response (10-mV to 100-mV Input)

8 Detailed Description

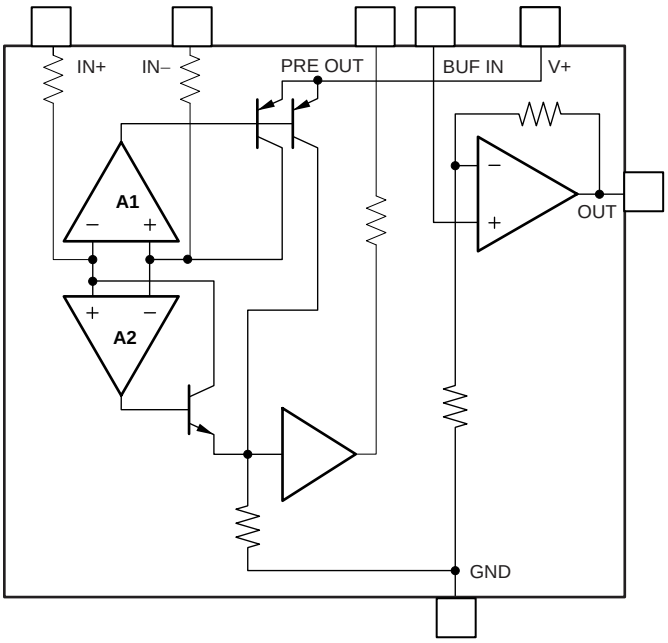
8.1 Overview

The INA270 and INA271 family of current-shunt monitors with voltage output can sense drops across current shunts at common-mode voltages from –16 V to +80 V, independent of the supply voltage. The INA270 and INA271 pinouts readily enable filtering.

The INA270 and INA271 are available with two output voltage scales: 14 V/V and 20 V/V. The 130-kHz bandwidth simplifies use in current-control loops.

The INA270 and INA271 operate from a single +2.7-V to +18-V supply, drawing a maximum of 900 μA of supply current. The devices are specified over the extended operating temperature range of –40°C to +125°C and are offered in an SOIC-8 package.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Basic Connection

Figure 15 shows the basic connection of the INA270 and INA271. Connect the input pins (IN+ and IN–) as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Place minimum bypass capacitors of 0.01 μF and 0.1 μF in value close to the supply pins. Although not mandatory, an additional 10-mF electrolytic capacitor placed in parallel with the other bypass capacitors may be useful in applications with particularly noisy supplies.

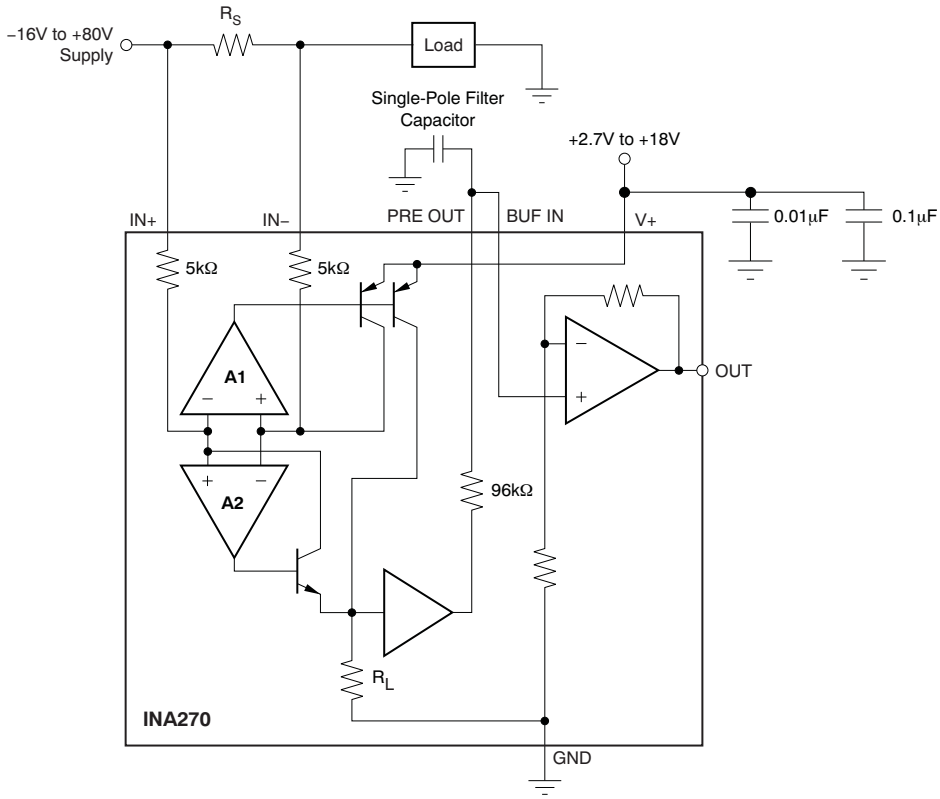


Figure 15. INA270 Basic Connections

8.3.2 Selecting R_S

The value chosen for the shunt resistor, R_S, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_S provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_S minimize voltage loss in the supply line. For most applications, best performance is attained with an R_S value that provides a full-scale shunt voltage range of 50 mV to 100 mV. Maximum input voltage for accurate measurements is (V_S – 0.2) / Gain.

8.3.3 Transient Protection

The –16-V to +80-V common-mode range of the INA270 and INA271 is ideal for withstanding automotive fault conditions ranging from 12-V battery reversal up to +80-V transients because no additional protective components are needed up to those levels. In the event that the INA270 and INA271 are exposed to transients on the inputs in excess of their ratings, external transient absorption with semiconductor transient absorbers (zeners or Transzorbs) are necessary.

Feature Description (continued)

Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it never allows the INA270 and INA271 to be exposed to transients greater than 80 V (that is, allow for transient absorber tolerance, as well as additional voltage because of transient absorber dynamic impedance). Despite the use of internal zener-type ESD protection, the INA270 and INA271 are not suited to using external resistors in series with the inputs because the internal gain resistors can vary up to ±30%, but are tightly matched (if gain accuracy is not important, then resistors can be added in series with the INA270 and INA271 inputs with two equal resistors on each input).

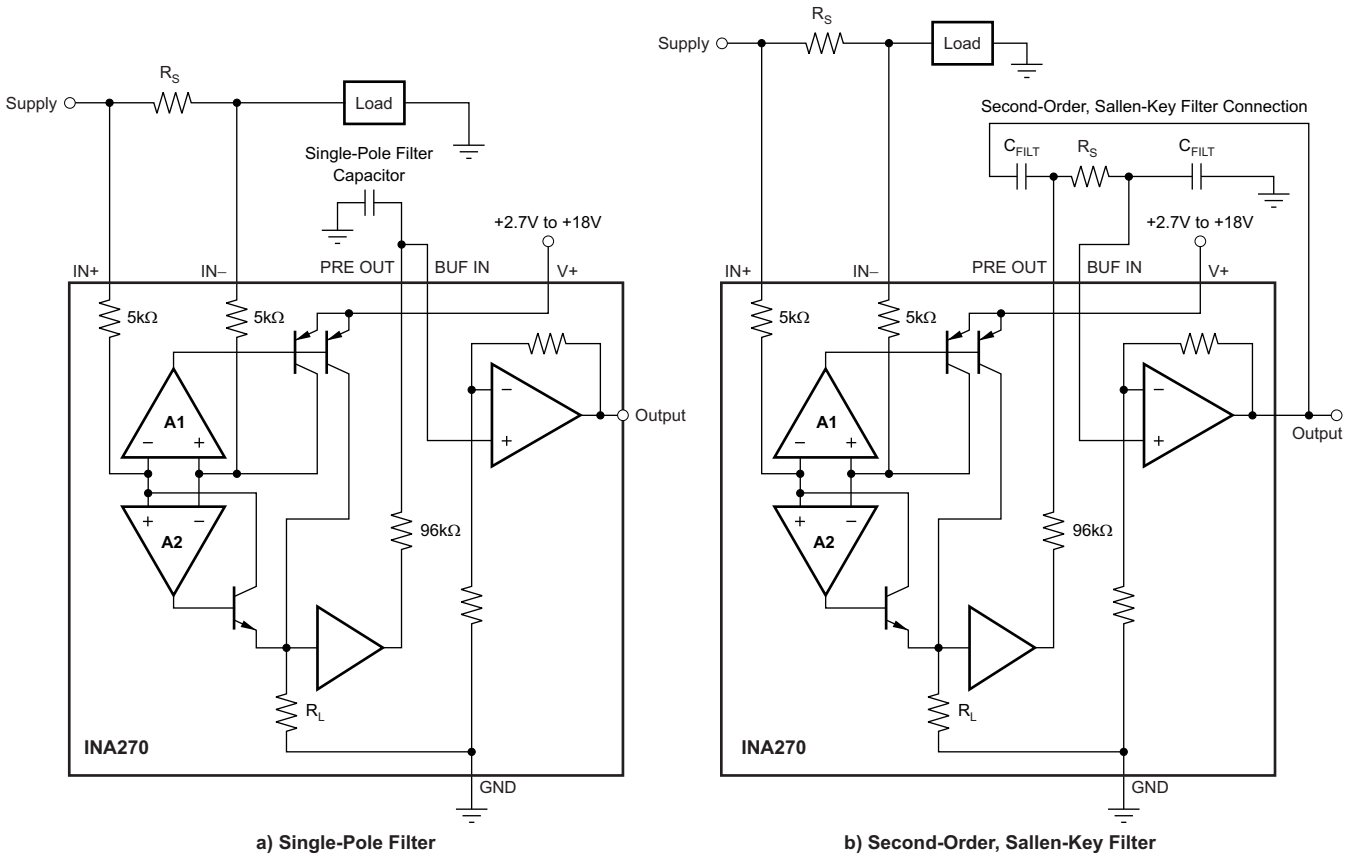
8.4 Device Functional Modes

8.4.1 First- or Second-Order Filtering

The output of the INA270 and INA271 is accurate within the output voltage swing range set by the power-supply pin, V+.

The INA270 and INA271 readily enable the inclusion of filtering between the preamp output and buffer input. Single-pole filtering can be accomplished with a single capacitor because of the 96-kΩ output impedance at PRE OUT on pin 3, as shown in Figure 16a.

The INA270 and INA271 readily lend themselves to second-order Sallen-Key configurations, as shown in Figure 16b. When designing these configurations consider that the PRE OUT 96-kΩ output impedance exhibits an initial variation of ±30% with the addition of a –2200-ppm/°C temperature coefficient.



NOTE: Remember to use the appropriate buffer gain (INA270 = 1.4, INA271 = 2) when designing Sallen-Key configurations.

Figure 16. The INA270–INA271 can be Easily Connected for First- or Second-Order Filtering

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Device Functional Modes (continued)

8.4.2 Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage

The accuracy of the INA270 and INA271 current shunt monitors is a function of two main variables: V_{SENSE} ($V_{IN+} – V_{IN–}$) and common-mode voltage (V_{CM}) relative to the supply voltage, V_S. V_{CM} is expressed as (V_{IN+} + $V_{IN–}$) / 2; however, in practice, V_{CM} is used as the voltage at V_{IN+} because the voltage drop across V_{SENSE} is usually small.

This section addresses the accuracy of these specific operating regions:

Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$
Normal Case 2: $V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$
Low V_{SENSE} Case 1:
$V_{SENSE} < 20$ mV, $–16 \text{ V} \leq V_{CM} < 0$
Low V_{SENSE} Case 2:
$V_{SENSE} < 20$ mV, $0 \text{ V} \leq V_{CM} \leq V_S$
Low V_{SENSE} Case 3:
$V_{SENSE} < 20$ mV, $V_S < V_{CM} \leq 80$ V

8.4.2.1 Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by Equation 1.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100\text{mV} - 20\text{mV}}$$

where

- V_{OUT1} = Output voltage with V_{SENSE} = 100 mV and
- V_{OUT2} = Output voltage with V_{SENSE} = 20 mV. (1)

Then the offset voltage is measured at V_{SENSE} = 100 mV and referred to the input (RTI) of the current shunt monitor, as shown in Equation 2.

$$V_{OS}\text{RTI (Referred-To-Input)} = \left(\frac{V_{OUT1}}{G}\right) - 100\text{mV} \quad (2)$$

In the *Typical Characteristics*, the *Output Error vs Common-Mode Voltage* curve (Figure 6) shows the highest accuracy for the this region of operation. In this plot, V_S = 12 V; for $V_{CM} \geq 12$ V, the output error is at its minimum. This case is also used to create the $V_{SENSE} \geq 20$ mV output specifications in the *Electrical Characteristics* table.

8.4.2.2 Normal Case 2: $V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode operating area in which the device functions, as illustrated in the *Output Error vs Common-Mode Voltage* curve (Figure 6). As noted, for this graph V_S = 12 V; for $V_{CM} < 12$ V, the output error increases when V_{CM} becomes less than 12 V, with a typical maximum error of 0.005% at the most negative V_{CM} = –16 V.

8.4.2.3 Low V_{SENSE} Case 1: $V_{SENSE} < 20$ mV, $–16 \text{ V} \leq V_{CM} < 0$; and Low V_{SENSE} Case 3: $V_{SENSE} < 20$ mV, $V_S < V_{CM} \leq 80$ V

Although the INA270 family of devices are not designed for accurate operation in either of these regions, some applications are exposed to these conditions. For example, when monitoring power supplies that are switched on and off while V_S is still applied to the INA270 or INA271, knowing what the behavior of the devices is in these regions is important.

Device Functional Modes (continued)

When V_{SENSE} approaches 0 mV, in these V_{CM} regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of V_{OUT} = 60 mV for V_{SENSE} = 0 mV. When V_{SENSE} approaches 20 mV, V_{OUT} returns to the expected output value with accuracy as specified in the *Electrical Characteristics*. Figure 17 shows this effect using the INA271 (gain = 20).

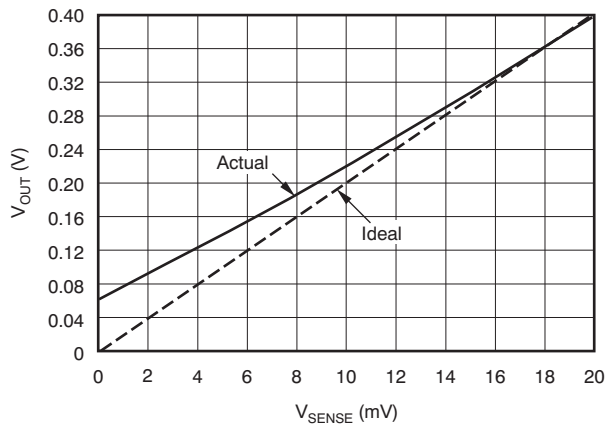
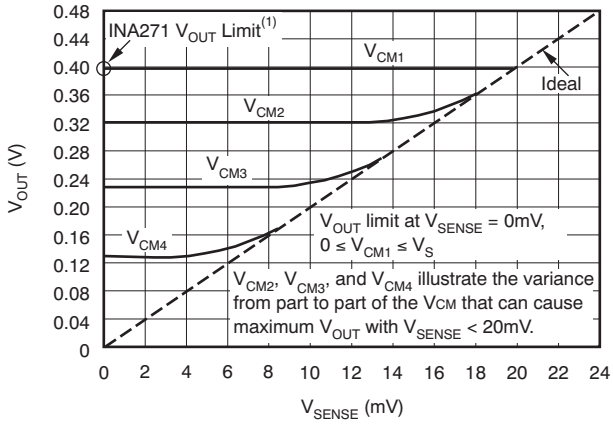


Figure 17. Example For Low V_{SENSE} Cases 1 and 3 (INA271, Gain = 20)

8.4.2.4 Low V_{SENSE} Case 2: V_{SENSE} < 20 mV, 0 V ≤ V_{CM} ≤ V_S

This region of operation is the least accurate for the INA270 family. To achieve the wide input common-mode voltage range, these devices use two op amp front ends in parallel. One op amp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is very low. Within this region, V_{OUT} approaches voltages close to linear operation levels for Normal Case 2.

This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0 V. Within this region, when V_{SENSE} approaches 20 mV, device operation is closer to that described by Normal Case 2. Figure 18 shows this behavior for the INA271. The V_{OUT} maximum peak for this case is determined by maintaining a constant V_S, setting V_{SENSE} = 0 mV, and sweeping V_{CM} from 0 V to V_S. The exact V_{CM} at which V_{OUT} peaks during this case varies from device to device. The maximum peak voltage for the INA270 is 0.28 V; for the INA271, the maximum peak voltage is 0.4 V.



NOTE: (1) INA271 V_{OUT} Limit = 0.4V. INA270 V_{OUT} Limit = 0.28V.

Figure 18. Example for Low V_{SENSE} Case 2 (INA271, Gain = 20)

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The INA270 and INA271 measures the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference terminal to adjust the functionality of the output signal offers multiple configurations discussed throughout this section. There is also a filtering feature to remove unwanted transients and smooth the output voltage.

9.2 Typical Application

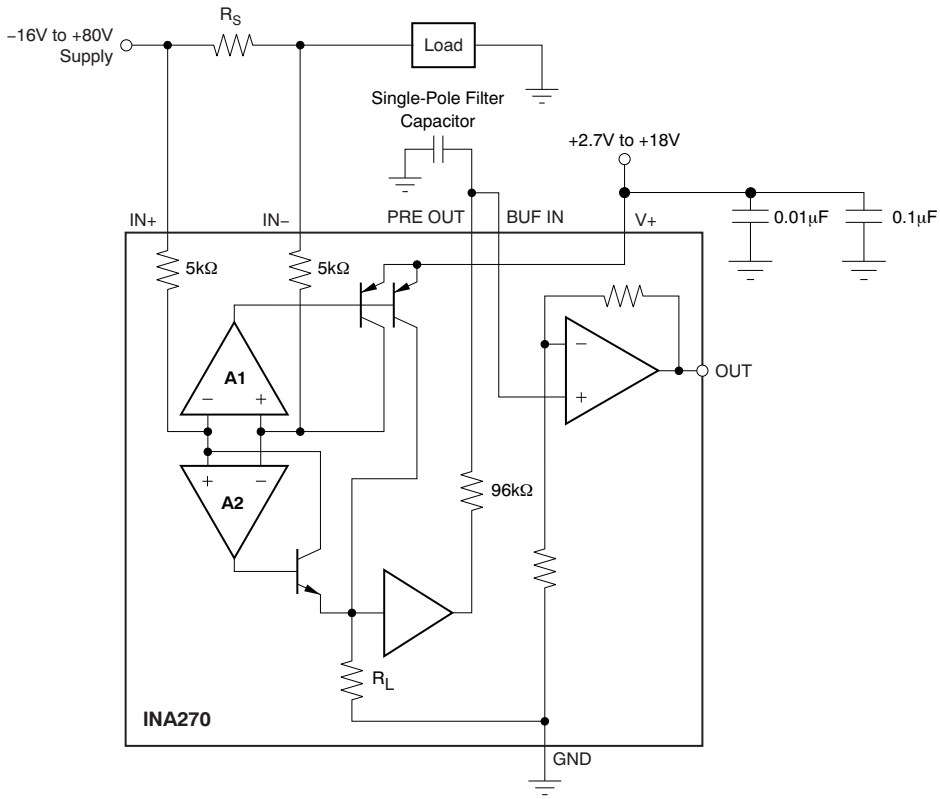

Figure 19. Filtering Configuration

9.2.1 Design Requirements

In this application, the device is configured to measure a triangular periodic current at 10 kHz with filtering. The average current through the shunt is the information that is desired. This current can be either solenoid current or inductor current where current is being pulsed through.

Selecting the capacitor size is based on the lowest frequency component to be filtered out. The amount of signal that is filtered out is dependant on this cutoff frequency. From the cutoff frequency, the attention is 20 dB per decade.

Typical Application (continued)

9.2.2 Detailed Design Procedure

Without this filtering capability, an input filter must be used. When series resistance is added to the input, large errors also come into play because the resistance must be large to create a low cutoff frequency. By using a 10-nF capacitor for the single-pole filter capacitor, the 10-kHz signal is averaged. The cutoff frequency made by the capacitor is set at 166 Hz frequency. This frequency is well below the periodic frequency and reduces the ripple on the output and the average current can easily be measured.

9.2.3 Application Curves

Figure 20 shows the output waveform without filtering. The output signal tracks the input signal with a large ripple. If this current is sampled by an ADC, many samples must be taken to average the current digitally. This process takes additional time to sample and average and is very time consuming, thus is unwanted for this application.

Figure 21 shows the output waveform with filtering. The output signal is filtered and the average can easily be measured with a small ripple. If this current is sampled by an ADC, only a few samples must be taken to average. Digital averaging is now not required and the time required is significantly reduced.

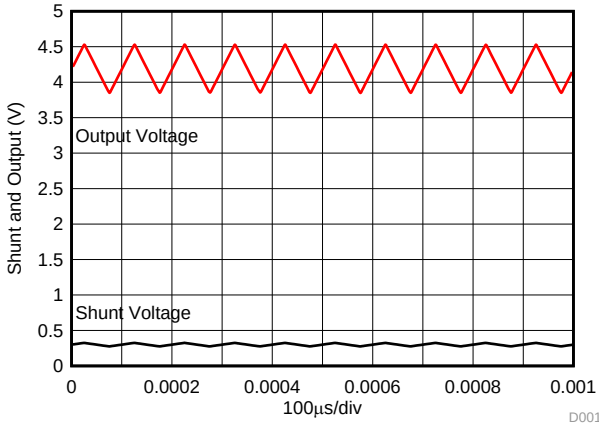

Figure 20. Without Filtering

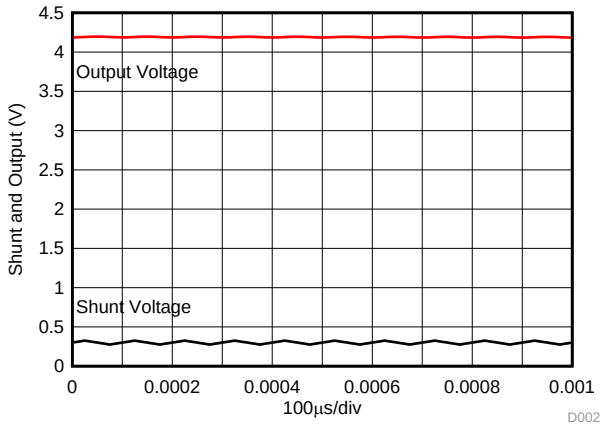

Figure 21. With Filtering

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10 Power Supply Recommendations

The input circuitry of the INA270 and INA271 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage is up to +80 V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

10.1 Shutdown

The INA270 and INA271 do not provide a shutdown pin; however, because these devices consume a quiescent current less than 1 mA, they can be powered by either the output of logic gates or by transistor switches to supply power. Driving the gate low shuts down the INA270 and INA271. Use a totem-pole output buffer or gate that can provide sufficient drive along with a 0.1-μF bypass capacitor, preferably ceramic with good high-frequency characteristics. This gate must have a supply voltage of 3 V or greater because the INA270 and INA271 require a minimum supply greater than 2.7 V. In addition to eliminating quiescent current, this gate also turns off the 10-μA bias current present at each of the inputs. Note that the IN+ and IN– inputs are able to withstand full common-mode voltage under all powered and under-powered conditions. An example shutdown circuit is shown in Figure 22.

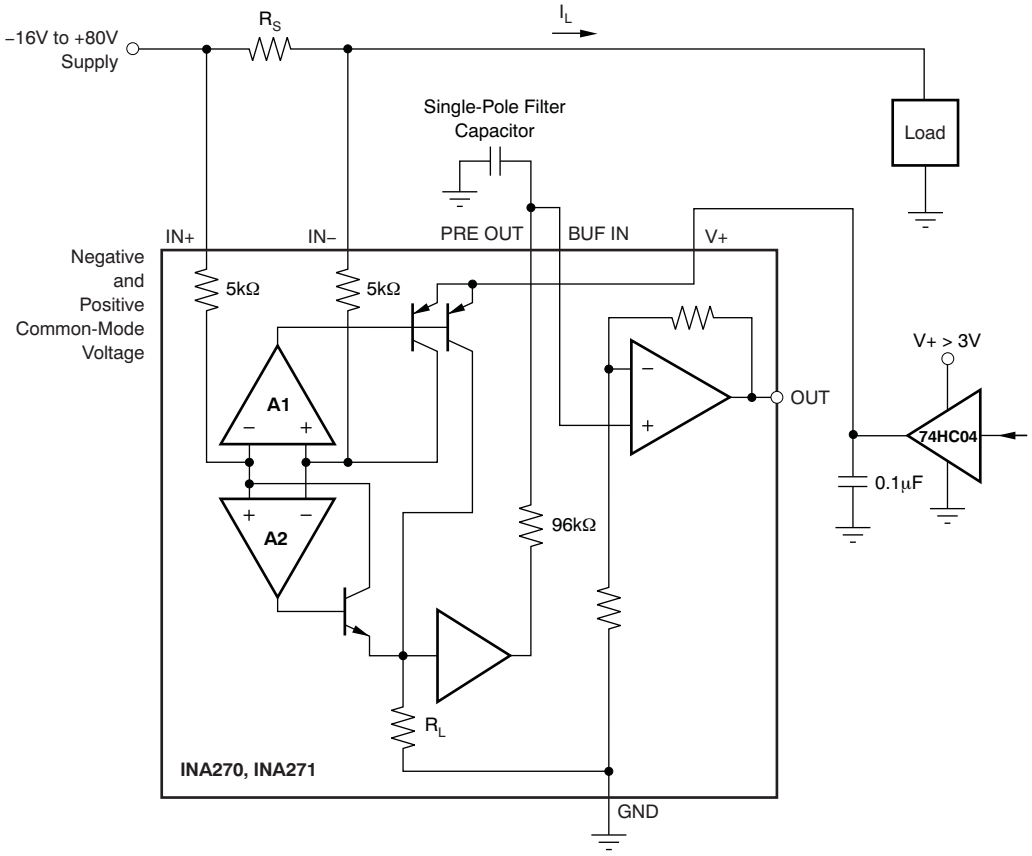

Figure 22. INA270–INA271 Example Shutdown Circuit

11 Layout

11.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

11.1.1 RFI and EMI

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Small ceramic capacitors placed directly across amplifier inputs can reduce RFI and EMI sensitivity. PCB layout must locate the amplifier as far away as possible from RFI sources. Sources can include other components in the same system as the amplifier itself, such as inductors (particularly switched inductors handling a lot of current and at high frequencies). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. If the amplifier cannot be located away from sources of radiation, shielding may be needed. Twisting wire input leads makes them more resistant to RF fields. The difference in input pin location of the INA270 and INA271 versus the INA193 to INA198 may provide different EMI performance.

11.2 Layout Example

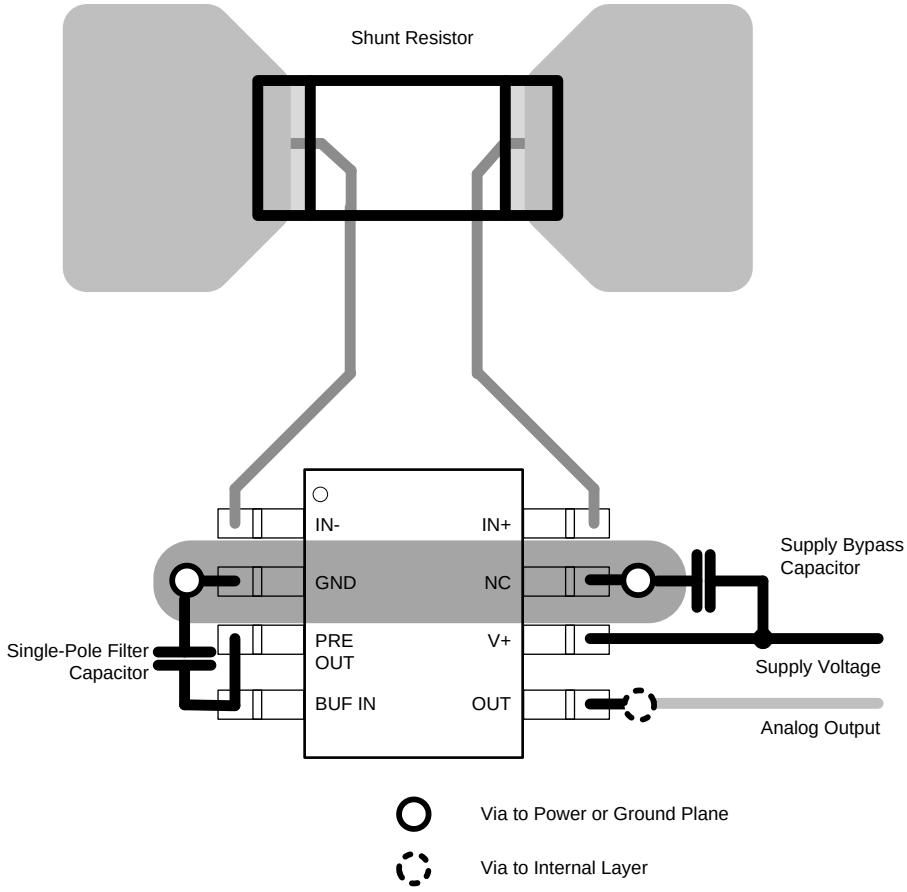

Figure 23. Example Layout

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

INA270 TINA-TI Spice Model, SBOM306

INA270 PSpice Model, SBOM485

INA270 TINA-TI Reference Design, SBOC246

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA270	Click here	Click here	Click here	Click here	Click here
INA271	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA270AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I270A	Samples
INA270AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I270A	Samples
INA271AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I271A	Samples
INA271AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I271A	Samples
INA271AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I271A	Samples
INA271AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I271A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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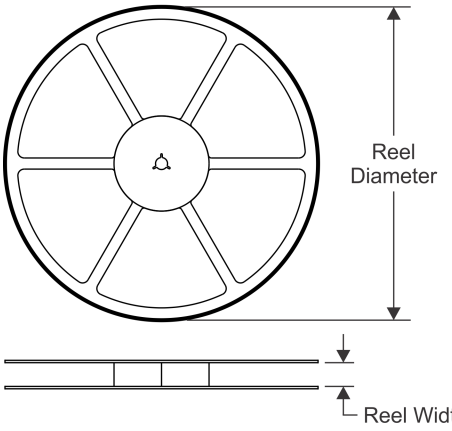
OTHER QUALIFIED VERSIONS OF INA271 :

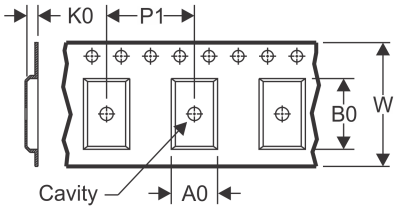
NOTE: Qualified Version Definitions:

TAPE AND REEL INFORMATION

REEL DIMENSIONS

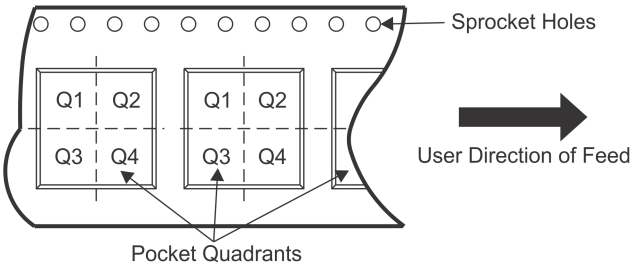


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

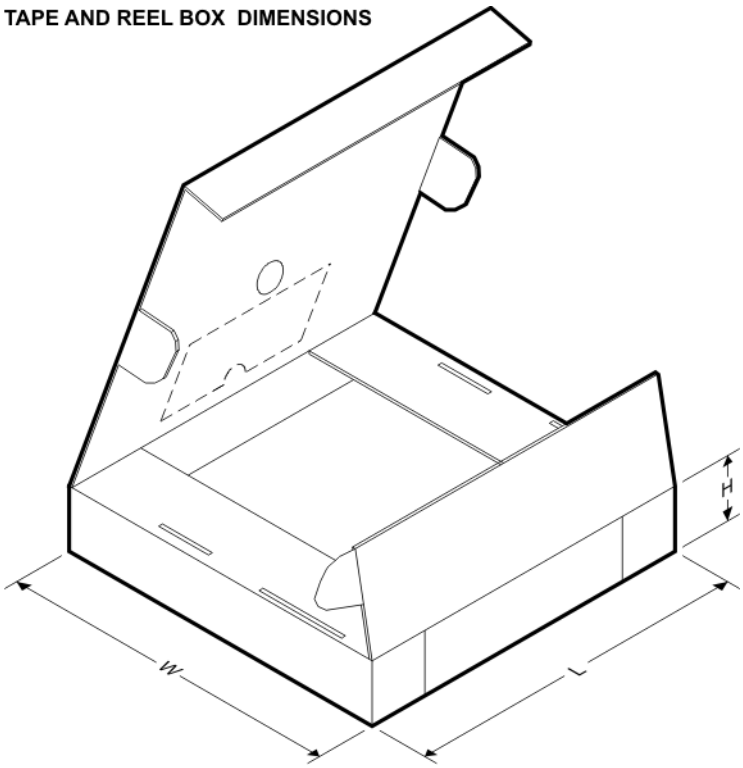
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA270AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA271AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

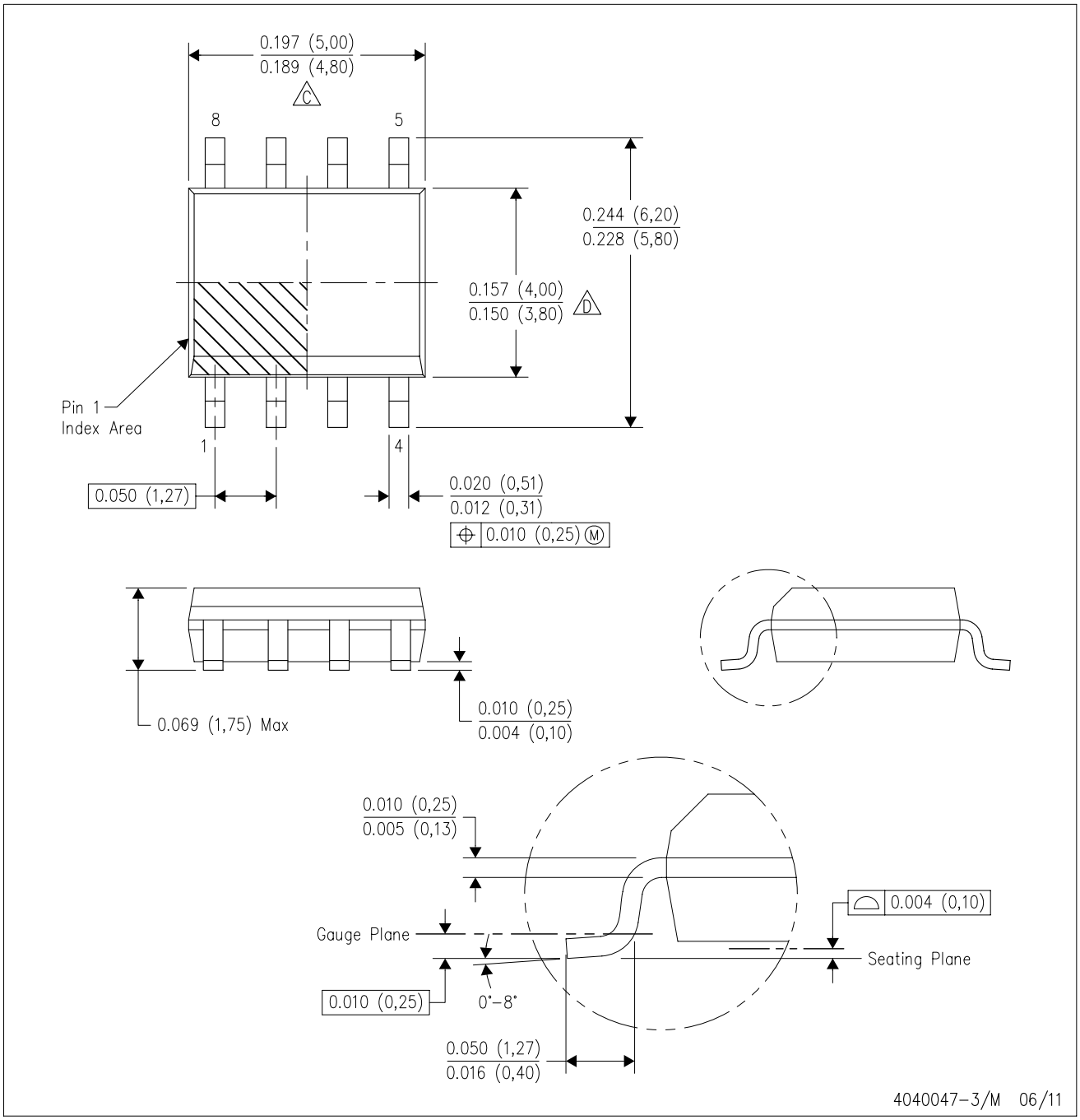
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

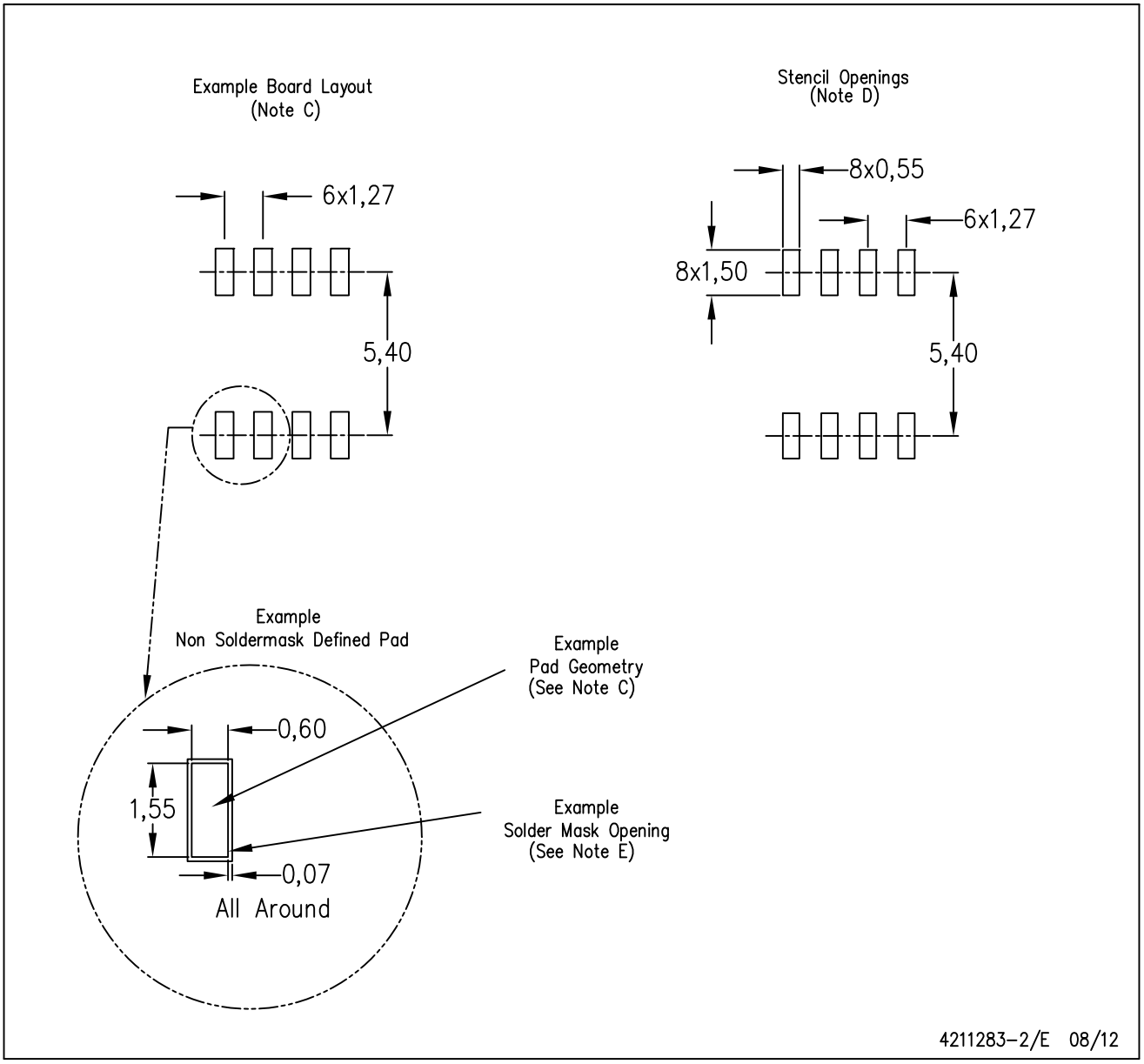
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA270AIDR	SOIC	D	8	2500	367.0	367.0	38.0
INA271AIDR	SOIC	D	8	2500	367.0	367.0	38.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

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