19-0464; Rev 5; 1/12

# +2.7V to +5.25V, Low-Power, 8-Channel, Serial 10-Bit ADCs



## General Description

The MAX148/MAX149 10-bit data-acquisition systems combine an 8-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and low power consumption. They operate from a single +2.7V to +5.25V supply, and sample to 133ksps. Both devices' analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface connects directly to SPI/QSPI™ and MICROWIRE™ devices without external logic. A serial-strobe output allows direct connection to TMS320-family digital signal processors. The MAX148/MAX149 use either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions.

The MAX149 has an internal 2.5V reference, while the MAX148 requires an external reference. Both parts have a reference-buffer amplifier with a ±1.5% voltage-adjustment range.

These devices provide a hard-wired $\overline{SHDN}$ pin and a software-selectable power-down, and can be programmed to automatically shut down at the end of a conversion. Accessing the serial interface automatically powers up the MAX148/MAX149, and the quick turn-on time allows them to be shut down between all conversions. This technique can cut supply current to under 60µA at reduced sampling rates.

The MAX148/MAX149 are available in 20-pin PDIP and 20-pin SSOP packages.

For 4-channel versions of these devices, see the MAX1248/MAX1249 data sheet.

## Applications

Portable Data Logging

Data Acquisition

Medical Instruments

Battery-Powered Instruments

Pen Digitizers

Process Control

***Pin Configuration appears at end of data sheet.***

## Features

- **8-Channel Single-Ended or 4-Channel Differential Inputs**
- **Single-Supply Operation: +2.7V to +5.25V**
- **Internal 2.5V Reference (MAX149)**
- **Low Power: 1.2mA (133ksps, 3V Supply)**
  **54µA (1ksps, 3V Supply)**
  **1µA (Power-Down Mode)**
- **SPI/QSPI/MICROWIRE/TMS320-Compatible 4-Wire Serial Interface**
- **Software-Configurable Unipolar or Bipolar Inputs**
- **20-Pin DIP/SSOP Packages**

## Ordering Information

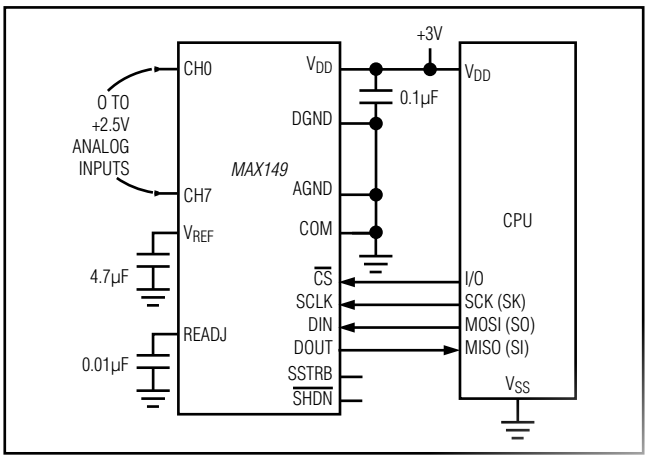
| PART† | TEMP RANGE | PIN-PACKAGE | INL (LSB) |
|---|---|---|---|
| **MAX148**ACPP+ | 0°C to +70°C | 20 PDIP | ±1/2 |
| MAX148BCPP+ | 0°C to +70°C | 20 PDIP | ±1 |
| MAX148ACAP+ | 0°C to +70°C | 20 SSOP | ±1/2 |
| MAX148BCAP+ | 0°C to +70°C | 20 SSOP | ±1 |

***Ordering Information continued at end of data sheet.***

*†Contact factory for availability of alternate surface-mount package.*

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

## Typical Operating Circuit




*QSPI is a trademark of Motorola, Inc. MICROWIRE is a trademark of National Semiconductor Corp.*

# +2.7V to +5.25V, Low-Power, 8-Channel, Serial 10-Bit ADCs

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to AGND, DGND.....-0.3V to +6V
AGND to DGND .....-0.3V to +0.3V
CH0–CH7, COM to AGND, DGND..... -0.3V to ($V_{DD}$ + 0.3V)
$V_{REF}$, REFADJ to AGND .....-0.3V to ($V_{DD}$ + 0.3V)
Digital Inputs to DGND .....-0.3V to +6V
Digital Outputs to DGND..... -0.3V to ($V_{DD}$ + 0.3V)
Digital Output Sink Current .....25mA
Continuous Power Dissipation ($T_A$ = +70°C)
PDIP (derate 11.11mW/°C above +70°C) .....889mW
SSOP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX148_C_P/MAX149_C_P ..... 0°C to +70°C
MAX148_E_P/MAX149_E_P .....-40°C to +85°C
MAX149BMAP.....-55°C to +125°C
Storage Temperature Range.....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = +2.7V to +5.25V; COM = 0; $f_{SCLK}$ = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX149—4.7µF capacitor at $V_{REF}$ pin; MAX148—external reference, $V_{REF}$ = 2.500V applied to $V_{REF}$ pin; $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC ACCURACY (Note 1)** | | | | | | |
| Resolution | | | 10 | | | Bits |
| Relative Accuracy (Note 2) | INL | MAX14_A | | | ±0.5 | LSB |
| | | MAX14_B | | | ±1.0 | |
| Differential Nonlinearity | DNL | No missing codes over temperature | | | ±1 | LSB |
| Offset Error | | MAX14_A | | ±0.15 | ±1 | LSB |
| | | MAX14_B | | ±0.15 | ±2 | |
| Gain Error (Note 3) | | MAX14_A | | | ±1 | LSB |
| | | MAX14_B | | | ±2 | |
| Gain Temperature Coefficient | | | | ±0.25 | | ppm/°C |
| Channel-to-Channel Offset Matching | | | | ±0.05 | | LSB |
| **DYNAMIC SPECIFICATIONS (10kHz Sine-Wave Input, 0 to 2.500$V_{P-P}$, 133ksps, 2.0MHz External Clock, Bipolar Input Mode)** | | | | | | |
| Signal-to-Noise + Distortion Noise | SINAD | | | 66 | | dB |
| Total Harmonic Distortion | THD | Up to the 5th harmonic | | -70 | | dB |
| Spurious-Free Dynamic Range | SFDR | | | 70 | | dB |
| Channel-to-Channel Crosstalk | | 65kHz, 2.500$V_{P-P}$ (Note 4) | | -75 | | dB |
| Small-Signal Bandwidth | | -3dB rolloff | | 2.25 | | MHz |
| Full-Power Bandwidth | | | | 1.0 | | MHz |
| **CONVERSION RATE** | | | | | | |
| Conversion Time (Note 5) | $t_{CONV}$ | Internal clock, $\overline{SHDN}$ = unconnected | 5.5 | | 7.5 | µs |
| | | Internal clock, $\overline{SHDN}$ = $V_{DD}$ | 35 | | 65 | |
| | | External clock = 2MHz, 12 clocks/ conversion | 6 | | | |
| Track/Hold Acquisition Time | $t_{ACQ}$ | | | | 1.5 | µs |
| Aperture Delay | | | | 30 | | ns |
| Aperture Jitter | | | | < 50 | | ps |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +2.7V to +5.25V; COM = 0; $f_{SCLK}$ = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX149—4.7µF capacitor at $V_{REF}$ pin; MAX148—external reference, $V_{REF}$ = 2.500V applied to $V_{REF}$ pin; $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **CONVERSION RATE (continued)** | | | | | | |
| Internal Clock Frequency | | $\overline{SHDN}$ = unconnected | | 1.8 | | MHz |
| | | $\overline{SHDN}$ = $V_{DD}$ | | 0.225 | | |
| External Clock Frequency | | | 0.1 | | 2.0 | MHz |
| | | Data transfer only | 1 | | 2.0 | |
| **ANALOG/COM INPUTS** | | | | | | |
| Input Voltage Range, Single-Ended and Differential (Note 6) | | Unipolar, COM = 0 | | | 0 to $V_{REF}$ | V |
| | | Bipolar, $V_{COM}$ = $V_{REF}$/2 | | | ±$V_{REF}$/2 | |
| Multiplexer Leakage Current | | On/off leakage current, $V_{CH_}$ = 0 or $V_{DD}$ | | ±0.01 | ±1 | µA |
| Input Capacitance | | | | 16 | | pF |
| **INTERNAL REFERENCE (MAX149 Only, Reference Buffer Enabled)** | | | | | | |
| $V_{REF}$ Output Voltage | | $T_A$ = +25°C (Note 7) | 2.470 | 2.500 | 2.530 | V |
| $V_{REF}$ Short-Circuit Current | | | | | 30 | mA |
| $V_{REF}$ Temperature Coefficient | | MAX149 | | ±30 | | ppm/°C |
| Load Regulation (Note 8) | | 0 to 0.2mA output load | | 0.35 | | mV |
| Capacitive Bypass at $V_{REF}$ | | Internal compensation mode | 0 | | | µF |
| | | External compensation mode | 4.7 | | | |
| Capacitive Bypass at REFADJ | | | 0.01 | | | µF |
| REFADJ Adjustment Range | | | | ±1.5 | | % |
| **EXTERNAL REFERENCE AT $V_{REF}$ (Buffer Disabled)** | | | | | | |
| $V_{REF}$ Input Voltage Range (Note 9) | | | 1.0 | | $V_{DD}$ + 50mV | V |
| $V_{REF}$ Input Current | | $V_{REF}$ = 2.500V | | 100 | 150 | µA |
| $V_{REF}$ Input Resistance | | | 18 | 25 | | kΩ |
| Shutdown $V_{REF}$ Input Current | | | | 0.01 | 10 | µA |
| REFADJ Buffer-Disable Threshold | | | $V_{DD}$ - 0.5 | | | V |
| **EXTERNAL REFERENCE AT REFADJ** | | | | | | |
| Capacitive Bypass at $V_{REF}$ | | Internal compensation mode | 0 | | | µF |
| | | External compensation mode | 4.7 | | | |
| Reference Buffer Gain | | MAX149 | | 2.06 | | V/V |
| | | MAX148 | | 2.00 | | |
| REFADJ Input Current | | MAX149 | | | ±50 | µA |
| | | MAX148 | | | ±10 | |

# +2.7V to +5.25V, Low-Power, 8-Channel, Serial 10-Bit ADCs

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +2.7V to +5.25V; COM = 0; $f_{SCLK}$ = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX149—4.7µF capacitor at $V_{REF}$ pin; MAX148—external reference, $V_{REF}$ = 2.500V applied to $V_{REF}$ pin; $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)** | | | | | | | |
| DIN, SCLK, $\overline{CS}$ Input High Voltage | $V_{IH}$ | $V_{DD} \le 3.6V$ | | 2.0 | | | V |
| | | $V_{DD} > 3.6V$ | | 3.0 | | | |
| DIN, SCLK, $\overline{CS}$ Input Low Voltage | $V_{IL}$ | | | | | 0.8 | V |
| DIN, SCLK, $\overline{CS}$ Input Hysteresis | $V_{HYST}$ | | | | 0.2 | | V |
| DIN, SCLK, $\overline{CS}$ Input Leakage | $I_{IN}$ | $V_{IN}$ = 0 or $V_{DD}$ | | | ±0.01 | ±1 | µA |
| DIN, SCLK, $\overline{CS}$ Input Capacitance | $C_{IN}$ | (Note 10) | | | | 15 | pF |
| $\overline{SHDN}$ Input High Voltage | $V_{SH}$ | | | $V_{DD}$ - 0.4 | | | V |
| $\overline{SHDN}$ Input Mid Voltage | $V_{SM}$ | | | 1.1 | | $V_{DD}$ - 1.1 | V |
| $\overline{SHDN}$ Input Low Voltage | $V_{SL}$ | | | | | 0.4 | V |
| $\overline{SHDN}$ Input Current | $I_S$ | $\overline{SHDN}$ = 0 or $V_{DD}$ | | | | ±4.0 | µA |
| $\overline{SHDN}$ Voltage, Unconnected | $V_{FLT}$ | $\overline{SHDN}$ = unconnected | | | $V_{DD}$/2 | | V |
| $\overline{SHDN}$ Maximum Allowed Leakage, Mid Input | | $\overline{SHDN}$ = unconnected | | | | ±100 | nA |
| **DIGITAL OUTPUTS (DOUT, SSTRB)** | | | | | | | |
| Output-Voltage Low | $V_{OL}$ | $I_{SINK}$ = 5mA | | | | 0.4 | V |
| | | $I_{SINK}$ = 16mA | | | | 0.8 | |
| Output-Voltage High | $V_{OH}$ | $I_{SOURCE}$ = 0.5mA | | $V_{DD}$ - 0.5 | | | V |
| Three-State Leakage Current | $I_L$ | $\overline{CS}$ = $V_{DD}$ | | | ±0.01 | ±10 | µA |
| Three-State Output Capacitance | $C_{OUT}$ | $\overline{CS}$ = $V_{DD}$ (Note 10) | | | | 15 | pF |
| **POWER REQUIREMENTS** | | | | | | | |
| Positive Supply Voltage | $V_{DD}$ | | | 2.70 | | 5.25 | V |
| Positive Supply Current | $I_{DD}$ | Operating mode, full-scale input (Note 11) | $V_{DD}$ = 5.25V | | 1.6 | 3.0 | mA |
| | | | $V_{DD}$ = 3.6V | | 1.2 | 2.0 | |
| | | Full power-down | $V_{DD}$ = 5.25V | | 3.5 | 15 | µA |
| | | | $V_{DD}$ = 3.6V | | 1.2 | 10 | |
| | | Fast power-down (MAX149) | | | 30 | 70 | |
| Supply Rejection (Note 12) | PSR | Full-scale input, external reference = 2.500V, $V_{DD}$ = 2.7V to 5.25V | | | ±0.3 | | mV |

## TIMING CHARACTERISTICS

($V_{DD}$ = +2.7V to +5.25V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Acquisition Time | $t_{ACQ}$ | | 1.5 | | | µs |
| DIN to SCLK Setup | $t_{DS}$ | | 100 | | | ns |
| DIN to SCLK Hold | $t_{DH}$ | | 0 | | | ns |
| SCLK Fall to Output Data Valid | $t_{DO}$ | Figure 1, MAX14_ _C/E | 20 | | 200 | ns |
| $\overline{CS}$ Fall to Output Enable | $t_{DV}$ | Figure 1 | | | 240 | ns |
| $\overline{CS}$ Rise to Output Disable | $t_{TR}$ | Figure 2 | | | 240 | ns |
| $\overline{CS}$ to SCLK Rise Setup | $t_{CSS}$ | | 100 | | | ns |
| $\overline{CS}$ to SCLK Rise Hold | $t_{CSH}$ | | 0 | | | ns |
| SCLK Pulse Width High | $t_{CH}$ | | 200 | | | ns |
| SCLK Pulse Width Low | $t_{CL}$ | | 200 | | | ns |
| SCLK Fall to SSTRB | $t_{SSTRB}$ | Figure 1 | | | 240 | ns |
| $\overline{CS}$ Fall to SSTRB Output Enable | $t_{SDV}$ | External clock mode only, Figure 1 | | | 240 | ns |
| $\overline{CS}$ Rise to SSTRB Output Disable | $t_{STR}$ | External clock mode only, Figure 2 | | | 240 | ns |
| SSTRB Rise to SCLK Rise | $t_{SCK}$ | Internal clock mode only (Note 7) | 0 | | | ns |

**Note 1:** Tested at $V_{DD}$ = 2.7V; COM = 0; unipolar single-ended input mode.

**Note 2:** Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.

**Note 3:** MAX149—internal reference, offset nulled; MAX148—external reference ($V_{REF}$ = +2.500V), offset nulled.

**Note 4:** Ground "on" channel; sine wave applied to all "off" channels.

**Note 5:** Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.

**Note 6:** The common-mode range for the analog inputs is from AGND to $V_{DD}$.

**Note 7:** Sample tested to 0.1% AQL.

**Note 8:** External load should not change during conversion for specified accuracy.

**Note 9:** ADC performance is limited by the converter's noise floor, typically 300µ$V_{P-P}$.

**Note 10:** Guaranteed by design. Not subject to production testing.

**Note 11:** The MAX148 typically draws 400µA less than the values shown.

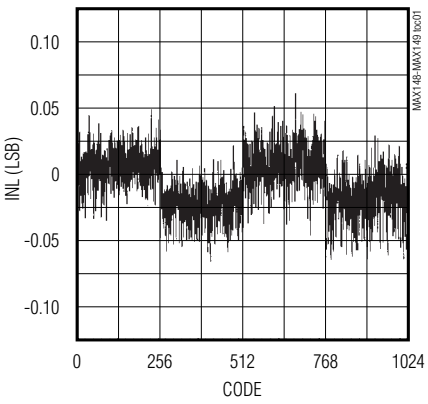
**Note 12:** Measured as $|V_{FS}(2.7V) - V_{FS}(5.25V)|$.

# +2.7V to +5.25V, Low-Power, 8-Channel, Serial 10-Bit ADCs

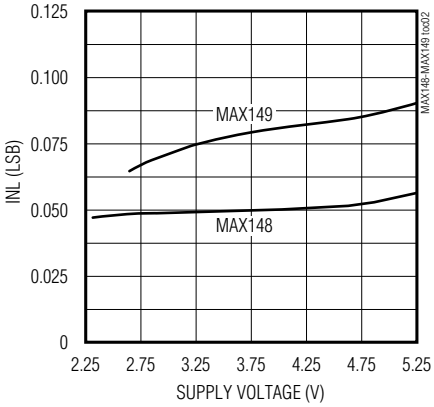
## Typical Operating Characteristics

($V_{DD}$ = 3.0V, VREF = 2.500V, $f_{SCLK}$ = 2.0MHz, $C_{LOAD}$ = 20pF, $T_A$ = +25°C, unless otherwise noted.)

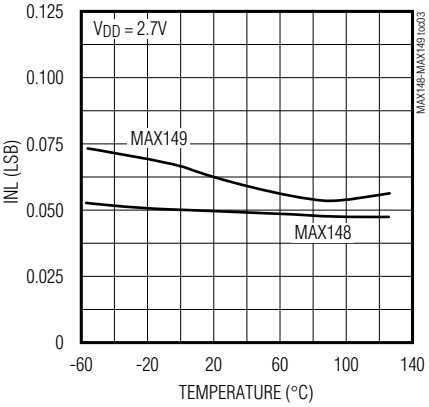
**INTEGRAL NONLINEARITY vs. CODE**



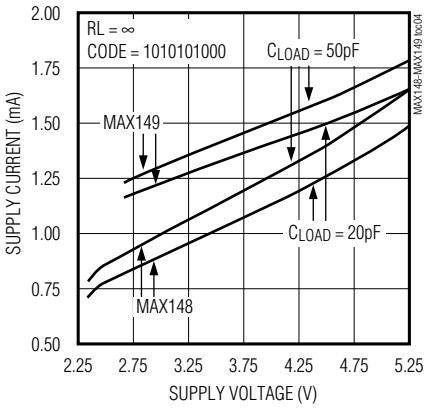

**INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE**



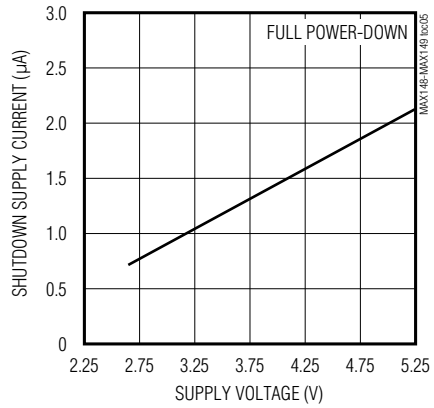

**INTEGRAL NONLINEARITY vs. TEMPERATURE**



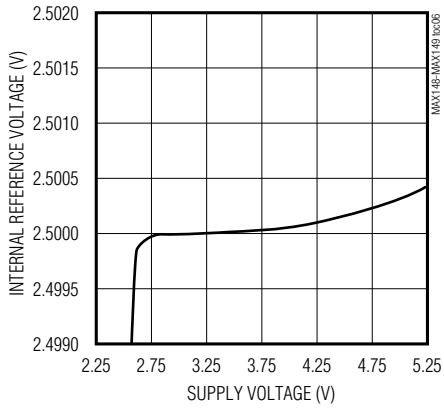

**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



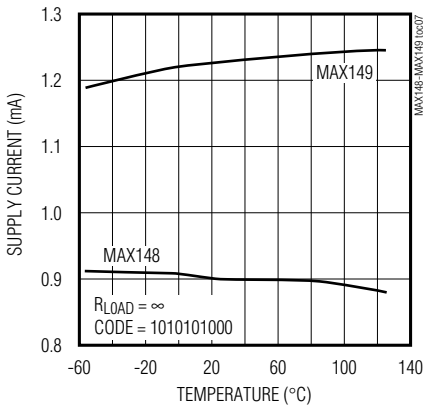

**SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE**



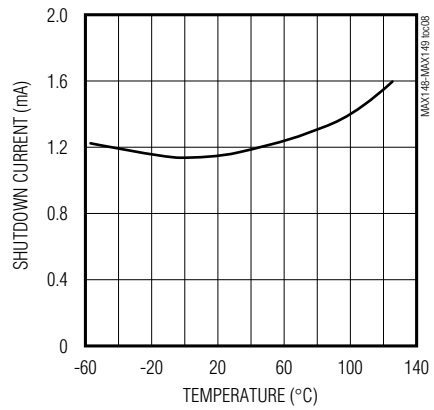

**MAX149 INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE**



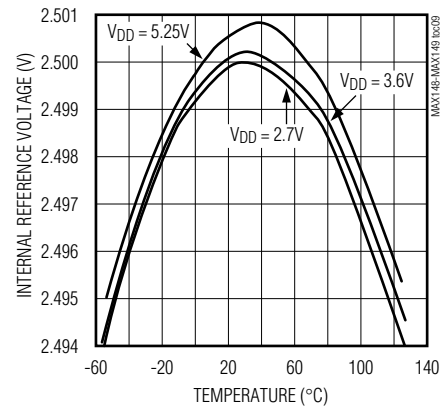

**SUPPLY CURRENT vs. TEMPERATURE**




**SHUTDOWN CURRENT vs. TEMPERATURE**




**MAX149 INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE**



## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1–8 | CH0–CH7 | Sampling Analog Inputs |
| 9 | COM | Ground Reference for Analog Inputs. COM sets zero-code voltage in single-ended mode. Must be stable to ±0.5 LSB. |
| 10 | $\overline{SHDN}$ | Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX148/MAX149 down; otherwise, they are fully operational. Pulling $\overline{SHDN}$ high puts the reference-buffer amplifier in internal compensation mode. Leaving $\overline{SHDN}$ unconnected puts the reference-buffer amplifier in external compensation mode. |
| 11 | $V_{REF}$ | Reference-Buffer Output/ADC Reference Input. Reference voltage for analog-to-digital conversion. In internal reference mode (MAX149 only), the reference buffer provides a 2.500V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to $V_{DD}$. |
| 12 | REFADJ | Input to the Reference-Buffer Amplifier. To disable the reference-buffer amplifier, tie REFADJ to $V_{DD}$. |
| 13 | AGND | Analog Ground |
| 14 | DGND | Digital Ground |
| 15 | DOUT | Serial-Data Output. Data is clocked out at SCLK's falling edge. High impedance when $\overline{CS}$ is high. |
| 16 | SSTRB | Serial-Strobe Output. In internal clock mode, SSTRB goes low when the MAX148/MAX149 begin the A/D conversion, and goes high when the conversion is finished. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode). |
| 17 | DIN | Serial-Data Input. Data is clocked in at SCLK's rising edge. |
| 18 | $\overline{CS}$ | Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance. |
| 19 | SCLK | Serial-Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed (duty cycle must be 40% to 60%). |
| 20 | $V_{DD}$ | Positive Supply Voltage |

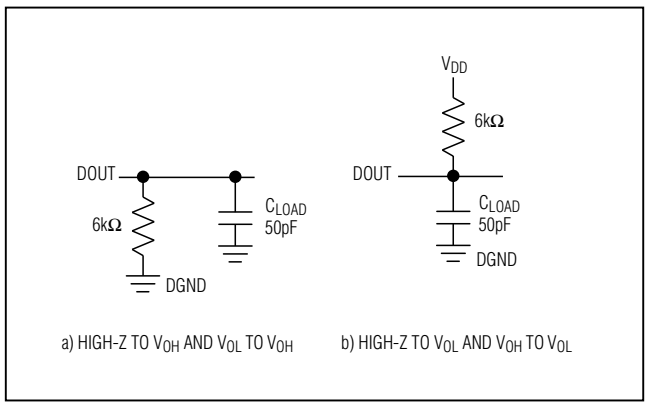



*Figure 1. Load Circuits for Enable Time*

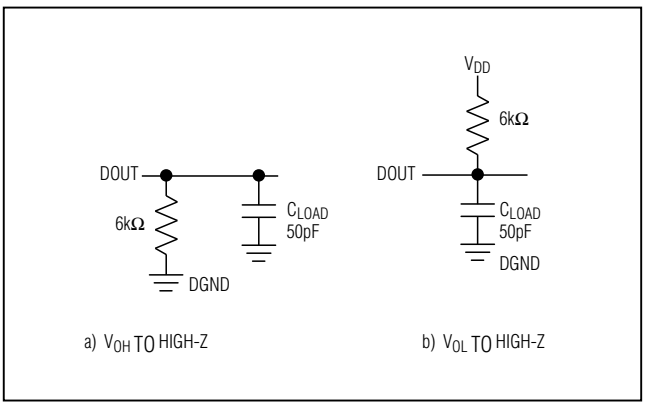



*Figure 2. Load Circuits for Disable Time*

# +2.7V to +5.25V, Low-Power, 8-Channel, Serial 10-Bit ADCs

## Detailed Description

The MAX148/MAX149 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 10-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). Figure 3 is a block diagram of the MAX148/MAX149.

### Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH7, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from the following pairs: CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the channels with Tables 2 and 3.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5 LSB (±0.1 LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor $C_{HOLD}$. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on $C_{HOLD}$ as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching $C_{HOLD}$ from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the comparator's input. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0 within the limits of 10-bit resolution. This action is equivalent to transferring a 16pF x [($V_{IN+}$) - ($V_{IN-}$)] charge from $C_{HOLD}$ to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

### Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of IIN+ - IN-I is sampled. At the end of the conversion, the positive input connects back to IN+, and $C_{HOLD}$ charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be

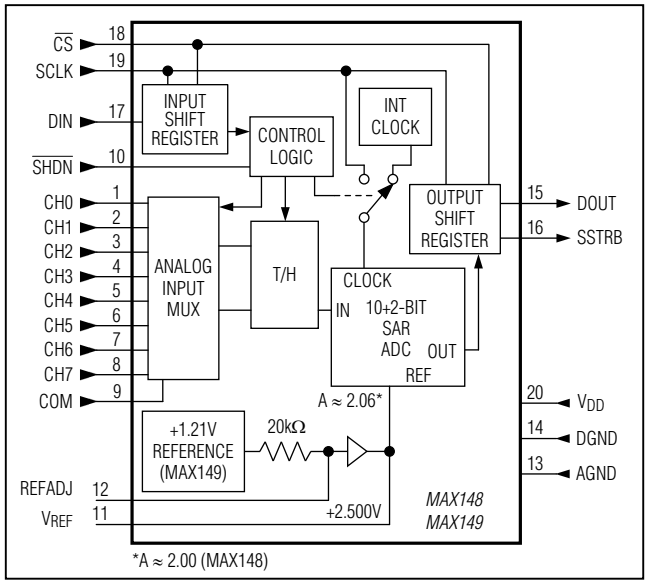



*Figure 3. Block Diagram*

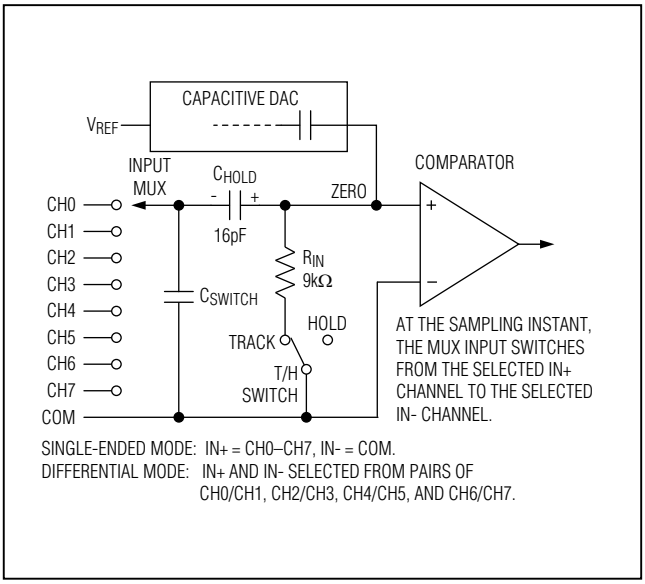



*Figure 4. Equivalent Input Circuit*

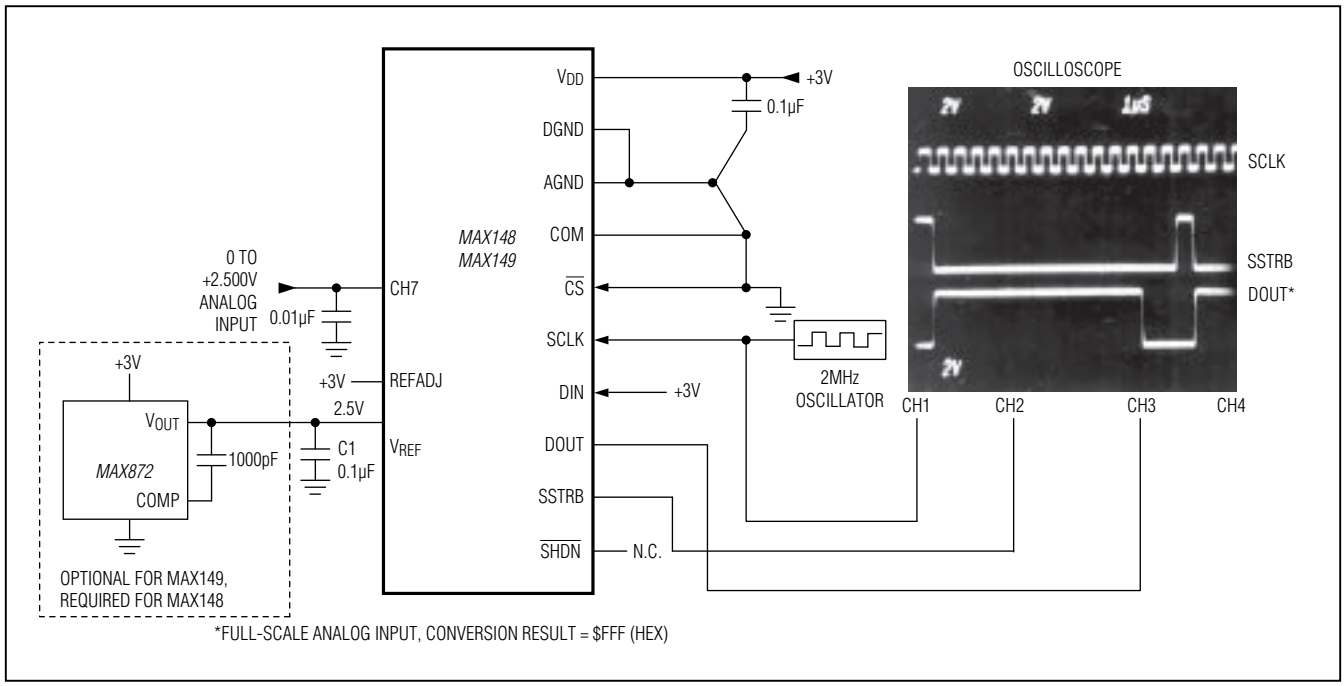



*Figure 5. Quick-Look Circuit*

allowed between conversions. The acquisition time, $t_{ACQ}$, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by the following equation:

$$t_{ACQ} = 7 \times (R_S + R_{IN}) \times 16pF$$

where $R_{IN}$ = 9kΩ, $R_S$ = the source impedance of the input signal, and $t_{ACQ}$ is never less than 1.5µs. Note that source impedances below 4kΩ do not significantly affect the ADC's AC performance.

Higher source impedances can be used if a 0.01µF capacitor is connected to the individual analog inputs. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

### Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

### Analog Input Protection

Internal protection diodes, which clamp the analog input to $V_{DD}$ and AGND, allow the channel input pins to swing from AGND - 0.3V to $V_{DD}$ + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed $V_{DD}$ by more than 50mV or be lower than AGND by 50mV.

**If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 2mA.**

### Quick Look

To quickly evaluate the MAX148/MAX149's analog performance, use the circuit of Figure 5. The MAX148/MAX149 require a control byte to be written to DIN before each conversion. Tying DIN to +3V feeds in control bytes of $FF (HEX), which trigger single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the conversion result is shifted out of DOUT. Varying the analog input to CH7 will alter the sequence of bits from DOUT. A total of 15 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

# +2.7V to +5.25V, Low-Power, 8-Channel, Serial 10-Bit ADCs

## Table 1. Control-Byte Format

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|
| START | SEL2 | SEL1 | SEL0 | UNI/$\overline{BIP}$ | SGL/$\overline{DIF}$ | PD1 | PD0 |

| BIT | NAME | DESCRIPTION | | |
|---|---|---|---|---|
| 7(MSB) | START | The first logic "1" bit after $\overline{CS}$ goes low defines the beginning of the control byte. | | |
| 6<br>5<br>4 | SEL2<br>SEL1<br>SEL0 | These three bits select which of the eight channels are used for the conversion (Tables 2 and 3) | | |
| 3 | UNI/$\overline{BIP}$ | 1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0 to $V_{REF}$ can be converted; in bipolar mode, the signal can range from $-V_{REF}/2$ to $+V_{REF}/2$. | | |
| 2 | SGL/$\overline{DIF}$ | 1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured (Tables 2 and 3). | | |
| 1 | PD1 | Selects clock and power-down modes. | | |
| 0(LSB) | PD0 | PD1 | PD0 | Mode |
| | | 0 | 0 | Full power-down |
| | | 0 | 1 | Fast power-down (MAX149 only) |
| | | 1 | 0 | Internal clock mode |
| | | 1 | 1 | External clock mode |

## Table 2. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

| SEL2 | SEL1 | SEL0 | CH0 | CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 | COM |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | + | | | | | | | | - |
| **1** | **0** | **0** | | + | | | | | | | - |
| **0** | **0** | **1** | | | + | | | | | | - |
| **1** | **0** | **1** | | | | + | | | | | - |
| **0** | **1** | **0** | | | | | + | | | | - |
| **1** | **1** | **0** | | | | | | + | | | - |
| **0** | **1** | **1** | | | | | | | + | | - |
| **1** | **1** | **1** | | | | | | | | + | - |

### *How to Start a Conversion*

Start a conversion by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX148/MAX149's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the control byte's MSB. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX148/MAX149 are compatible with SPI/QSPI and MICROWIRE devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. MICROWIRE, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit*, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the conversion result). See Figure 20 for MAX148/ MAX149 QSPI connections.

**Table 3. Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)**

| SEL2 | SEL1 | SEL0 | CH0 | CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | + | - | | | | | | |
| 0 | 0 | 1 | | | + | - | | | | |
| 0 | 1 | 0 | | | | | + | - | | |
| 0 | 1 | 1 | | | | | | | + | - |
| 1 | 0 | 0 | - | + | | | | | | |
| 1 | 0 | 1 | | | - | + | | | | |
| 1 | 1 | 0 | | | | | - | + | | |
| 1 | 1 | 1 | | | | | | | - | + |

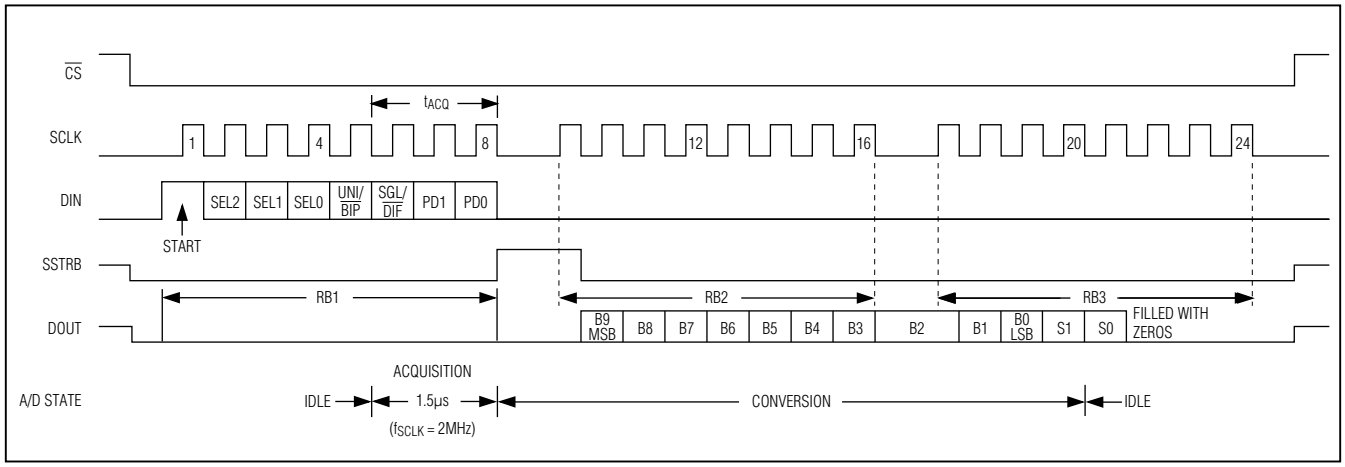



*Figure 6. 24-Clock External Clock Mode Conversion Timing (MICROWIRE and SPI-Compatible, QSPI-Compatible with $f_{SCLK} \leq 2MHz$)*

### *Simple Software Interface*

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion, padded with one leading zero, two sub-LSB bits, and three trailing zeros. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. To avoid excessive T/H droop, make sure the total conversion time does not exceed 120µs.

### *Digital Output*

In unipolar input mode, the output is straight binary (Figure 17). For bipolar input mode, the output is twos complement (Figure 18). Data is clocked out at the falling edge of SCLK in MSB-first format.

### *Clock Modes*

The MAX148/MAX149 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX148/MAX149.

# +2.7V to +5.25V, Low-Power, 8-Channel, Serial 10-Bit ADCs

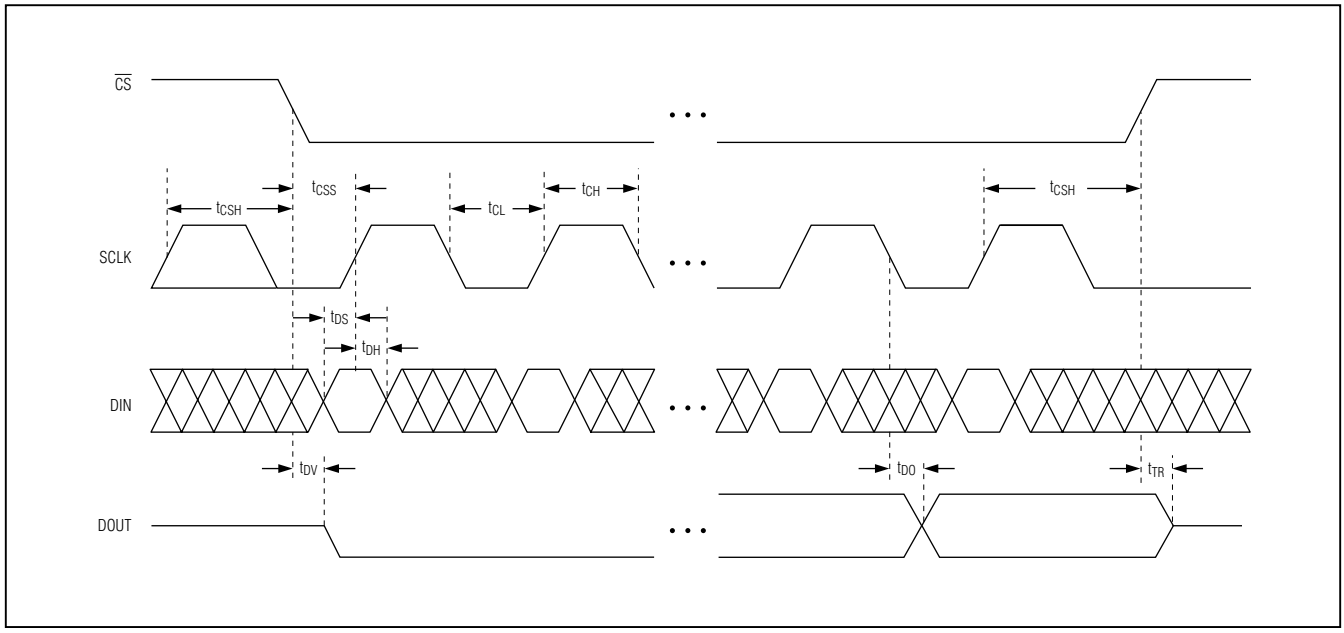



*Figure 7. Detailed Serial-Interface Timing*

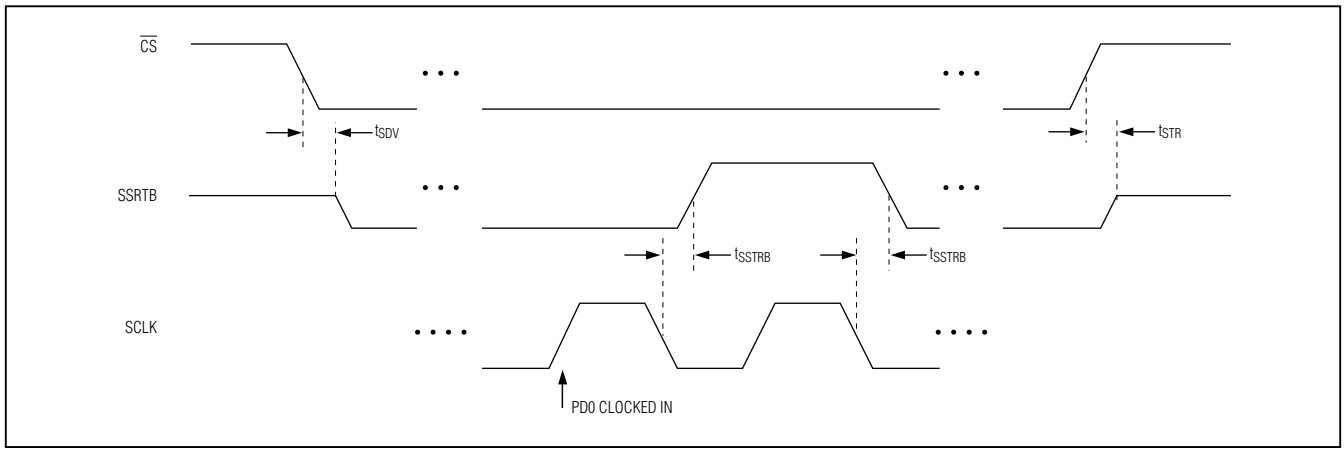



*Figure 8. External Clock Mode SSTRB Detailed Timing*

The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7–10 show the timing characteristics common to both modes.

### *External Clock*

In external clock mode, the external clock not only shifts data in and out, but it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive- approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB outputs a logic-low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial-clock frequency is less than 100kHz, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

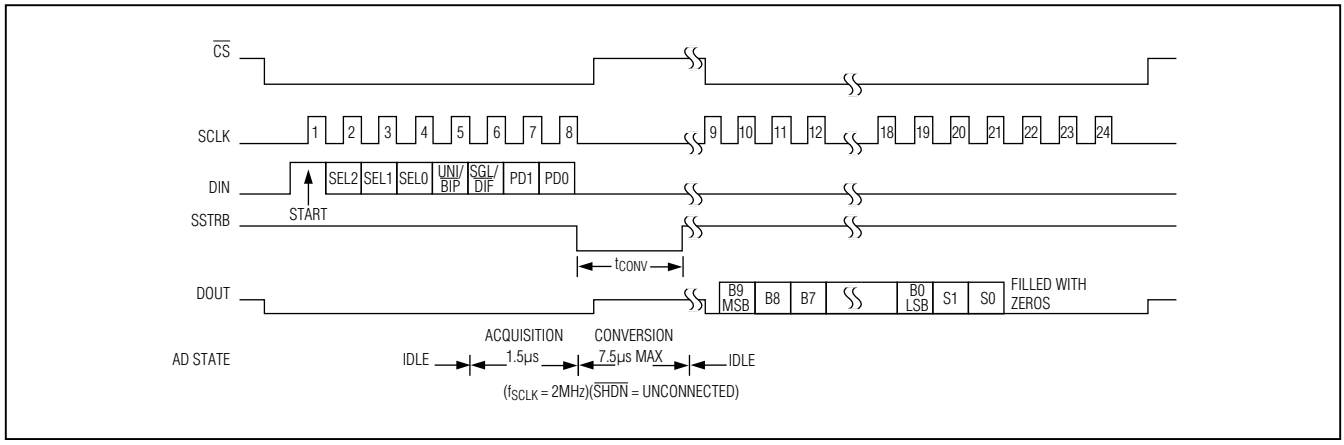



*Figure 9. Internal Clock Mode Timing*

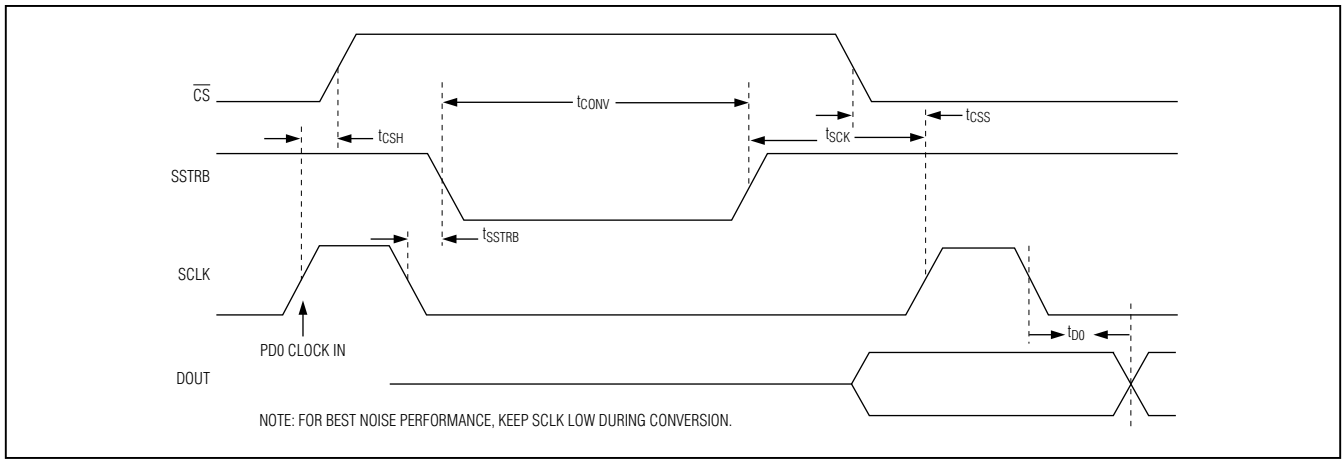



*Figure 10. Internal Clock Mode SSTRB Detailed Timing*

### *Internal Clock*

In internal clock mode, the MAX148/MAX149 generate their own conversion clocks internally. This frees the µP from the burden of running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate from 0 to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB is low for a maximum of 7.5µs ($\overline{SHDN}$ = unconnected), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 9). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX148/MAX149 and three-states DOUT, but it does not adversely affect an internal clock mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 10 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX148/MAX149 at clock rates exceeding 2.0MHz if the minimum acquisition time ($t_{ACQ}$) is kept above 1.5µs.

### *Data Framing*

The falling edge of $\overline{CS}$ does **not** start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on SCLK's falling edge, after the eighth bit of

**Table 4. Typical Power-Up Delay Times**

| REFERENCE BUFFER | REFERENCE-BUFFER COMPENSATION MODE | VREF CAPACITOR (µF) | POWER-DOWN MODE | POWER-UP DELAY (µs) | MAXIMUM SAMPLING RATE (ksps) |
|---|---|---|---|---|---|
| Enabled | Internal | — | Fast | 5 | 26 |
| Enabled | Internal | — | Full | 300 | 26 |
| Enabled | External | 4.7 | Fast | See Figure 14c | 133 |
| Enabled | External | 4.7 | Full | See Figure 14c | 133 |
| Disabled | — | — | Fast | 2 | 133 |
| Disabled | — | — | Full | 2 | 133 |

the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as follows:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle; e.g., after $V_{DD}$ is applied.

OR

The first high bit clocked into DIN after bit 3 of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

The fastest the MAX148/MAX149 can run with $\overline{CS}$ held low between conversions is 15 clocks per conversion. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is tied low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers (µCs) require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion is typically the fastest that a µC can drive the MAX148/MAX149. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

## Applications Information

### Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX148/MAX149 in internal clock mode, ready to convert with SSTRB = high. After the power supplies stabilize, the internal reset time is 10µs, and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros. Also see Table 4.

### Reference-Buffer Compensation

In addition to its shutdown function, $\overline{SHDN}$ selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. The 100kHz minimum clock rate is limited by droop on the sample-and-hold and is independent of the compensation used.

Unconnect $\overline{SHDN}$ to select external compensation. The *Typical Operating Circuit* uses a 4.7µF capacitor at $V_{REF}$. A 4.7µF value ensures reference-buffer stability and allows converter operation at the 2MHz full clock speed. External compensation increases power-up time (see the *Choosing Power-Down Mode* section and Table 4).

Pull $\overline{SHDN}$ high to select internal compensation. Internal compensation requires no external capacitor at $V_{REF}$ and allows for the shortest power-up times. The maximum clock rate is 2MHz in internal clock mode and 400kHz in external clock mode.

### Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down mode or fast power-down mode via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high or unconnected (Tables 1 and 5). In both software power-down modes, the serial interface remains operational, but the ADC does not convert. Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte.

Full power-down mode turns off all chip functions that draw quiescent current, reducing supply current to 2µA (typ). Fast power-down mode turns off all circuitry except the bandgap reference. With fast power-down mode, the supply current is 30µA. Power-up time can be shortened to 5µs in internal compensation mode.

Table 4 shows how the choice of reference-buffer compensation and power-down mode affects both power-up

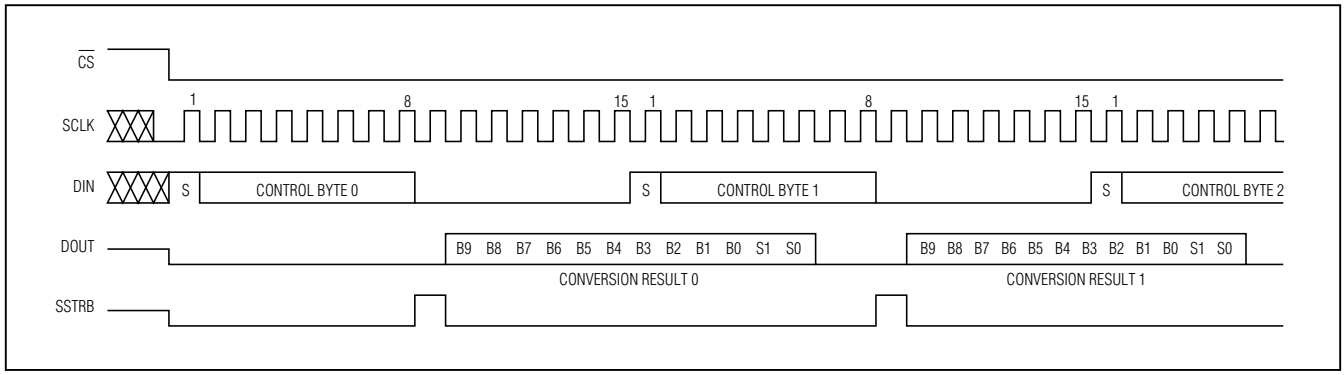



*Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing*

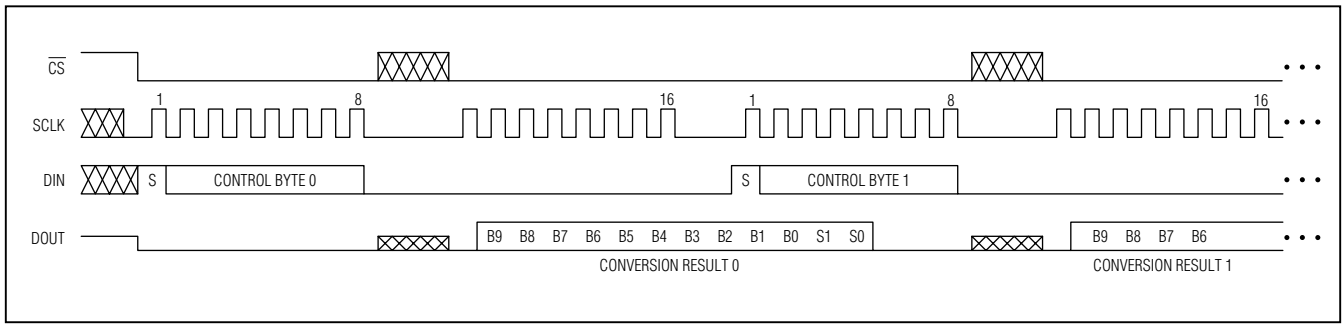



*Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing*

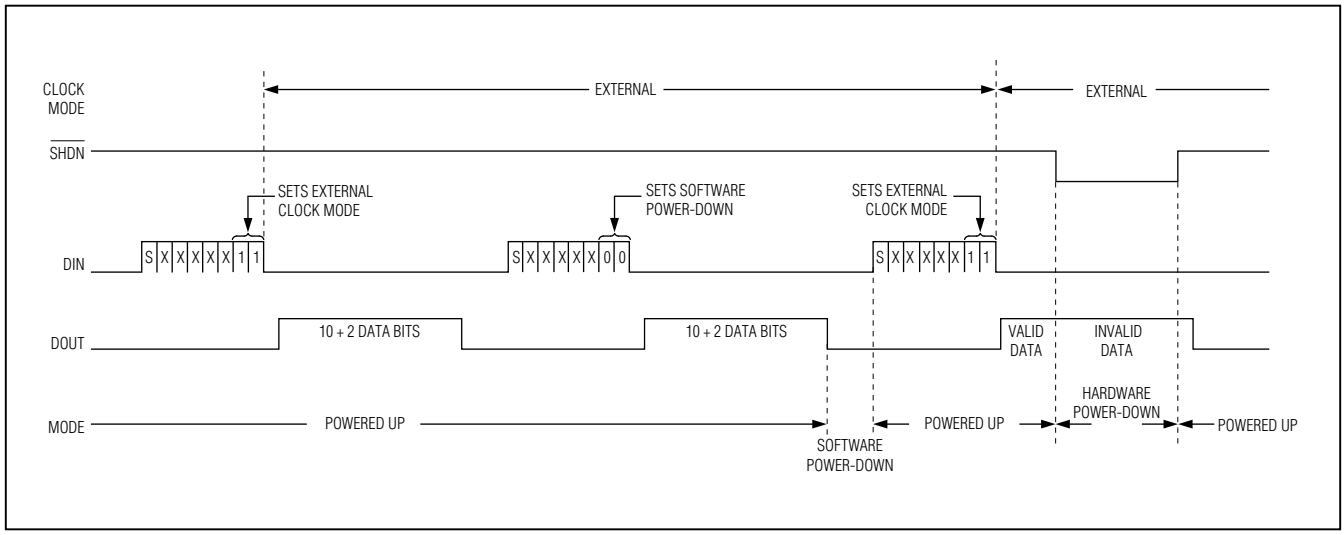



*Figure 12a. Timing Diagram Power-Down Modes, External Clock*

delay and maximum sample rate. In external compensation mode, power-up time is 20ms with a 4.7µF compensation capacitor when the capacitor is initially fully discharged. From fast power-down, startup time can be eliminated by using low-leakage capacitors that do not discharge more than ½ LSB while shut down. In power-down, leakage currents at $V_{REF}$ cause droop on the reference bypass capacitor. Figures 12a and 12b show the various power-down sequences in both external and internal clock modes.

# +2.7V to +5.25V, Low-Power, 8-Channel, Serial 10-Bit ADCs

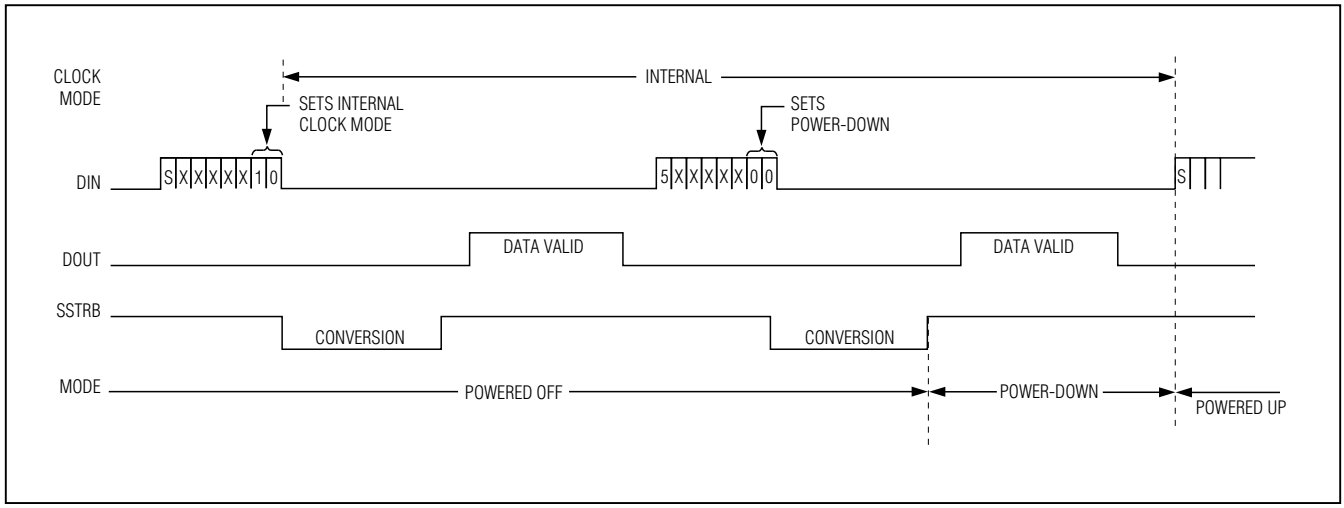



*Figure 12b. Timing Diagram Power-Down Modes, Internal Clock*

## Table 5. Software Power-Down and Clock Mode

| PD1 | PD0 | DEVICE MODE |
|---|---|---|
| 0 | 0 | Full Power-Down |
| 0 | 1 | Fast Power-Down |
| 1 | 0 | Internal Clock |
| 1 | 1 | External Clock |

## Table 6. Hard-Wired Power-Down and Internal Clock Frequency

| $\overline{SHDN}$ STATE | DEVICE MODE | REFERENCE BUFFER COMPENSATION | INTERNAL CLOCK FREQUENCY |
|---|---|---|---|
| 1 | Enabled | Internal | 225kHz |
| Unconnected | Enabled | External | 1.8MHz |
| 0 | Power-Down | — | — |

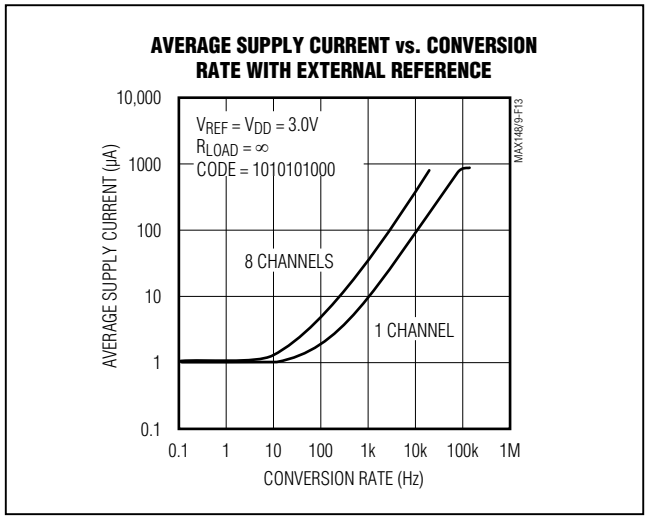



*Figure 13. Average Supply Current vs. Conversion Rate with External Reference*

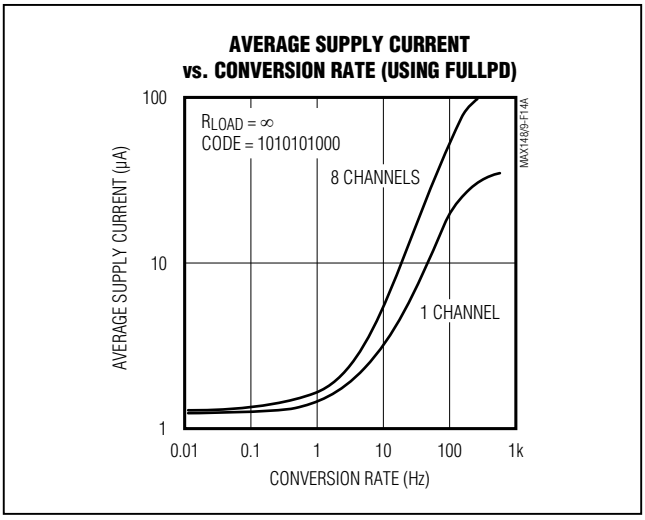



*Figure 14a. MAX149 Supply Current vs. Conversion Rate, FULLPD*

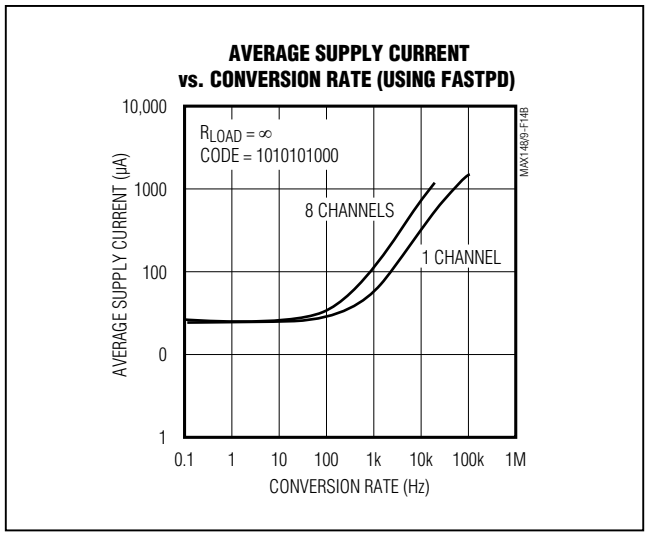



*Figure 14b. MAX149 Supply Current vs. Conversion Rate, FASTPD*

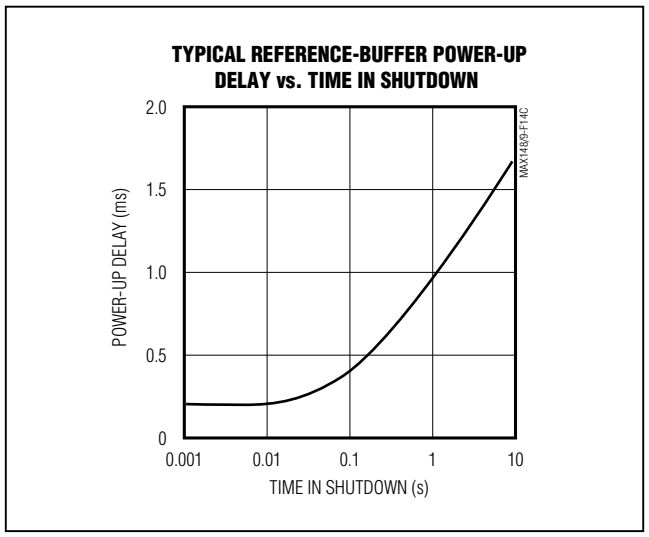



*Figure 14c. Typical Reference-Buffer Power-Up Delay vs. Time in Shutdown*

### Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 5, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC operates in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out after the MAX148/MAX149 enter a software power-down.

The first logical 1 on DIN is interpreted as a start bit and powers up the MAX148/MAX149. Following the start bit, the data input word or control byte also determines clock mode and power-down states. For example, if the DIN word contains PD1 = 1, then the chip remains powered up. If PD0 = PD1 = 0, a power-down resumes after one conversion.

### Hardware Power-Down

Pulling $\overline{SHDN}$ low places the converter in hardware power-down (Table 6). Unlike software power-down mode, the conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. $\overline{SHDN}$ also controls the clock frequency in internal clock mode. Leaving $\overline{SHDN}$ unconnected sets the internal clock frequency to 1.8MHz. When returning to normal operation with $\overline{SHDN}$ unconnected, there is a $t_{RC}$ delay of approximately 2MΩ x $C_L$, where $C_L$ is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high sets internal clock frequency to 225kHz. This feature eases the settling-time requirement for the reference voltage. With an external reference, the MAX148/MAX149 can be considered fully powered up within 2µs of actively pulling $\overline{SHDN}$ high.

### Power-Down Sequencing

The MAX148/MAX149 auto power-down modes can save considerable power when operating at less than maximum sample rates. Figures 13, 14a, and 14b show the average supply current as a function of the sampling rate. The following discussion illustrates the various power-down sequences.

### Lowest Power at Up to 500 Conversions/Channel/Second

The following examples show two different power-down sequences. Other combinations of clock rates, compensation modes, and power-down modes may give lowest power consumption in other applications.

Figure 14a depicts the MAX149 power consumption for one or eight channel conversions utilizing full power-down mode and internal-reference compensation. A 0.01µF bypass capacitor at REFADJ forms an RC filter with the internal 20kΩ reference resistor with a 0.2ms time constant. To achieve full 10-bit accuracy, 8 time constants or 1.6ms are required after power-up. Waiting this 1.6ms in FASTPD mode instead of in full power-up can reduce power consumption by a factor of 10 or more. This is achieved by using the sequence shown in Figure 15.

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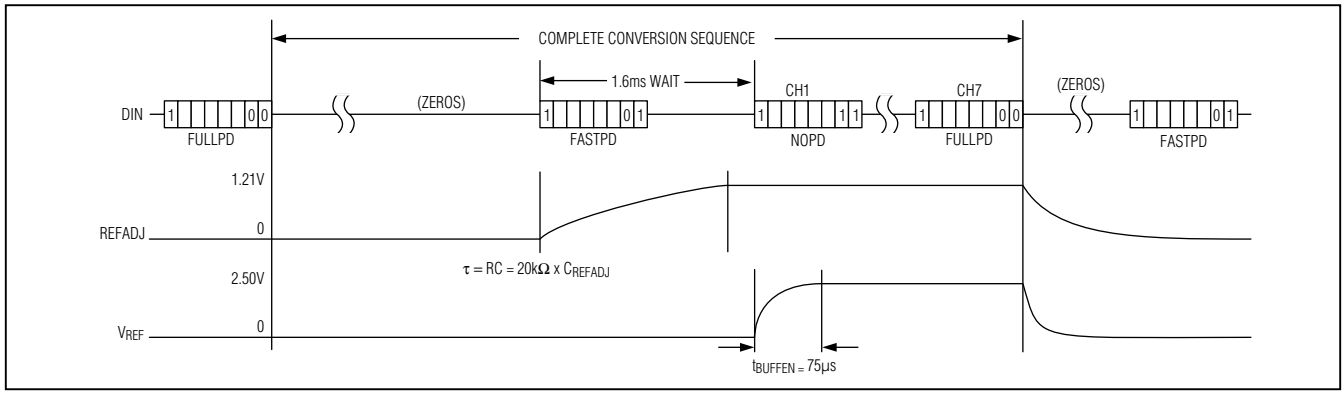



*Figure 15. MAX149 FULLPD/FASTPD Power-Up Sequence*

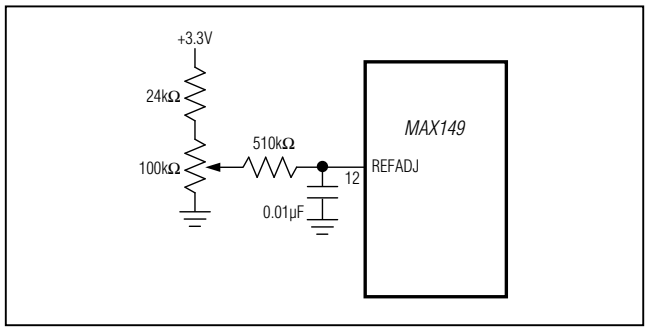



*Figure 16. MAX149 Reference-Adjust Circuit*

### *Lowest Power at Higher Throughputs*

Figure 14b shows the power consumption with external-reference compensation in fast power-down, with one and eight channels converted. The external 4.7µF compensation requires a 75µs wait after power-up with one dummy conversion. This graph shows fast multichannel conversion with the lowest power consumption possible. Full power-down mode may provide increased power savings in applications where the MAX148/MAX149 are inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

## *Internal and External References*

The MAX149 can be used with an internal or external reference voltage, whereas an external reference is required for the MAX148. An external reference can be connected directly at $V_{REF}$ or at the REFADJ pin.

An internal buffer is designed to provide 2.5V at $V_{REF}$ for both the MAX149 and the MAX148. The MAX149's internally trimmed 1.21V reference is buffered with a 2.06 gain. The MAX148's REFADJ pin is also buffered with a 2.00 gain to scale an external 1.25V reference at REFADJ to 2.5V at $V_{REF}$.

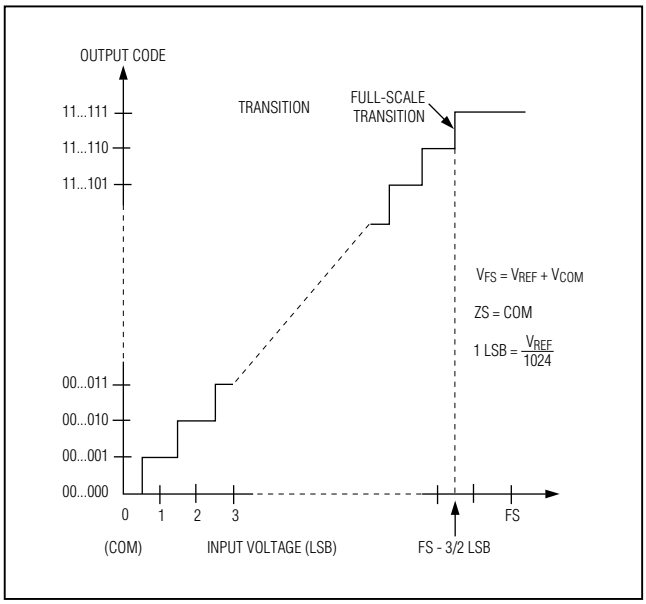



*Figure 17. Unipolar Transfer Function, Full Scale ($V_{FS}$) = $V_{REF}$ + $V_{COM}$, Zero Scale (ZS) = COM*

### *Internal Reference (MAX149)*

The MAX149's full-scale range with the internal reference is 2.5V with unipolar inputs and ±1.25V with bipolar inputs. The internal reference voltage is adjustable to ±1.5% with the circuit in Figure 16.

### *External Reference*

With both the MAX149 and MAX148, an external reference can be placed at either the input (REFADJ) or the output ($V_{REF}$) of the internal reference-buffer amplifier. The REFADJ input impedance is typically 20kΩ for the MAX149, and higher than 100kΩ for the MAX148. At $V_{REF}$, the DC input resistance is a minimum of 18kΩ. During conversion, an external reference at $V_{REF}$ must

## Table 7. Full Scale and Zero Scale

| UNIPOLAR MODE | | BIPOLAR MODE | | |
|---|---|---|---|---|
| Full Scale | Zero Scale | Positive Full Scale | Zero Scale | Negative Full Scale |
| $V_{REF} + V_{COM}$ | $V_{COM}$ | $V_{REF}/2 + V_{COM}$ | $V_{COM}$ | $- V_{REF}/2 + V_{COM}$ |

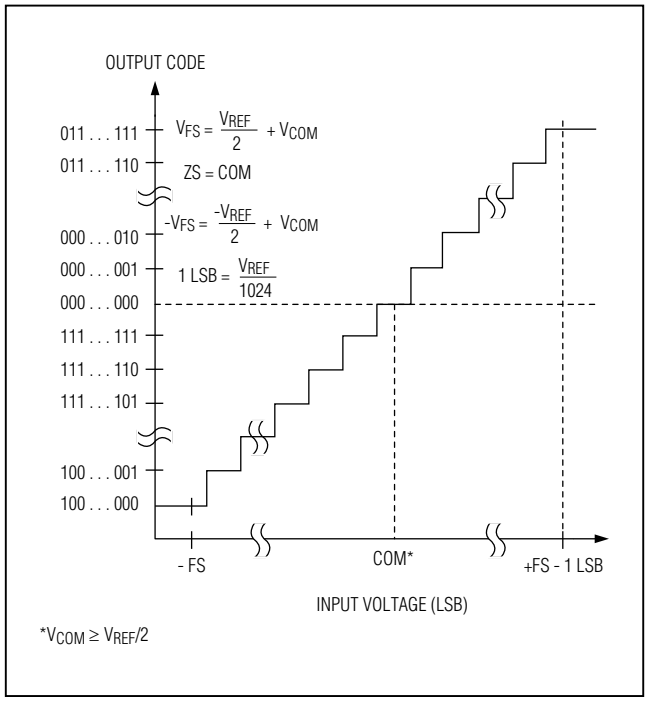



*Figure 18. Bipolar Transfer Function, Full Scale ($V_{FS}$) = $V_{REF}/2$ + $V_{COM}$, Zero Scale (ZS) = COM*

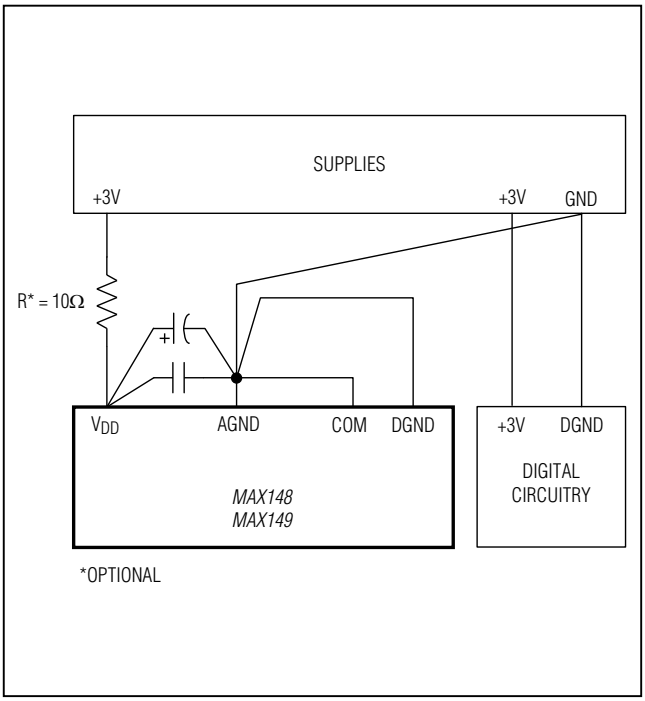



*Figure 19. Power-Supply Grounding Connection*

deliver up to 350µA DC load current and have 10Ω or less output impedance. If the reference has a higher output impedance or is noisy, bypass it close to the $V_{REF}$ pin with a 4.7µF capacitor.

Using the REFADJ input makes buffering the external reference unnecessary. To use the direct $V_{REF}$ input, disable the internal buffer by tying REFADJ to $V_{DD}$. In power-down, the input bias current to REFADJ is typically 25µA (MAX149) with REFADJ tied to $V_{DD}$. Pull REFADJ to AGND to minimize the input bias current in power-down.

### Transfer Function

Table 7 shows the full-scale voltage ranges for unipolar and bipolar modes.

The external reference must have a temperature coefficient of 20ppm/°C or less to achieve accuracy to within 1 LSB over the 0°C to +70°C commercial temperature range.

Figure 17 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 18 shows the bipolar input/output transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1 LSB = 2.44mV (2.500V/1024) for unipolar operation, and 1 LSB = 2.44mV [(2.500V/2 - -2.500V/2)/1024] for bipolar operation.

# +2.7V to +5.25V, Low-Power, 8-Channel, Serial 10-Bit ADCs

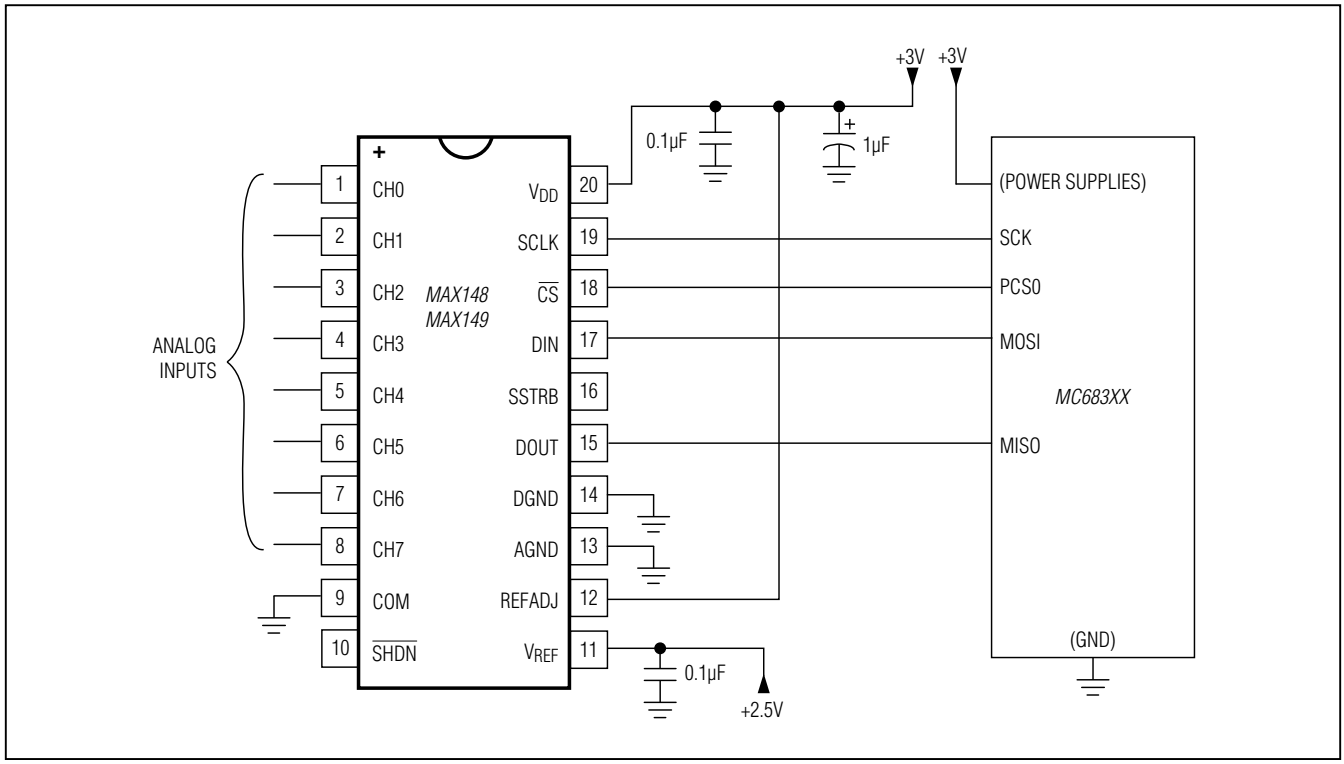



*Figure 20. MAX148/MAX149 QSPI Connections, External Reference*

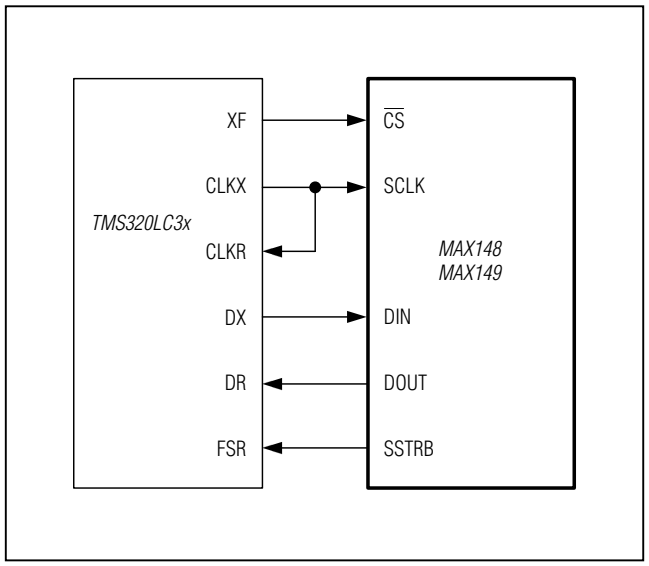



*Figure 21. MAX148/MAX149-to-TMS320 Serial Interface*

### Layout, Grounding, and Bypassing

For best performance, use PCBs. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 19 shows the recommended system ground connections. Establish a single-point analog ground (star ground point) at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. For lowest-noise operation, the ground return to the star ground's power supply should be low impedance and as short as possible.

High-frequency noise in the $V_{DD}$ power supply may affect the high-speed comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 1µF capacitors close to pin 20 of the MAX148/MAX149. Minimize capacitor lead lengths for best supply-noise rejection. If the power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter (Figure 19).

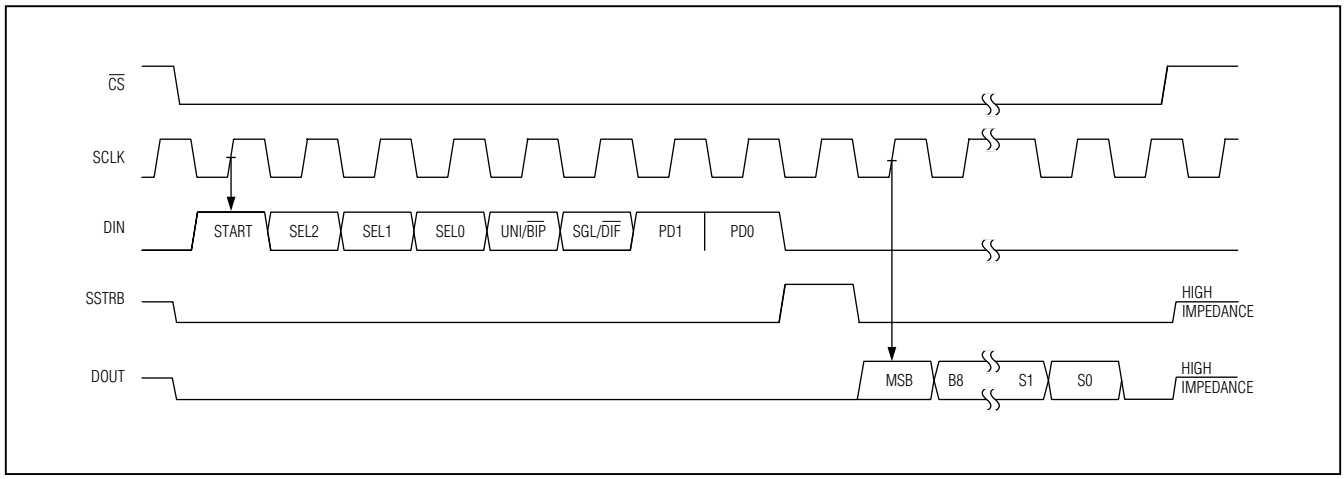



*Figure 22. TMS320 Serial-Interface Timing Diagram*

### *High-Speed Digital Interfacing with QSPI*

The MAX148/MAX149 can interface with QSPI using the circuit in Figure 20 ($f_{SCLK}$ = 2.0MHz, CPOL = 0, CPHA = 0). This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU, since QSPI incorporates its own microsequencer.

The MAX148/MAX149 are QSPI compatible up to the maximum external clock frequency of 2MHz.

### *TMS320LC3x Interface*

Figure 21 shows an application circuit to interface the MAX148/MAX149 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 22.

Use the following steps to initiate a conversion in the MAX148/MAX149 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are tied together with the MAX148/MAX149's SCLK input.
2) The MAX148/MAX149's $\overline{CS}$ pin is driven low by the TMS320's XF_ I/O port to enable data to be clocked into the MAX148/MAX149's DIN.
3) An 8-bit word (1XXXXX11) should be written to the MAX148/MAX149 to initiate a conversion and place the device into external clock mode. See Table 1 to select the proper XXXXX bit values for your specific application.
4) The MAX148/MAX149's SSTRB output is monitored through the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX148/MAX149.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 10 + 2-bit conversion result followed by 4 trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX148/MAX149 until the next conversion is initiated.

# +2.7V to +5.25V, Low-Power, 8-Channel, Serial 10-Bit ADCs

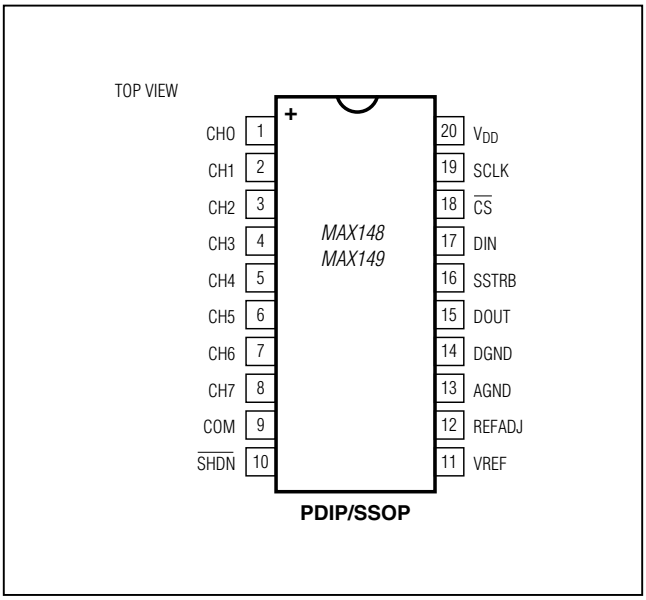
## Ordering Information (continued)

| PART† | TEMP RANGE | PIN-PACKAGE | INL (LSB) |
|---|---|---|---|
| MAX148AEPP+ | -40°C to +85°C | 20 PDIP | ±1/2 |
| MAX148BEPP+ | -40°C to +85°C | 20 PDIP | ±1 |
| MAX148AEAP+ | -40°C to +85°C | 20 SSOP | ±1/2 |
| MAX148BEAP+ | -40°C to +85°C | 20 SSOP | ±1 |
| **MAX149**ACPP+ | 0°C to +70°C | 20 PDIP | ±1/2 |
| MAX149BCPP+ | 0°C to +70°C | 20 PDIP | ±1 |
| MAX149ACAP+ | 0°C to +70°C | 20 SSOP | ±1/2 |
| MAX149BCAP+ | 0°C to +70°C | 20 PDIP | ±1 |
| MAX149AEPP+ | -40°C to +85°C | 20 PDIP | ±1/2 |
| MAX149BEPP+ | -40°C to +85°C | 20 PDIP | ±1 |
| MAX149AEAP+ | -40°C to +85°C | 20 SSOP | ±1/2 |
| MAX149BEAP+ | -40°C to +85°C | 20 SSOP | ±1 |
| MAX149BMAP/PR+ | -55°C to +125°C | 20 SSOP | ±1 |
| MAX149BMAP/PR2+ | -55°C to +125°C | 20 SSOP | ±1 |
| MAX149BMAP/PR3+ | -55°C to +125°C | 20 SSOP | ±1 |

†*Contact factory for availability of alternate surface-mount package.*

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

## Pin Configuration




## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. | LAND PATTERN NO. |
|---|---|---|---|
| 20 PDIP | P20+4 | 21-0043 | — |
| 20 SSOP | A20+1 | 21-0056 | 90-0094 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 3 | 5/09 | Revised *Ordering Information*, *Electrical Characteristics* table, *Pin Description*, Figure 9, added ruggedized plastic information. | 1–4, 7, 13, 14, 16, 17, 22–23 |
| 4 | 1/10 | Revised *Ordering Information*. | 22 |
| 5 | 1/12 | Removed military options. | 1, 2, 22 |

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