High Reliability Serial EEPROMs

WL-CSP EEPROM family
SPI BUS

BU9829GUL-W

No.10001EAT13

●Description

BU9829GUL-W is Serial EEPROM built-in LDO regulator by SPI BUS interface.

●Features

○EEPROM PART

1) 2,048 words × 8 bits architecture serial EEPROM
2) Wide operating voltage range (1.6V～3.6V)
3) Serial Peripheral Interface
4) Self-timed write cycle with automatic erase
5) Low Power consumption Write (3.6V) : 1.5mA (Typ.)
   Read (3.6V) : 0.5mA (Typ.)
   Standby (3.6V) : 0.1μA (Typ.)
6) Auto-increment of registers address for Read mode
7) 32 byte Page Write mode
8) DATA security
   Defaults to power up with write-disabled state
   Software instructions for write-enable/disable
   Block writes protection by status register
   Write inhibit at low Vcc
9) Initial data FFh in all address, 00h in status register and 10 in VSET[1:0].
10) Data retention: 10 years
11) Endurance : 100,000 erase/write cycles

○LDO REGULATOR PART

12) Low power consumption
    Standby (3.6V) : 0.1 μA (Typ.)
    Operation (3.6V) : 0.1mA (Typ.)
13) Power on/off by enable pin
14) Initial LDO output voltage 2.9V
15) Setting output voltage by EEPROM command (VSET WRITE)

●Absolute maximum rating (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc1(EEPROM)	-0.3～4.5	V
	Vcc2(LDO)		
Power Dissipation	Pd	220	mW
Storage Temperature	Tstg	-65 ～ 125	℃
Operating Temperature	Topr	-30 ～ 85	℃
Terminal Voltage	—	-0.3～Vcc＋0.3	V

●EEPROM recommended operating condition

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc1	1.6～3.6	V
Input Voltage	VIN	0～Vcc1	

●LDO regulator recommended operating condition

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc2	2.9～3.6	V
Input Voltage	VIN	0～Vcc2	

●**Memory cell characteristics** (Ta=25℃, Vcc1=1.6～3.6V)

Parameter	Limits			Unit
	Min.	Typ.	Max.	
Write/Erase Cycle *1	100,000	—	—	Cycle
Data Retention *1	10	—	—	Year

*1 : Not 100% tested

●**Input/output capacity** (Ta=25℃, Frequency=5MHz)

Parameter	Symbol	Conditions	Limits		Unit
			Min.	Max.	
Input Capacitance *1	C_{IN}	V_{IN}=GND	—	8	pF
Output Capacitance *1	C_{OUT}	V_{OUT}=GND	—	8	pF

*1:Not 100% TESTED

●**EEPROM DC operating characteristics** (Unless otherwise specified, Ta=-30～85℃, Vcc1=1.6～3.6V)

Parameter	Symbol	Limits			Unit	Test condition
		Min.	Typ.	Max.		
"H" Input Voltage1	VIH1	0.7xVcc1	—	Vcc1+0.3	V	2.5≦Vcc1≦3.6V
"H" Input Voltage2	VIH2	0.75xVcc1	—	Vcc1+0.3	V	1.6≦Vcc1＜2.5V
"L" Input Voltage1	VIL1	-0.3	—	0.3xVcc1	V	2.5V≦Vcc1≦3.6V
"L" Input Voltage2	VIL2	-0.3	—	0.25xVcc1	V	1.6V≦Vcc1＜2.5V
"L" Output Voltage1	VOL1	0	—	0.2	V	IOL=1.0mA , 2.5V≦Vcc1≦3.6V
"L" Output Voltage2	VOL2	0	—	0.2	V	IOL=1.0mA , 1.6V≦Vcc1＜2.5V
"H" Output Voltage1	VOH1	Vcc1-0.2	—	Vcc1	V	IOH=-0.4mA , 2.5V≦Vcc1≦3.6V
"H" Output Voltage1	VOH2	Vcc1-0.2	—	Vcc1	V	IOH=-100μA , 1.6V≦Vcc1＜2.5V
Input Leakage Current	ILI	-1	—	1	μA	VIN=0～Vcc1
Output Leakage Current	ILO	-1	—	1	μA	VOUT=0～Vcc1 , CSB=Vcc1
Operating Current Write	ICC1	—	—	1.5	mA	Vcc1=1.8V , fSCK =2MHz, tE/W=5ms Byte Write, Page Write, Write Status Register
	ICC2	—	—	2.0	mA	Vcc1=2.5V , fSCK =5MHz,tE/W=5ms Byte Write, Page Write, Write Status Register
Operating Current Read	ICC3	—	—	0.2	mA	Vcc1=1.8V , fSCK=2MHz , SO=OPEN Read, Read Status Register
	ICC4	—	—	0.6	mA	Vcc1=2.5V , fSCK=5MHz,SO=OPEN Read, Read Status Register
Standby Current	ISB	—	—	1.0	μA	Vcc1=3.6V , CSB=Vcc1 , SCK , SI=Vcc1/GND ,SO=OPEN

○This product is not designed for protection against radioactive rays.

●**EEPROM AC operating characteristics** (Ta=-30～85℃)

Parameter	Symbol	1.6≦VCC1＜1.8V			1.8≦VCC1≦3.6V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCK clock Frequency	fSCK	—	—	2.5	—	—	5	MHz
SCK High Time	tSCKWH	200	—	—	80	—	—	ns
SCK Low Time	tSCKWL	200	—	—	80	—	—	ns
CSB High Time	tCS	200	—	—	90	—	—	ns
CSB Setup Time	tCSS	150	—	—	60	—	—	ns
CSB Hold Time	tCSH	150	—	—	60	—	—	ns
SCK Setup Time	tSCKS	50	—	—	50	—	—	ns
SCK Hold Time	tSCKH	50	—	—	50	—	—	ns
SI Setup Time	tDIS	50	—	—	20	—	—	ns
SI Hold Time	tDIH	50	—	—	20	—	—	ns
Output Data Delay Time	tPD	—	—	100	—	—	80	ns
Output Hold Time	tOH	0	—	—	0	—	—	ns
Outuput Disable Time *1	tOZ	—	—	200	—	—	80	ns
SCK Rise Time *1	tRC	—	—	1	—	—	1	μs
SCK Fall Time *1	tFC	—	—	1	—	—	1	μs
Output Rise Time *1	tRO	—	—	50	—	—	50	ns
Output Fall Time *1	tFO	—	—	50	—	—	50	ns
Write Cycle Time	tE/W	—	—	5	—	—	5	ms
Wait Time From Vcc1 ON To EEPROM Command	tON	15	—	—	15	—	—	ms

*1 : Not 100% tested

●Synchronous data input/output timing

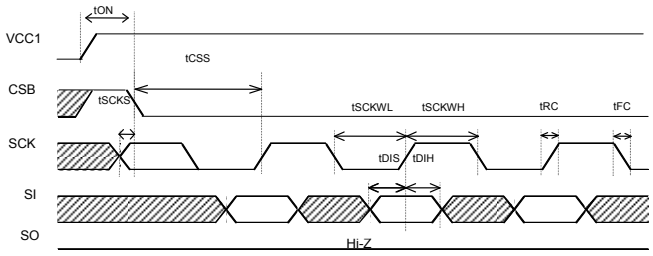


Fig.1 Input timing

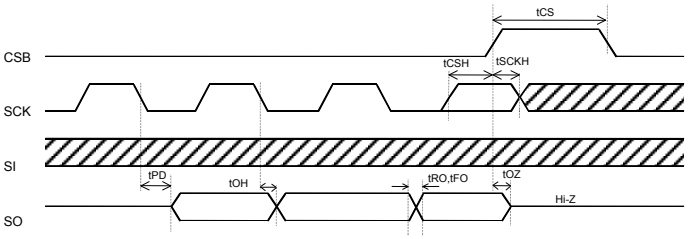


Fig.2 Input and output timing

SI data is latched into the chip at the rising edge of SCK clock. Address and data must be transferred from MSB.

SO data toggles at the falling edge of SCK clock. Output data toggles from MSB.

●AC condition

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Load Capacitance	CL	-	-	100	pF
Input Rise times	-	-	-	50	ns
Input Fall times	-	-	-	50	ns
Input Pulse Voltage	-	0.25Vcc1/0.75Vcc1			V
Input and Output Timing Reference Voltages	-	0.3VCc1/0.7Vcc1			V

●Pin configuration

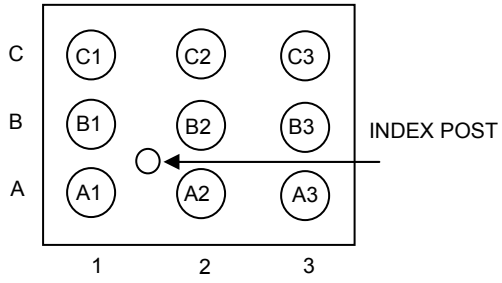


Fig.3 Pin configuration (bottom view)

●Pin function

Land No.	Pin Name	I/O	Function
A1	Vcc1	—	Power Supply (EEPROM)
A2	CSB	IN	Chip Select Control
A3	SCK	IN	Serial Data Clock Input
B1	Vcc2	—	Power Supply (LDO)
B2	SI	IN	Start Bit, Op.code, Address, Serial Data Input
B3	SO	OUT	Serial Data Output
C1	V_{OUT}	OUT	LDO Regulator Output
C2	GND	—	Ground (0V)
C3	LDOEN	IN	LDO Regulator Enable

●LDO regulator DC operating characteristics (Unless otherwise specified Ta=-30～85℃)

Parameter	Symbol	Specification			Unit	test condition
		Min.	Typ.	Max.		
Output Voltage1-1	VOUT1-1	2.9	3.0	3.2	V	3.2V≦Vcc2≦3.6V, IOUT=0, 2mA, VSET=1, 0=[1:1]
Output Voltage1-2	VOUT1-2	2.9	3.0	3.1	V	3.2V≦Vcc2≦3.6V, IOUT=2, 10mA, VSET=1, 0=[1:1]
Output Voltage2-1	VOUT2-1	2.8	2.9	3.1	V	3.1V≦Vcc2≦3.6V, IOUT=0, 2mA, VSET=1, 0=[1:0]
Output Voltage2-2	VOUT2-2	2.8	2.9	3.0	V	3.1V≦Vcc2≦3.6V, IOUT=2, 10mA, VSET=1, 0=[1:0]
Output Voltage3-1	VOUT3-1	2.7	2.8	3.0	V	3.0V≦Vcc2≦3.6V, IOUT=0, 2mA, VSET=1, 0=[0:1]
Output Voltage3-2	VOUT3-2	2.7	2.8	2.9	V	3.0V≦Vcc2≦3.6V, IOUT=2, 10mA, VSET=1, 0=[0:1]
Output Voltage4-1	VOUT4-1	2.6	2.7	2.9	V	2.9V≦Vcc2≦3.6V, IOUT=0, 2mA, VSET=1, 0=[0:0]
Output Voltage4-2	VOUT4-2	2.6	2.7	2.8	V	2.9V≦Vcc2≦3.6V, IOUT=2, 10mA, VSET=1, 0=[0:0]
Operating Current	ICC	-	-	200	μA	Vcc2=3.6V, IOUT=0A
Standby Current	ISB	-	-	1.0	μA	Vcc2=3.6V, IOUT=0A, LDOEN=GND
“H” Input Voltage	VIH	1.4	-	Vcc2+0.3	V	2.9V≦Vcc2≦3.6V
“L” Input Voltage	VIL	-0.3	-	0.6	V	2.9V≦Vcc2≦3.6V

○This product is not designed for protection against radioactive rays.

●LDO regulator AC operating characteristics

Parameter	Symbol	Specification			Unit	Test condition
		Min.	Typ.	Max.		
Vcc1 Rise Time	tVCC1	-	-	5	msec	VCC1 x 0%→VCC1 x 95% point
LDOEN Wait Time	tLDOEN	15	-	-	msec	VCC1 x 0%point→ LDOEN=High

●Output voltage depend on VSET bit

The 2bit data are stored into the VSET memory and output voltage change among VOUT1～VOUT4.
VSET data are Written into non-volatile memory array. Initial VSET data is 1,0 in VSET[1:0] and VOUT is 2.9V.

STEP	VOUT(typ.) [V]	VSET1	VSET0
VOUT1	3.0	1	1
VOUT2	2.9	1	0
VOUT3	2.8	0	1
VOUT4	2.7	0	0

●Input power supply regulation timing

①Using EEPROM PART

In case of using EEPROM part, be sure to raise Vcc1 up to operating voltage. In this time, Vcc2 has no connection with operating.

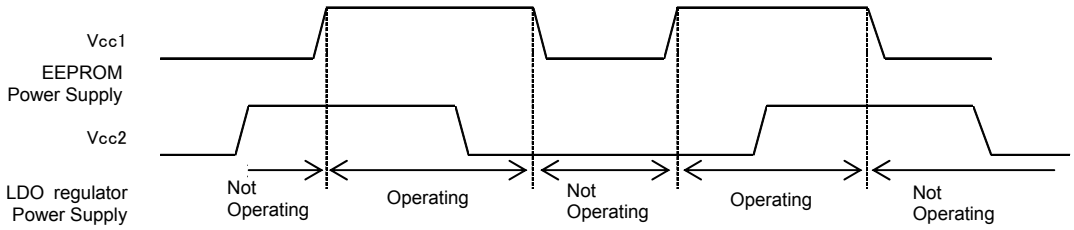


Fig.4 Using EEPROM Part, Regulation Timing

②Using LDO regulator part

In case of using LDO regulator part, be sure to raise Vcc1 and Vcc2 up to operating voltage.
After rising Vcc1, wait 15msec and rising LDOEN.
When LDOEN is raised, Vcc1 must be operating voltage.

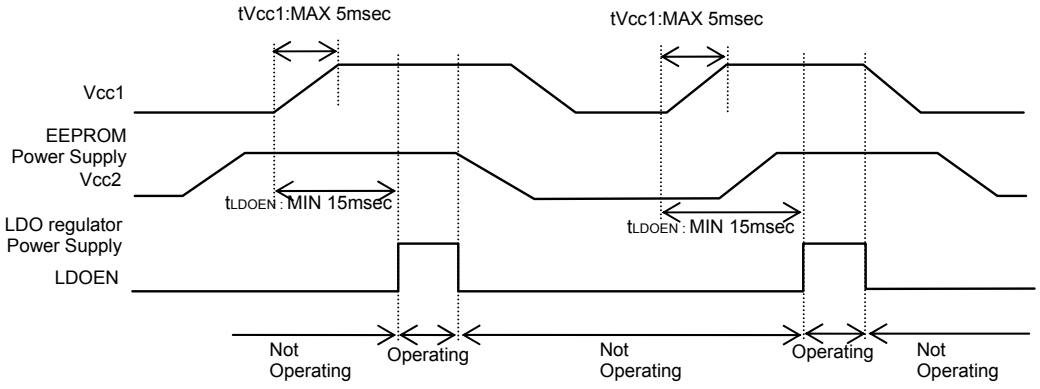


Fig.5 Using LDO Regulator Part, Regulation Timing

●Block diagram

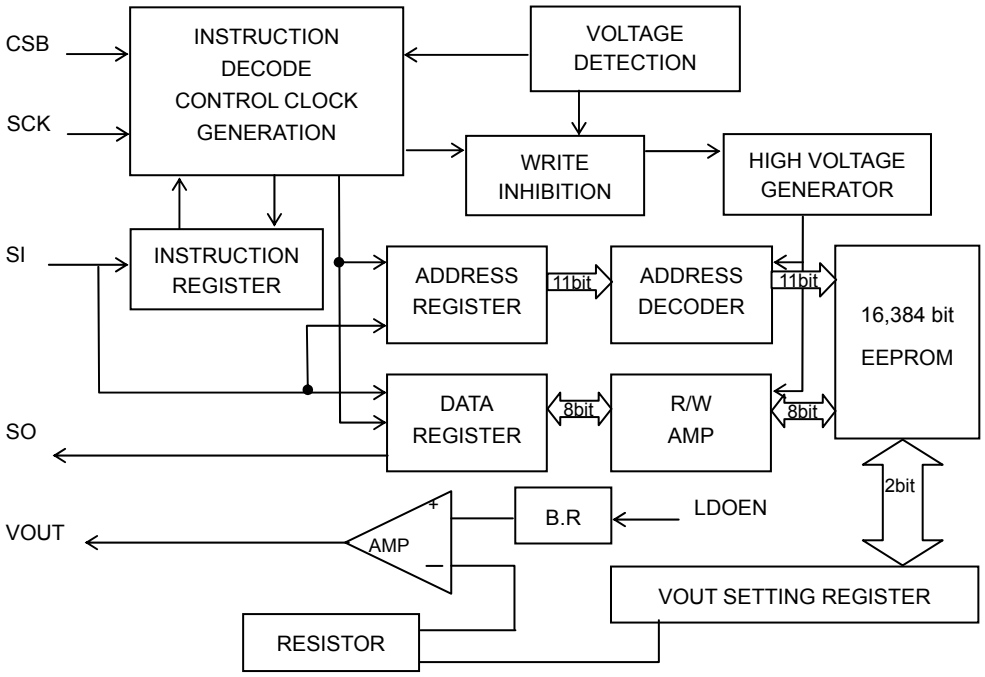


Fig.6 Block diagram

●Characteristic data (The following characteristic data are typical values.)

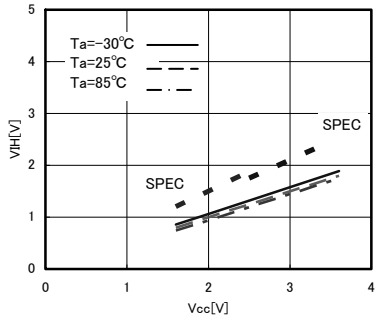


Fig.7 "H" input voltage VIH (EEPROM)

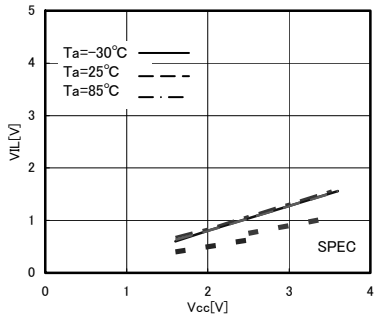


Fig.8 "L" input voltage VIL (EEPROM)

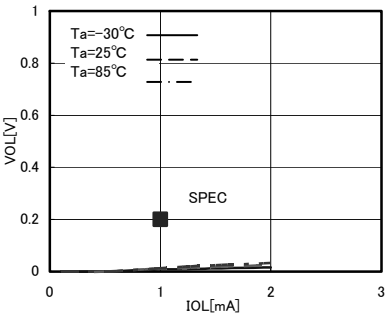


Fig.9 "L" output voltage VOL

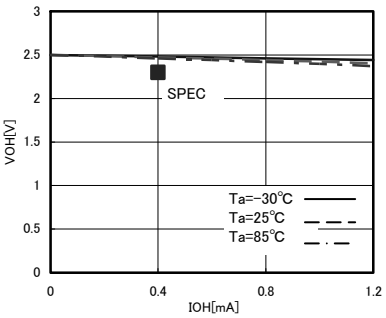


Fig.10 "H" output voltage VOH

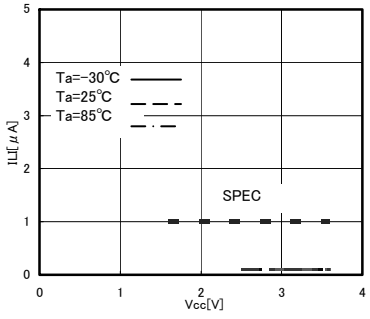


Fig.11 Input leak current ILI

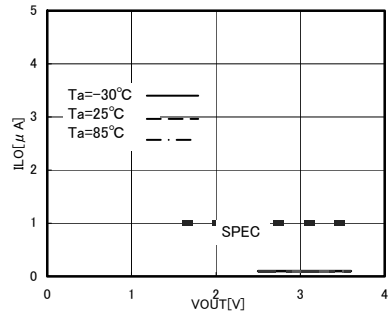


Fig.12 Output leak current ILO

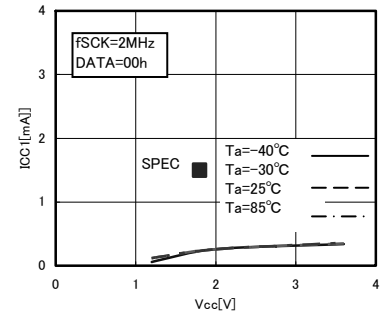


Fig.13 Current consumption at WRITE operation ICC1

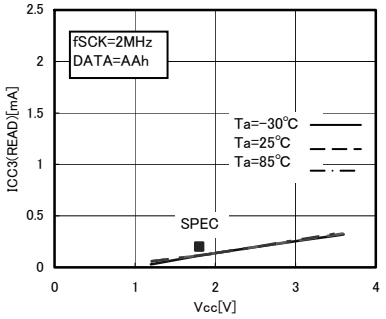


Fig.14 Consumption Current at READ operation ICC3

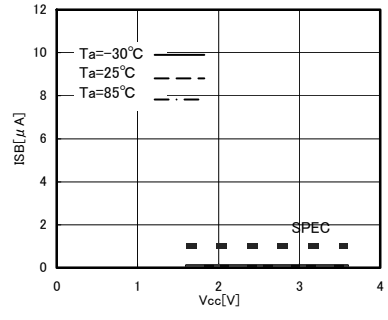


Fig.15 Standby operation ISB (EEPROM)

●Characteristic data

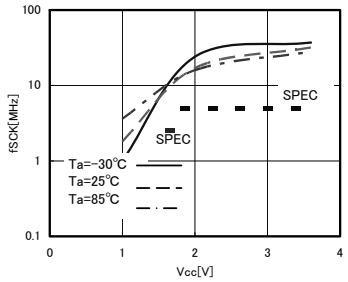


Fig.16 SCK frequency fSCK

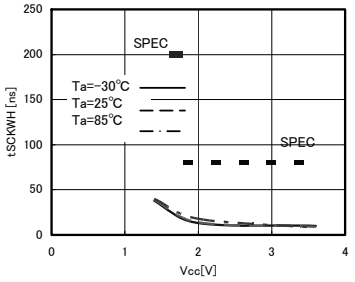


Fig.17 SCK high time tSCKWH

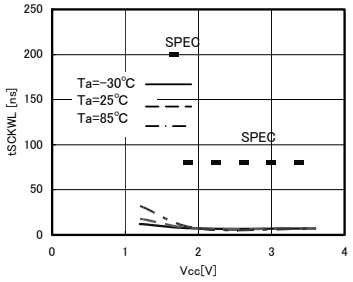


Fig.18 SCK low time tSCKWL

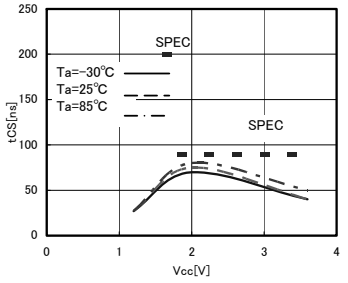


Fig.19 CSB high time tCS

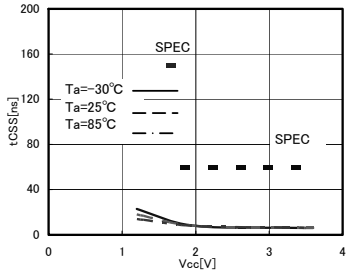


Fig.20 CSB setup time tCSS

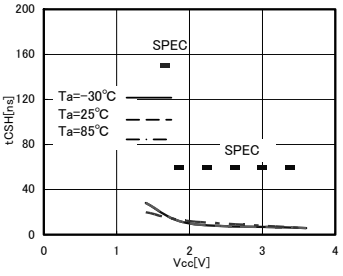


Fig.21 CSB hold time tCSH

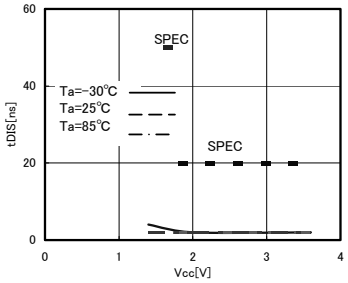


Fig.22 SI setup time tDIS

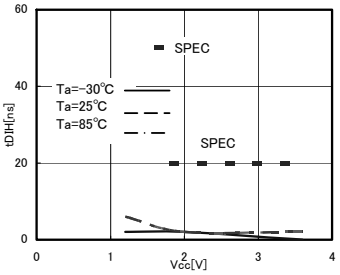


Fig.23 SI hold time tDIH

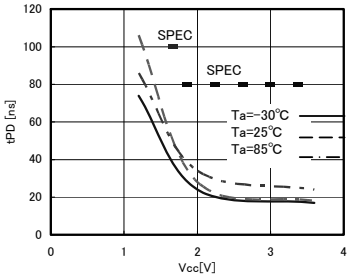


Fig.24 Data output delay time tPD

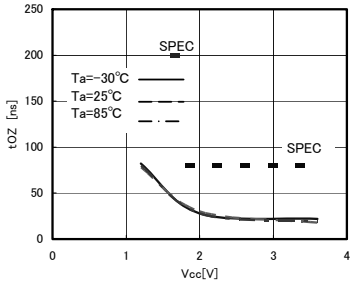


Fig.25 Output disable time tOZ

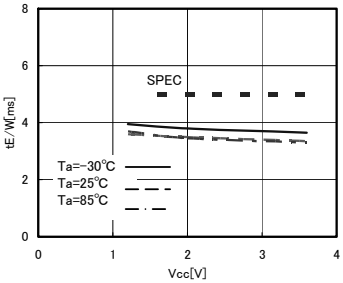


Fig.26 Write cycle time tE/W

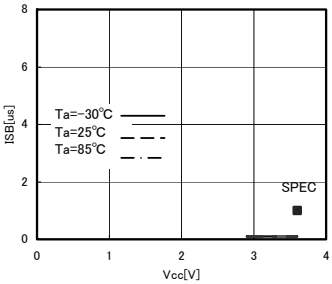


Fig.27 Standby operation ISB (LDO)

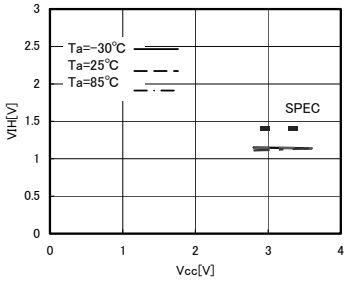


Fig.28 "H" input voltage VIH (LDO)

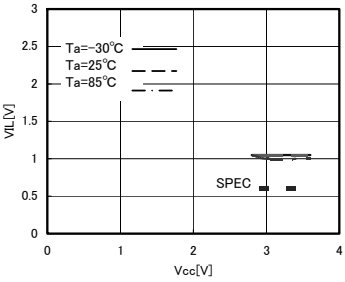


Fig.29 "L" input voltage VIL (LDO)

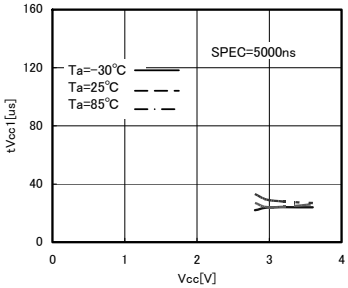


Fig.30 Vcc1 rise time tVcc1

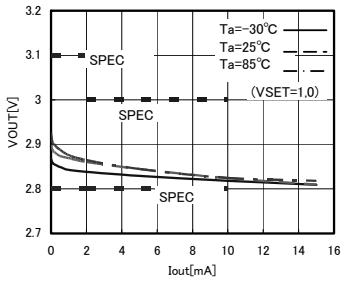


Fig.31 Vout response (LDO)

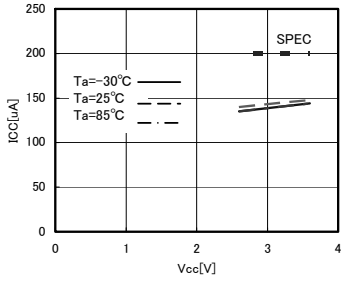


Fig.32 Current consumption ICC (LDO)

●Functional description

○Status Register

The device has status register.

Status register consists of 8bits and is shown following parameters.

2 bits (BP0 and BP1) are set by “Write Status Register” commands, which are non-volatile.

Specification of endurance and data retention are as well as memory array. WEN bit is set by “Write Enable” and “Write Disable” commands. After power become on, the device is disable mode. $\overline{R}/B$ bit is a read-only and status bit. The device is clocked out value of the status register by “Read Status Register” command input.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	BP1	BP0	WEN	$\overline{R}/B$

Bit	Definition
BP0/BP1	Block write protection for memory array (EEPROM)
WEN	Write enable/disable status bit WEN=0 : write disable WEN=1 : write enable
$\overline{R}/B$	READY/BUSY status bit $\overline{R}/B$ =0 : READY $\overline{R}/B$ =1 : BUSY

BP1	BP0	Block Write Protection
0	0	NONE
0	1	600h-7FFh
1	0	400h-7FFh
1	1	000h-7FFh

●Instruction code

Instruction	Operation	Op.Code	Address
WREN	Write enable	0000 0110	-
WRDI	Write disable	0000 0100	-
READ	Read data from memory array	0000 0011	A10 ～ A0
WRITE	Write data to memory array	0000 0010	A10 ～ A0
RDSR	Read status register	0000 0101	-
WRSR	Write status registe r	0000 0001	-
VSET_READ	Read VSET data	0000 0011	800h
VSET_WRITE	Write VSET data	0000 0010	800h

●Timing chart

1. WRITE ENABLE

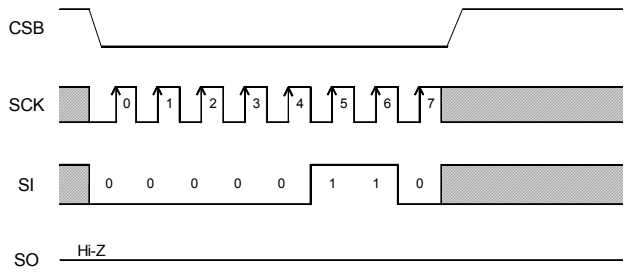


Fig.33 WRITE ENABLE CYCLE TIMING

2. WRITE DISABLE

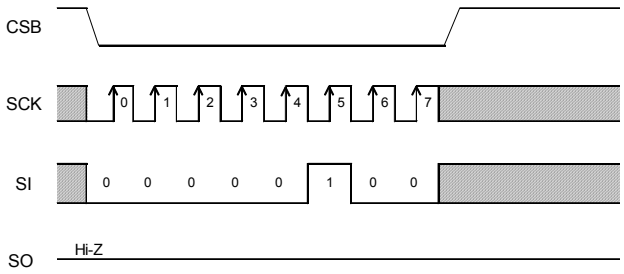


Fig.34 WRITE DISABLE CYCLE TIMING

○The device has both of the enable and disable mode. After “Write Enable” is executed, the device becomes in the enable mode. After “Write Disable” is executed, the device becomes in the disable mode. After CSB goes low, each of Op.code is recognized at the rising edge of 7th clock. Each of instructions is effective inputting seven or more SCK clocks. This “Write Enable” instruction must be proceeded before the any write commands. The device ignores inputting the any write commands in the disable mode. Once the any write commands is executed in the enable mode, the device becomes the disable mode. After the power become on, the device is in the disable mode.

3. READ

The data stored in the memory are clocked out after “Read” instruction is received. After CSB goes low, the address need to be sent following by Op.code of “Read”. The data at the address specified are clocked out from D7 to D0, which is start at the falling edge of 23th clock. This device has the auto-increment feature that provides the whole data of the memory array with one read command, outputs the next address data following the addressed 8bits of data by keeping SCK clocking. When the highest address is reached, the address counter rolls over to the lowest address allowing the continuous read cycle.

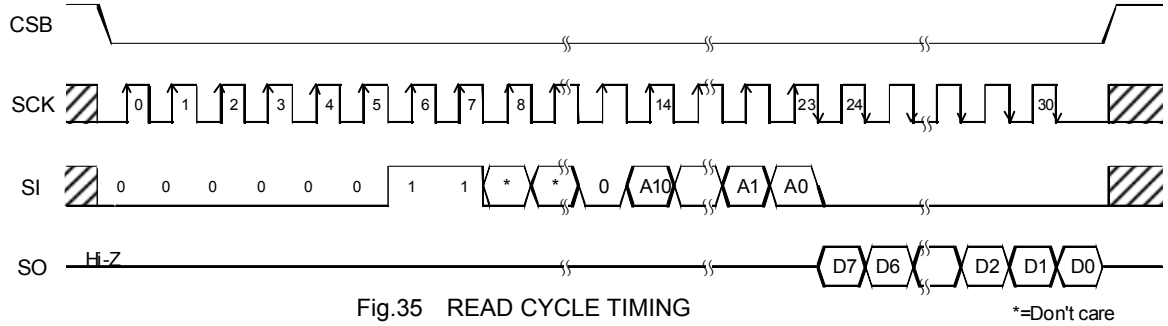


Fig.35 READ CYCLE TIMING

*=Don't care

4. WRITE

This “Write” command writes 8bits of data into the specified address. After CSB goes low, the address need to be sent following by Op.code of “Write”. Between the rising edge of the 29th clock and it of the 30th clock, the rising edge of CSB initiates high voltage cycle, which writes the data into non-volatile memory array, but the command is cancelled if CSB is high except that period. It takes maximum 5ms in high voltage cycle (tE/W). The device does not receive any command except for “Read Status Register” command during this high voltage cycle. This device is capable of writing the data of maximum 32byte into memory array at the same time, which keep inputting two or more byte data with CSB “L” after 8bits of data input. For this Page Write commands, the eight higher order bits of address are set, the six low order address bits are internally incremented by 5bits of data input. If more than 16 words, are transmitted the address counter “roll over”, and the previous transmitted data is overwritten.

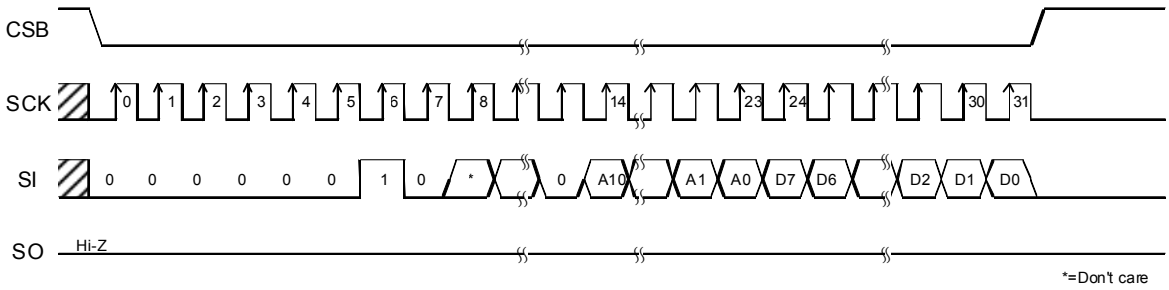


Fig. 36 WRITE CYCLE TIMING

5. RDSR (READ STATUS REGISTER)

The data stored in the status register is clocked out after “Read Status Register” instruction is received.

After CSB goes low, Op.colde of “Read Status Register” need to sent. The data stored in the status register is clocked out of the device on the falling edge of 7th clock. Bit7, Bit6, Bit5 and Bit4 in the status register are read as 0.

This device has the auto-increment feature as well as “Read” that output the 8bits of the same data following it to keep SCK clocking. It is possible to see ready and busy state by executing this command during tE/W. If more than 16 words, are transmitted the address counter “roll over” and the previous transmitted data is overwritten.

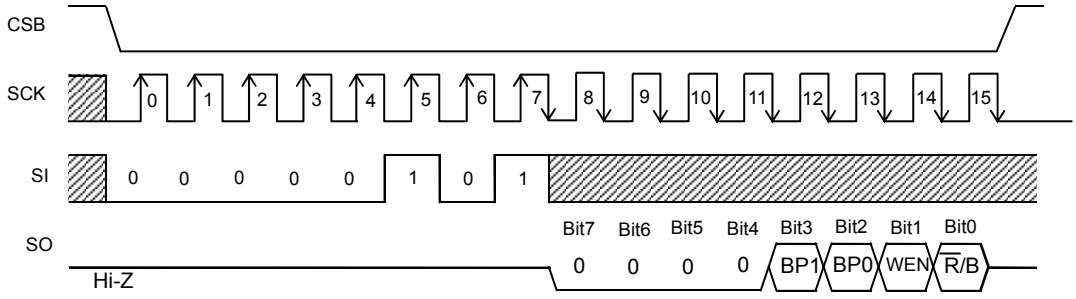


Fig.37 READ STATUS REGISTER CYCLE TIMING

6. WRSR (WRITE STATUS RESISTER)

This “Write Status Register” command writes the data, two (BP1, BP0) of the eight bits, into the status register. Write protection is set by BP1 and BP0 bits. After CSB goes low, Op.code of “Read Status Register” need to sent. Between the rising edge of the 15th clock and it or the 16th clock, the rising edge of CSB initiates high voltage cycle, which writes the data into non-volatile memory array, but the command is cancelled if CSB is high except that period. It takes maximum 5ms in high voltage cycle (tE/W) as well as “Write”.Block write protection is determined by BP1 and BP0 bits, which is selected from quarter, half and the entire memory array. (See Table2 BLOCK WRITE PROTECTION>)

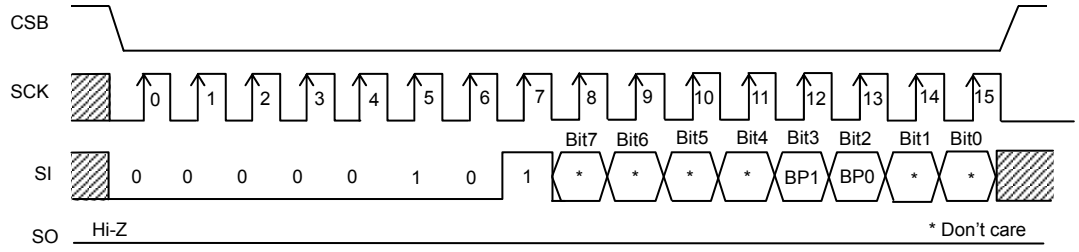


Fig. 38 WRITE STATUS REGISTER WRITE CYCLE TIMING

7. VSET READ

The VSET data stored in the memory are clocked out after “VSET Read” instruction set address 800h is received.
After CSB goes low, the address (800h) need to be sent following by Op.code of “Read”. 0 are clocked out from D7 to D2 and the VSET data are clocked out from D1 to D0, which is start at the falling edge of 23th clock.

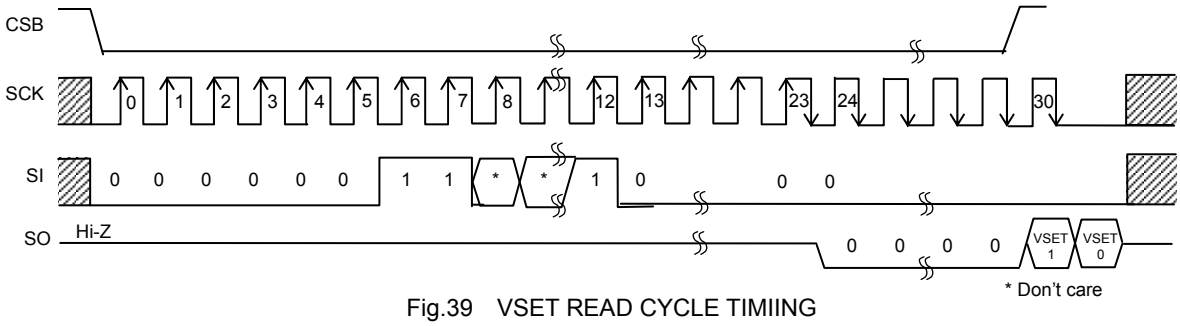


Fig.39 VSET READ CYCLE TIMIING

8. VSET WRITE

This “Write” command set address 800h writes VSET data into VSET1 and VSET0 memory array. After CSB goes low, the address (800h) and VSET data need to be sent following by Op.code of “VSET Write”. Between the rising edge of the 29th clock and it of the 30th clock, the rising edge of CSB initates high voltage cycle, which writes the data into non-volatile memory array, but the command is cancelled if CSB is high except that period. It takes maximum 5ms in high voltage cycle (tE/W). The device does not receive any command except for “Read Status Register” command during this high voltage cycle.

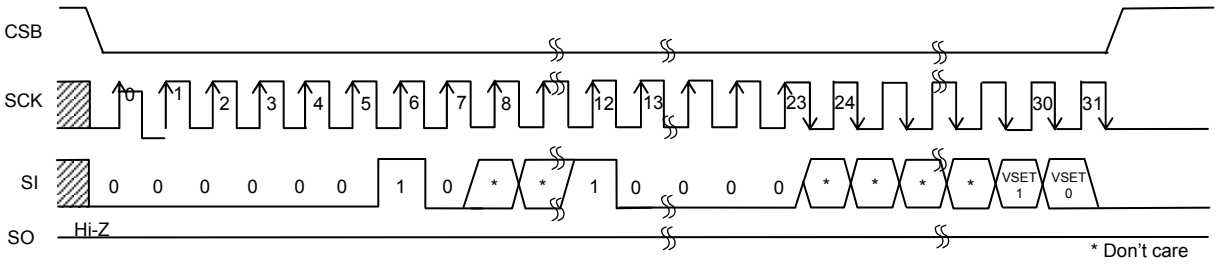


Fig. 40 VSET WRITE CYCLE TIMING

●EEPROM soft ware

○READ, VSET_READ, RDSR Command cancel

Cancel of these commands is possible by changing CSB pin to “HIGH” in all sections.

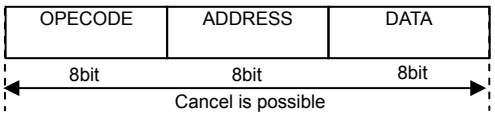


Fig.41 READ, VSET_READ Cancel Timing

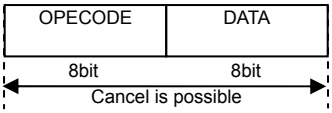


Fig.42 RDSR Cancel Timing

○WRITE, PAGE_WRITE, VSET_WRITE、WRSR Command cancel

Cancel of these write command is possible by changing CSB pin to “HIGH” in opecode, address and data input sections (section a~b), but it is impossible after data input section (section c~d), if Vcc1 is OFF during tE/W, please write again because write data is not guaranteed in specified address, if SCK and CSB rise at the same time in section C, command is instability. It is recommend to rise CSB in “SCK=L” section.

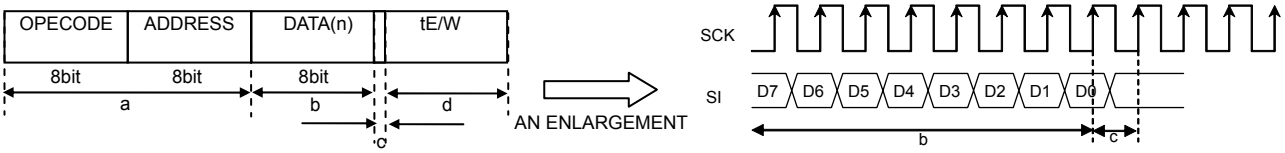


Fig.43 WRITE, PAGE_WRITE, VSET_WRITE READ VSET_READ Cancel Timing

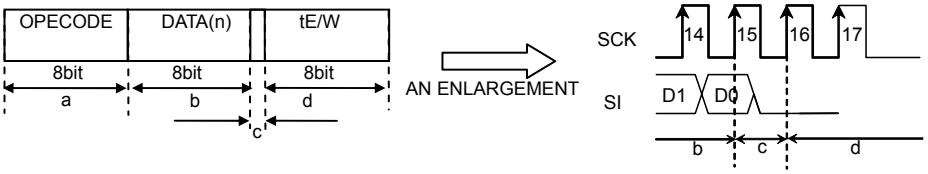


Fig.44 WRSR Cancel Timing

○WREN, WRDI command cancel

Cancel of these commands is possible by changing CSB pin to “HIGH” of opecode to rising 8 clk, but it is impossible after rising 8 clk. In the case, please send WREN or WRDI cancel timing command again.

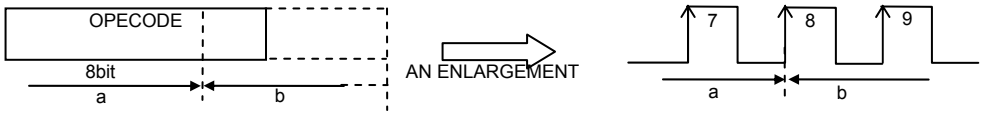


Fig.45 WREN, WRDI Cancel Timing

●Data polling

If RDSR command is carried out daring tE/W, according to out put data ($\overline{R}/B$ bit), to monitor READY/BUSY state is possible. Because of this, it is possible to send next command earlier than regular programming time (tE/W MAX=5ms). If $\overline{R}/B$ bit is “1”, EEPROM’s state is “BUSY”. If this becomes “0”, it is possible to send next command to change EEPROM to “READY” state. Status register data read by this command in tE/W is not data written by WRSR command but old data before. Status register data in each section is shown below.

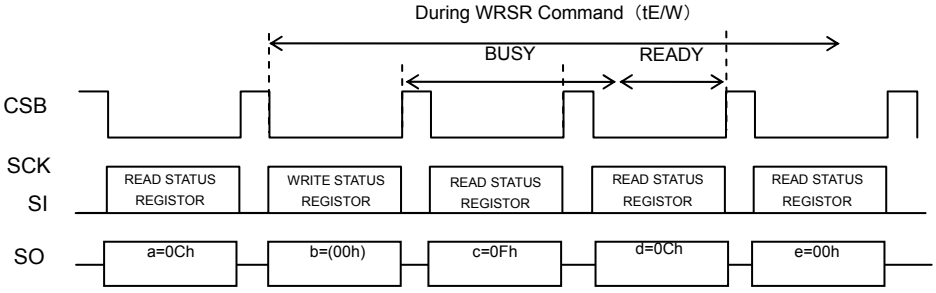


Fig.46 Status register data in each section

●EEPROM part

1. Hardware Connection of EEPROM

EEPROM may have malfunction owing to noise signal for input pin, and movement in the low voltage region at power ON/OFF. These malfunctions may occur, especially at min voltage limit of EEPROM or below.
To avoid this, please note about hardware connection showed as follows.

1.1 Input Terminals

Input equivalent circuits of CSB, SCK and SI are showed Fig.47, 48.
Input terminal is connected between CMOS schmitt trigger input circuit and input protection circuit.
These pin are not pull up or pull down, therefore please don't input Hi-Z in use. And please make CSB "HIGH" in the low voltage region at power ON/OFF. If CSB is "LOW" at power ON/OFF, malfunction may occur. To make other input terminals pull up or pull down is recommendable.

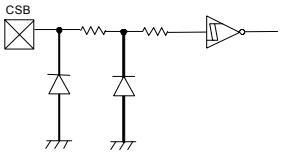


Fig.47 CSB terminals equivalent circuit

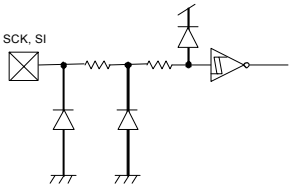


Fig.48 SCK,SI terminals equivalent circuit

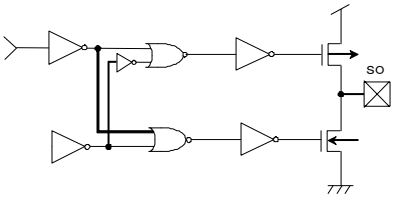


Fig.49 SO terminals equivalent circuit

1.2 Output Terminals

Output equivalent circuit of so is showed Fig.49. This output terminal is 3 states buffer.
The data is output from so at output timing by READ command, so is Hi-z except this timing. If EEPROM malfunction occur by Hi-z input of the microcontroller port connected with so, please make so pull up or pull down. If it doesn't affected the microcontroller movement to make so open, it is no problem. Load capacity of so disturb high speed movement of EEPROM. If this load capacity is 100pF or below, BU9829GUL-W can move in 2.5MHz (Vcc1=1.6V~1.8V) or 5MHz (Vcc1=1.8V~3.6V)

1.3 Input pin pull up, pull down resistance

The design method of pull up/pull down resistance for input and output are as follows.

1.3.1 Pull up resistance Rpu of input terminals

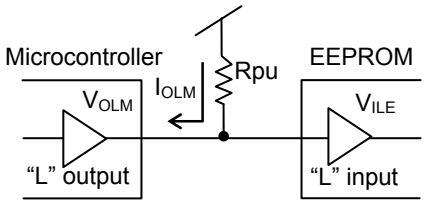


Fig.50 Input terminal pull up resistance

$$Rpu \geqq \frac{V_{CC}-V_{OLM}}{I_{OLM}} \quad \cdots ①$$

$$V_{OLM} \leqq V_{ILE} \quad \cdots ②$$

Example) When Vcc=5V, V_{ILE}=1.5V, V_{OLM}=0.4V, I_{OLM}=2mA,
from the equation①,

$$Rpu \geqq \frac{5-0.4}{2\times10^{-3}}$$

$$\therefore Rpu \geqq 2.3[k\Omega]$$

- V_{ILE} : EEPROM V_{IL} specifications
- V_{OLM} : Microcontroller V_{OL} specifications
- I_{OLM} : Microcontroller I_{OL} specifications

With the value of Rpu to satisfy the above equation, V_{OLM} becomes 0.4V or below, and with V_{ILE}(=1.5V), the equation ② is also satisfied.

1.3.2 Pull down resistance Rpd of input terminals

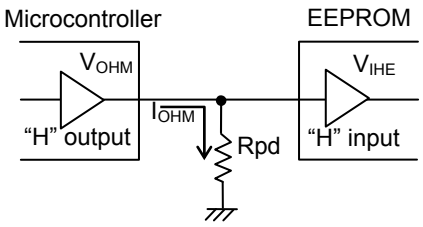


Fig.51 Input terminals Pull down resistance

$$Rpd \geqq \frac{V_{OHM}}{I_{OHM}} \quad \cdots ①$$

$$V_{OHM} \leqq V_{IHE} \quad \cdots ②$$

Example) When Vcc=5V, V_{IHE}=3.5V, V_{OHM}=2.4V, I_{OHM}=2mA,
from the equation①,

$$Rpd \geqq \frac{2.4}{2\times10^{-3}}$$

$$\therefore Rpd \geqq 1.2\ [k\Omega]$$

- V_{IHE} : EEPROM V_{IH} specifications
- V_{OHM} : Microcontroller V_{OH} specifications
- I_{OHM} : Microcontroller I_{OH} specifications

With the value of Rpd to satisfy the above equation, V_{OHM} becomes 2.4V or higher, and with V_{IHE}(=3.5V), the equation②is also satisfied.

1.3.3 Pull up resistance Rpu of SO pin

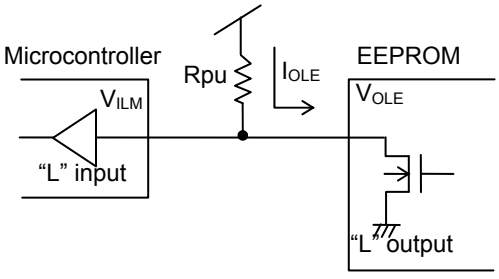


Fig.52 SO Pull up resistance

$$Rpu \geqq \frac{V_{CC}-V_{OLE}}{I_{OLE}} \quad \cdots ①$$

$$V_{OLE} \leqq V_{ILM} \quad \cdots ②$$

Example) When Vcc=5V, V_{OLE}=0.4V, V_{ILM}=1.5V, I_{OLE}=2.1mA,
from the equation①,

$$Rpu \geqq \frac{5-0.4}{2.1\times10^{-3}}$$

$$\therefore Rpu \geqq 2.2\ [k\Omega]$$

- V_{OLE} : EEPROM V_{OL} specifications
- I_{OLE} : Microcontroller I_{OL} specifications
- V_{ILM} : Microcontroller V_{IL} specifications

With the value of Rpd to satisfy the above equation, V_{OLE} becomes 0.4V or higher, and with V_{ILM}(=1.5V), the equation②is also satisfied.

1.3.4 Pull up resistance Rpu of SO pin

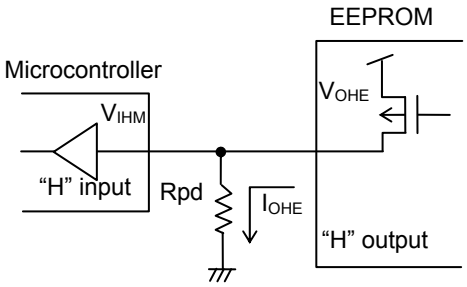


Fig.53 SO Pull down resistance

$$Rpd \geqq \frac{V_{OHE}}{I_{OHE}} \quad \cdots ①$$

$$V_{OHE} \geqq V_{IHM} \quad \cdots ②$$

Example) When Vcc=5V, V_{OHE}=Vcc-0.5V, V_{IHM}=Vccx0.7V, I_{OHE}=0.4mA,
from the equation①,

$$Rpd \geqq \frac{5-0.5}{0.4\times10^{-3}}$$

$$\therefore Rpd \geqq 11.3\ [k\Omega]$$

- V_{OHE} : EEPROM V_{OH} specifications
- I_{OHE} : EEPROM I_{OH} specifications
- V_{IHM} : Microcontroller V_{IH} specifications

With the value of Rpu to satisfy the above equation, V_{OHE} becomes 4.5V or higher, and with V_{IHM}(=3.5V), the equation ② is also satisfied.

●LDO regulator part

LDO regulator part of BU9829GUL-W is CMOSLDO of low power consumption. The data are stored into EEPROM and output voltage change among 2.7~3.0V. 1step is 0.1V. LDO regulator part had LDOEN pin and VOUT pin. To make this LDOEN pin LOW is standby mode of low power consumption.

○LDOEN Input Terminals

Input equivalent circuit of LDOEN is showed Fig.54. Input terminal is connected between input circuits made from NMOS and pull up and input protection circuit. This pin is not pull up or pull down, therefore please don't input Hi-z. If LDOEN is LOW, all circuit don't move and LDO part is standby mode of low power consumption.

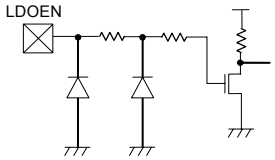


Fig.54 VOUT output terminals

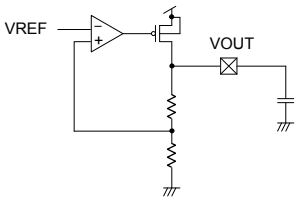
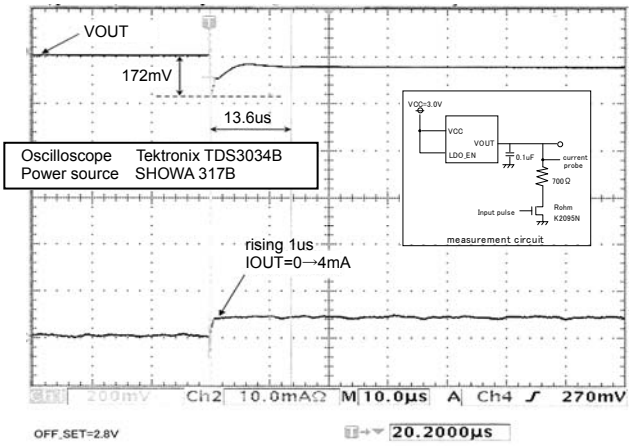


Fig.55 VOUT output terminals

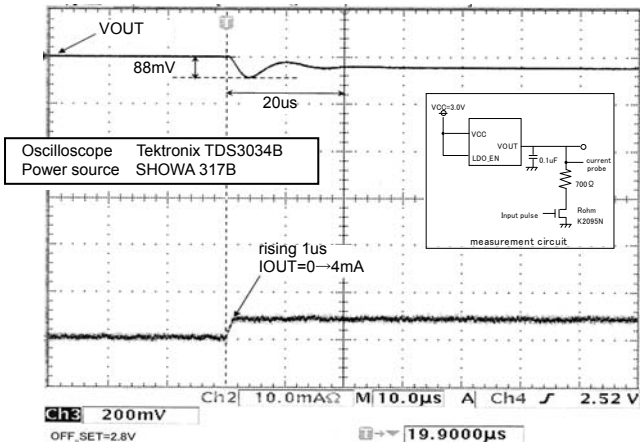
○VOUT Output Terminals

Output equivalent circuit of VOUT is showed Fig.55. If LDOEN is HIGH, LDO regulator output regulate voltage from VOUT pin. If LDOEN is LOW, VOUT pin is GND by VOUT-GND resistance. Output overshoots change by output capacity, in actual use, please evaluate and decide output capacity.



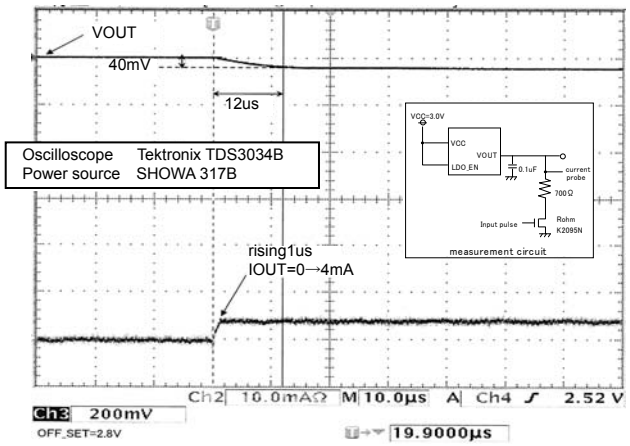
BU9829GUL-W Evaluation result
(I_{OUT}=0mA→4mA,C_{OUT}=1.0uF)

Fig.56 CL=0µF Transitional response



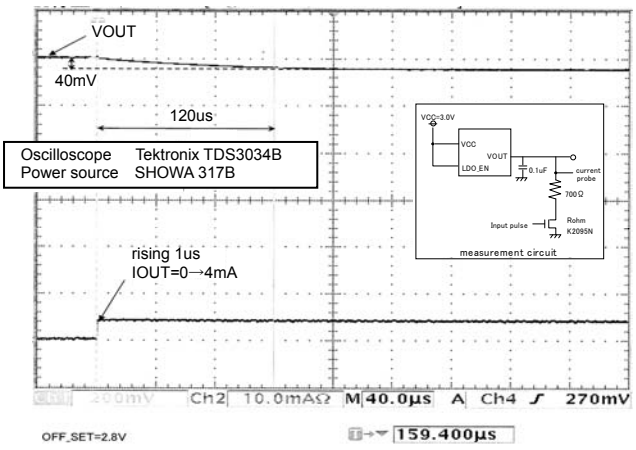
BU9829GUL-W Evaluation result
(I_{OUT}=0mA→4mA,C_{OUT}=0.1uF)

Fig.57 CL=0.1µF Transitional response



BU9829GUL-W Evaluation result
(I_{OUT}=0mA→4mA,C_{OUT}=1.0uF)

Fig.58 CL=1.0µF Transitional response



BU9829GUL-W Evaluation result
(I_{OUT}=0mA→4mA,C_{OUT}=1.0uF)

Fig.59 CL=10µF Transitional response

○Package power dissipation

Package power dissipation of BU9829GUL-W is 220mW. It is the value at environmental temperature is 25℃. In the case of use at 25℃ or higher, degradation is done at 2.2W/℃. If output current is very large, please take care of package power dissipation.

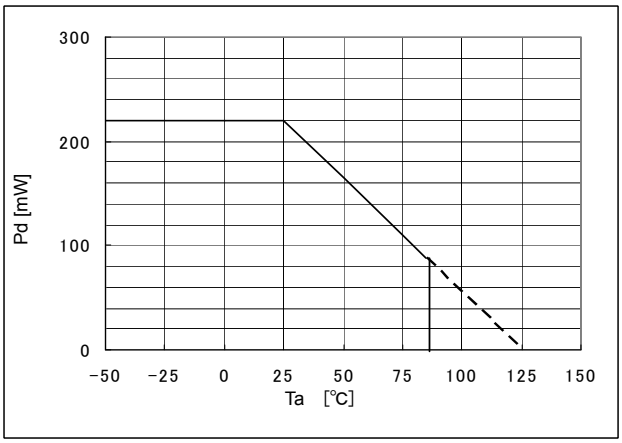


Fig.60 Package power dissipation

○Large Current Protection Circuit

VOUT terminal has large current protection circuit. This circuit protects IC from large current. However, this protection circuit effective unexpected accident. Please avoid continual use of protection circuit.

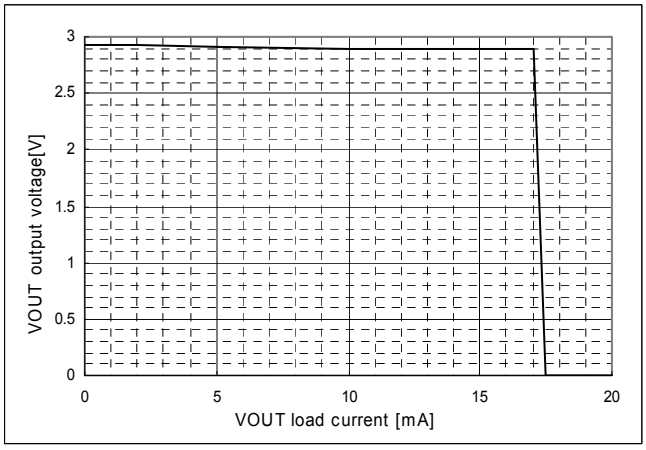


Fig.61 Large Current Protection Circuit

●POR circuit

This IC has a POR (Power On Reset) circuit as mistake write countermeasure. After POR action, it gets in write disable. The POR circuit is valid only when power is ON, and does not work when power is OFF. When power is ON, if the recommended conditions of the following tR, tOFF, and Vbot are not satisfied, it may become write enable status owing to noise the likes.

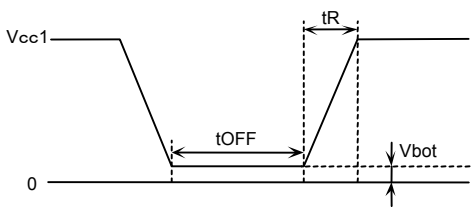


Fig.62 Rise waveform

Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

●LVCC circuit

LVCC (Vcc-Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.
At LVCC voltage (Typ. =1.9V) or below, it prevent data rewrite.

●Noise countermeasures

○Vcc noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1μF) between IC Vcc and GND. At that moment, attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

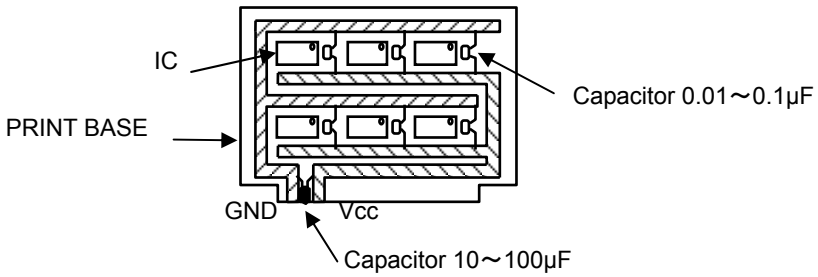


Fig.63 Vcc noise countermeasures example

●Recommendable application circuit

1. It is recommended to attach bypass condensers on power line.
2. Be sure to make CSB pull up. At power on, mat cause the abnormal function.
3. Please make LDOEN pull down.
4. If EEPROM malfunction occur by Hi-Z input of the microcontroller part connected with SO, please make SO pull up or pull down.
5. Please attach capacity at VOUT terminal. Outputs overshoot change by output capacity. In actual use, please evaluate and decide output capacity.

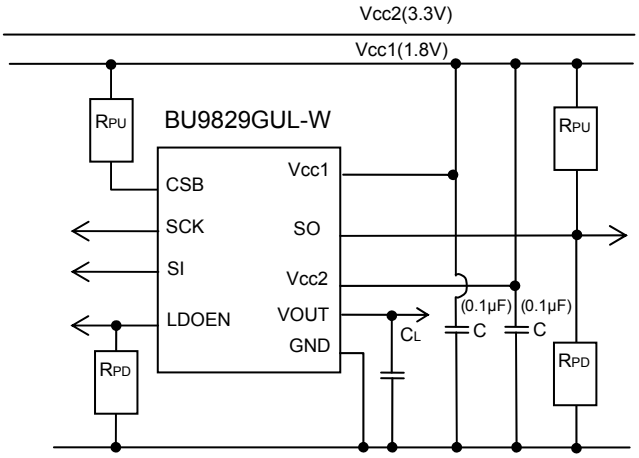


Fig.64 Recommendable Application circuit

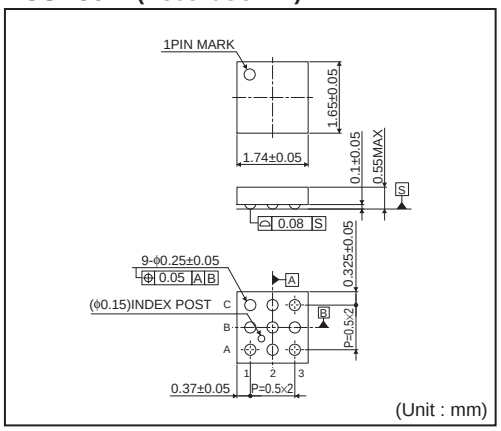
●Notes for use

- Absolute maximum ratings
  We pay attention to quality control of this IC, but if there is special mode exceeded absolute maximum rating, please take a physical safety measures. Because we can't specify short mode and open made, etc.
- Heat design
  In consideration of permissible dissipation in actual use condition, carry out heat design with sufficient margin.
- Absolute maximum ratings
  If the absolute maximum ratings such as impressed voltage and operating temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.
- Common impedance
  Please pay attention to VCC and GND wiring. For example, lower common impedance and to make wiring think, etc.
- GND electric potential
  Set the voltage of GND terminal lowest at any action condition. And, please make pin except GND voltage of GND or over.
- Test of set base
  If low impedance pin connect with capacity at test of set base, please discharge each test progress to stress IC. Please embroider earth for static electricity neasures at structure progress, pay attention to carry and conservation. When set base connect with test base at test progress, please connect and remove from power OFF.

●Ordering part number

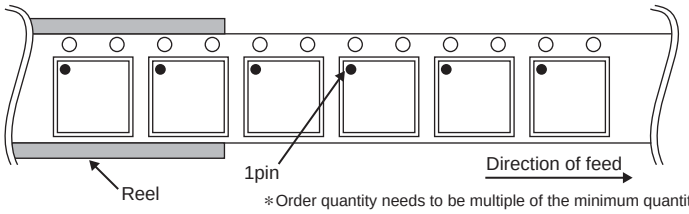
B	U	9	8	2	9	G	U	L	-	W	E	2
Part No.		Part No.				Package GUL : VCSP50L1				W-CELL	Packaging and forming specification E2: Embossed tape and reel	

VCSP50L1(BU9829GUL-W)



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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