

IT500-IT505

Monolithic Dual Cascoded N-Channel JFET General Purpose Amplifier

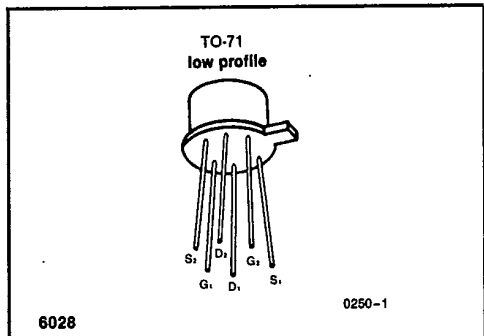


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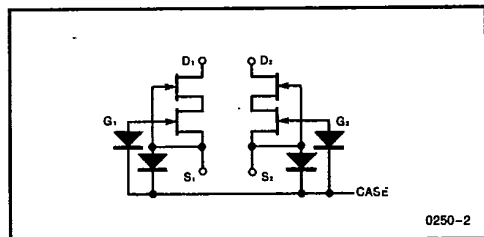
GENERAL DESCRIPTION

A low noise, low leakage FET that employs a cascode structure to accomplish very low I_G at high voltage levels, while giving high transconductance and very high common, mode rejection ratio.

PIN CONFIGURATION



SCHEMATIC DIAGRAM



FEATURES

- $CMRR > 120dB$
- $I_G < 5pA$ @ 50V_{DG}
- $C_{rss} < 0.5pF$
- $g_{os} > .025\mu S$

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ C$ unless otherwise specified)

Drain-Source and Drain-Gate Voltages (Note 1)	60V
Drain Current (Note 1)	50mA
Gate-Gate Voltage	$\pm 60V$
Storage Temperature	$-65^\circ C$ to $+200^\circ C$
Operating Temperature	$-55^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering, 10sec)	$+300^\circ C$

	One Side	Both Sides
Power Dissipation (Note 3)	250mW	500mW
Derate above $25^\circ C$	3.8mW/ $^\circ C$	7.7mW/ $^\circ C$

NOTE 1. Per transistor.

NOTE 2. Due to the non-symmetrical structure of these devices, the drain and source ARE NOT interchangeable.

NOTE 3. @ $85^\circ C$ free air temp.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-71
IT500
IT501
IT502
IT503
IT504
IT505

INTERISL'S SOLE AND EXCLUSIVE WARRANTY OBLIGATION WITH RESPECT TO THIS PRODUCT SHALL BE THAT STATED IN THE WARRANTY ARTICLE OF THE CONDITION OF SALE. THE WARRANTY SHALL BE EXCLUSIVE AND SHALL BE IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE.

NOTE: All typical values have been characterized but are not tested.

IT500-IT505**INTERSIL****IT500-IT505****ELECTRICAL CHARACTERISTICS** ($T_A = 25^\circ\text{C}$ unless otherwise specified)

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Symbol	Characteristics	Test Conditions	Limits		Units
			Min	Max	
I_{GSS}	Gate Reverse Current	$V_{GS} = -20\text{V}$, $V_{DS} = 0$, $T_A = 125^\circ\text{C}$		-100	pA
				-5	nA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu\text{A}$, $V_{DS} = 0$	-50		
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 20\text{V}$, $I_D = 1\text{nA}$	-0.7	-4	V
V_{GS}	Gate-Source Voltage		-0.2	-3.8	
I_G	Gate Operating Current	$V_{DG} = 35\text{V}$, $I_D = 200\mu\text{A}$, $T_A = 125^\circ\text{C}$		-5	pA
				-5	nA
I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 20\text{V}$, $V_{GS} = 0$	0.7	7	mA
g_{fs}	Common-Source Forward Transconductance (Note 1)	$V_{DS} = 20\text{V}$, $V_{GS} = 0$	1000	4000	μs
g_{fs}	Common-Source Forward Transconductance (Note 1)	$V_{DG} = 20\text{V}$, $I_D = 200\mu\text{A}$	500	1600	
g_{os}	Common-Source Output Conductance	$V_{DS} = 20\text{V}$, $V_{GS} = 0$		1	
g_{os}	Common-Source Output Conductance	$V_{DS} = 20\text{V}$, $I_D = 200\mu\text{A}$		0.025	
C_{g1g2}	Gate to Gate Capacitance (Note 4)	$V_{G1} = V_{G2} = 10\text{V}$		3.5	pF
C_{iss}	Common-Source Input Capacitance (Note 4)	$V_{DS} = 20\text{V}$, $V_{GS} = 0$	$f = 1\text{MHz}$	7	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 3, 4)			0.5	
NF	Spot Noise Figure (Note 4)			0.5	dB
$\bar{e}_n$	Equivalent Input Noise Voltage (Note 4)			50	$\mu\text{V}/\sqrt{\text{Hz}}$
			$f = 1\text{kHz}$	15	

Symbol	Characteristics	Test Conditions	IT500		IT501		IT502		IT503		IT504		IT505		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$I_{G1-I_{G2}}$	Differential Gate Current	$V_{DG} = 20\text{V}$, $I_D = 200\mu\text{A}$, $T_A = 125^\circ\text{C}$		5		5		5		5		10		15	nA
I_{DSS1} I_{DSS2}	Saturation Drain Current Ratio (Note 1)	$V_{DS} = 20\text{V}$, $V_{GS} = 0\text{V}$	0.95	1	0.95	1	0.95	1	0.95	1	0.9	1	0.85	1	
g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	$f = 1\text{kHz}$	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	0.85	1	

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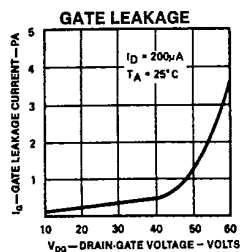
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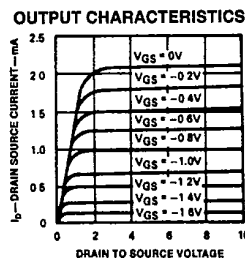
ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristics	Test Conditions	IT500		IT501		IT502		IT503		IT504		IT505		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{GS1}-V_{GS2}$	Differential Gate-Source Voltage	$V_{DG} = 20\text{V}$ $I_D = 200\mu\text{A}$		5		5		10		15		25		50	mV
$\Delta V_{GS1}-V_{GS2}$	Gate-Source Differential Voltage	$T_A = 25^\circ\text{C}$ $T_B = 125^\circ\text{C}$		5		10		20		40		100		200	$\mu\text{V}/^\circ\text{C}$
ΔT	Change with Temp. (Note 2, 4)			5		10		20		40		100		200	
C_{MRR} (Note 5)	Common Mode Rejection Ratio (Note 4)	$\Delta V_{DD} = 10\text{V}$, $I_D = 200\mu\text{A}$	120		120		120		120		120		120		dB

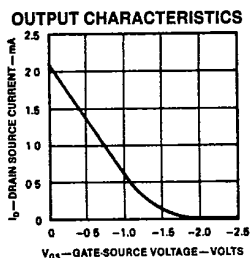
- NOTES: 1. Pulse test required, pulsewidth = 300 μs , duty cycle $\leq 3\%$.
 2. Measured at end points, T_A and T_B .
 3. With case guarded C_{RSS} is typically $< 0.15\text{pF}$.
 4. For design reference only, not 100% tested.
 5. $C_{MRR} = 20 \log_{10} \Delta V_{DD} / \Delta [V_{GS1}-V_{GS2}]$, $\Delta V_{DD} = 10/-20\text{V}$

TYPICAL PERFORMANCE CHARACTERISTICS

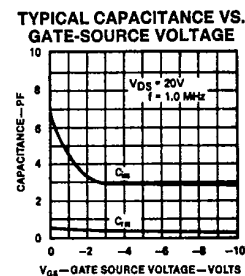
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0250-7

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