

Rev. V12

#### **Features**

- Attenuation: 0.5 dB Steps to 31.5 dB
- Low DC Power Consumption
- Small Footprint, JEDEC Package
- Integral TTL Driver
- 50 ohm Impedance
- · Test Boards are Available
- Tape and Reel Packaging Available
- CSP-1 Package

## **Description**

M/A-COM's AT90-0107 is a GaAs FET 6-bit digital attenuator with integral TTL driver. Step size is 0.5 dB providing a 31.5 dB total attenuation range. This device is in an PQFN plastic surface mount package. The AT90-0107 is ideally suited for use where accuracy, fast speed, very low power consumption and low costs are required.

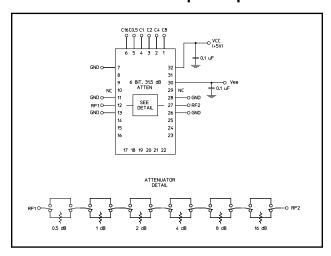
## **Ordering Information**

Part Number	Package		
AT90-0107	Bulk Packaging		
AT90-0107TR	1000 piece reel		
AT90-0107-TB	Sample Test Board		

Note: Reference Application Note M513 for reel size information.

Commitment to produce in volume is not guaranteed.

## **Schematic with Off-Chip Components**



# Pin Configuration<sup>2</sup>

Pin No.	Function	Pin No.	Function
1	C8	17	NC
2	C4	18	NC
3	C2	19	NC
4	C1	20	NC
5	C0.5	21	NC
6	C16	22	NC
7	GND	23	NC
8	NC	24	NC
9	NC	25	NC
10	NC <sup>1</sup>	26	GND
11	GND	27	RF2
12	RF1	28	GND
13	GND	29	NC <sup>1</sup>
14	NC	30	-Vee
15	NC	31	NC
16	NC	32	+Vcc

- 1. Pins 10 & 29 must be isolated
- The exposed pad centered on the package bottom must be connected to RF and DC ground. (For PQFN Packages)

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Rev. V12

# Electrical Specifications: $T_A = +25$ °C, $Vee = -5 \text{ V} \pm 0.25 \text{ V}$ , $Vcc = +5 \text{ V} \pm 0.25 \text{ V}$

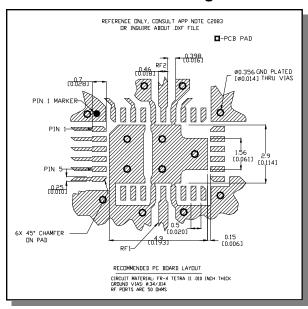
Parameter	Test Conditions	Frequency	Units	Min	Тур	Max
Insertion Loss	_	DC - 4.0 GHz	dB	_	4.5	5.1
Attenuation Accuracy	Individual Bits 0.5-1-2-4-8-16 dB Any Combination of Bits 1 to 31.5 dB	DC - 4.0 GHz DC - 4.0 GHz	dB dB	_	_	±(.3 +7% of atten setting) ±(.5 +8% of atten setting)
VSWR	Full Range	DC - 4.0 GHz	Ratio	_	2.0:1	2.2:1
Switching Speed	50% Cntl to 90%/10% RF 10% to 90% or 90% to 10%	_	ns ns	_	75 20	_
1 dB Compression	_ _	50 MHz 0.5 - 4.0 GHz	dBm dBm	_	+21 +24	_
Input IP <sub>3</sub>	Two-tone inputs up to +5 dBm	50 MHz 0.5-4.0 GHz	dBm dBm	_	+35 +48	_
V <sub>IL</sub> V <sub>IH</sub>	LOW-level input voltage HIGH-level input voltage	_	V V	0.0 2.0	_	0.8 5.0
lin (Input Leakage Current)	Vin = V <sub>CC</sub> or GND	_	uA	-1.0	_	1.0
Icc (Quiescent Supply Current)	Vcntrl = V <sub>CC</sub> or GND	_	uA	_	250	400
ΔIcc (Additional Supply Current Per TTL Input Pin)	$V_{CC}$ = Max, Vcntrl = $V_{CC}$ - 2.1 V	_	mA	_	_	1.0
lee	VEE min to max, Vin = V <sub>IL</sub> or V <sub>IH</sub>	_	mA	-1.0	-0.2	_
Thermal Resistance θjc	_	_	°C/W	_	15	_

# **Absolute Maximum Ratings** <sup>3,4</sup>

Parameter	Absolute Maximum
Max. Input Power 0.05 GHz 0.5 - 4.0 GHz	+27 dBm +34 dBm
V <sub>CC</sub>	-0.5V ≤ V <sub>CC</sub> ≤ +7.0V
V <sub>EE</sub>	-8.5V ≤ V <sub>EE</sub> ≤ +0.5V
V <sub>CC</sub> - V <sub>EE</sub>	-0.5V ≤ V <sub>CC</sub> - V <sub>EE</sub> ≤ 14.5V
Vin <sup>5</sup>	-0.5V ≤ Vin ≤ V <sub>CC</sub> + 0.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +125°C

- 3. Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.
- Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

# Recommended PCB Configuration<sup>6</sup>



- 6. Application Note S2083 is available on line at www.macom.com
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Rev. V12

## **Handling Procedures**

Please observe the following precautions to avoid damage:

# **Static Sensitivity**

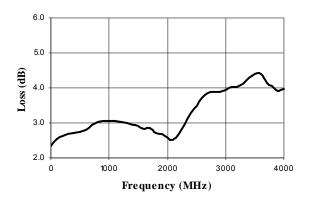
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

## **Moisture Sensitivity**

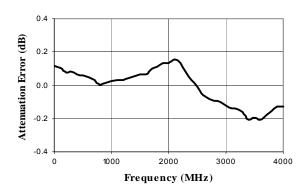
The MSL rating for this part is defined as Level 2 per IPC/JEDEC J-STD-020. Parts shall be stored and/or baked as required for MSL Level 2 parts.

# Typical Performance Curves

#### Insertion Loss



## Attenuation Error, 0.5 dB Bit

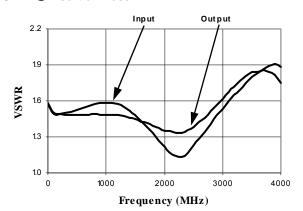


## Truth Table (Digital Attenuator)

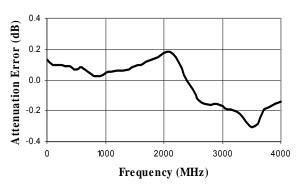
C16	C8	C4	C2	C1	C0.5	Attenuation
0	0	0	0	0	0	Loss, Reference
0	0	0	0	0	1	0.5 dB
0	0	0	0	1	0	1.0 dB
0	0	0	1	0	0	2.0 dB
0	0	1	0	0	0	4.0 dB
0	1	0	0	0	0	8.0 dB
1	0	0	0	0	0	16.0 dB
1	1	1	1	1	1	31.5 dB

0 = TTL Low; 1 = TTL High

#### **VSWR** @ Insertion Loss



#### Attenuation Error, 1 dB Bit



3

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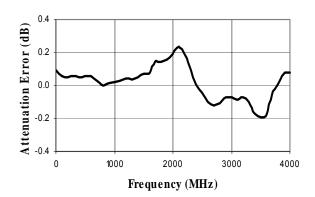
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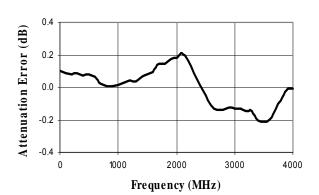
Rev. V12

## **Typical Performance Curves**

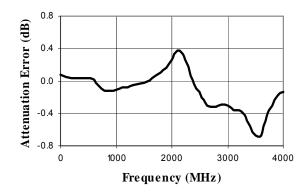
#### Attenuation Error, 2 dB Bit



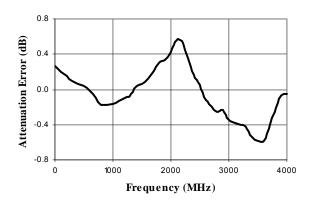
#### Attenuation Error, 4 dB Bit



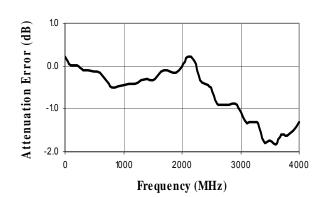
#### Attenuation Error, 8 dB Bit



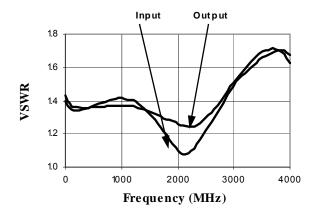
#### Attenuation Error, 16 dB Bit



## Attenuation Error, Max. Attenuation



#### VSWR, 0.5 dB Bit



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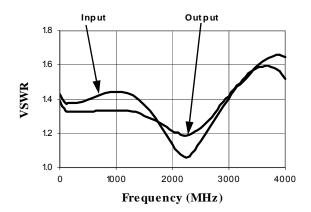
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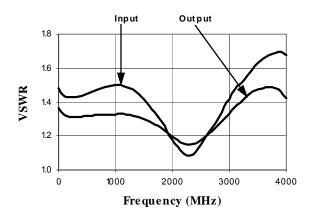
Rev. V12

# **Typical Performance Curves**

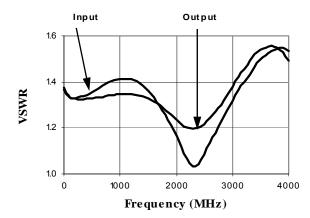
#### VSWR, 1 dB Bit



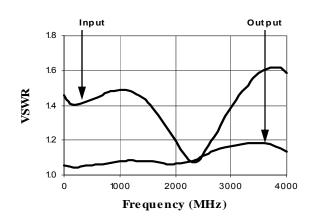
#### VSWR, 2 dB Bit



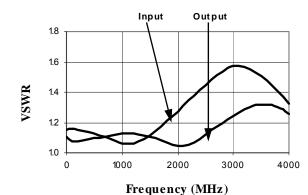
#### VSWR, 4 dB Bit



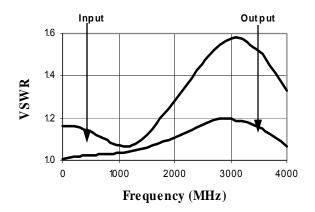
VSWR, 8 dB Bit



## VSWR, 16 dB Bit



## VSWR, Max. Attenuation



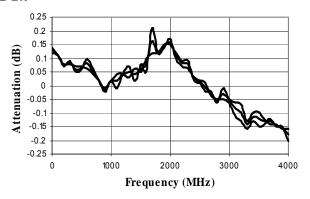
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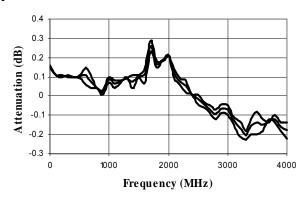
Rev. V12

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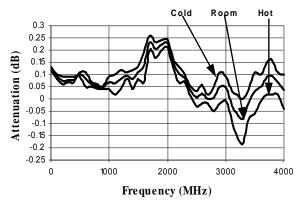
# Typical Attenuation Deviation vs. Temperature for 0.5 dB Bit



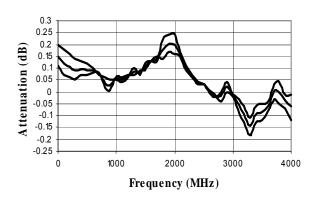
Typical Attenuation Deviation vs. Temperature for 1 dB Bit



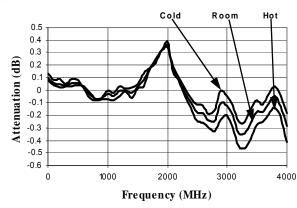
Typical Attenuation Deviation vs. Temperature for 2 dB Bit



Typical Attenuation Deviation vs. Temperature for 4 dB Bit

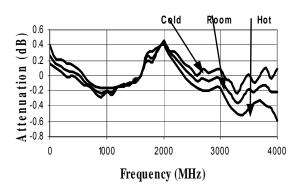


Typical Attenuation Deviation vs. Temperature for 8 dB Bit



6

Typical Attenuation Deviation vs. Temperature for 16 dB Bit



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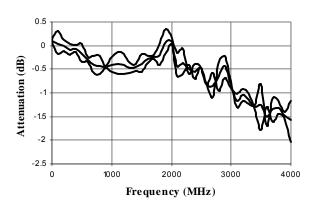
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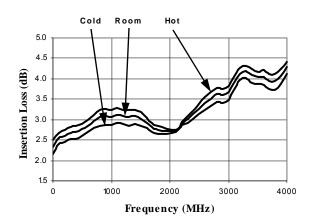
Rev. V12

## **Typical Performance Curves**

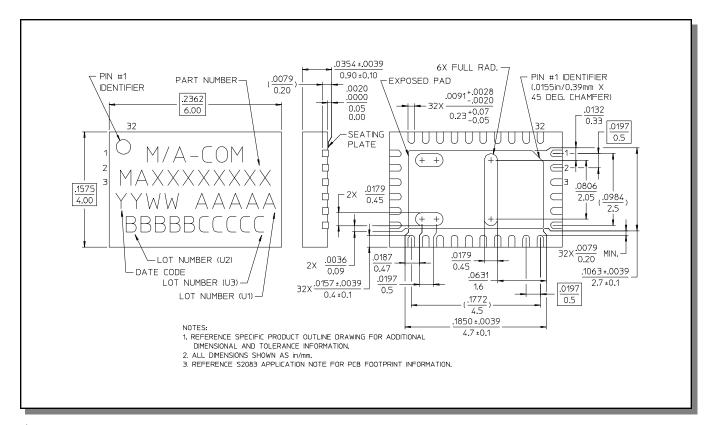
# Typical Attenuation Deviation vs. Temperature at Maximum Atten.



#### Insertion Loss vs. Temperature



# CSP-1, 4 x 6 mm, 32-lead PQFN<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> Reference Application Note M538 for lead-free solder reflow recommendations.

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