HD26C31

Quadruple Differential Line Drivers With 3 State Outputs

REJ03D0292–0200Z
(Previous ADE-205-574 (Z))
Rev.2.00
Jul.16.2004

Description

The HD26C31 features quadruple differential line drivers which satisfy the requirements of EIA standard RS-422A. This device is designed to provide differential signals with high current capability on bus lines. The circuit provides enable input to control all four drivers. The output circuit has active pull up and pull down and is capable of sinking or sourcing 20 mA.

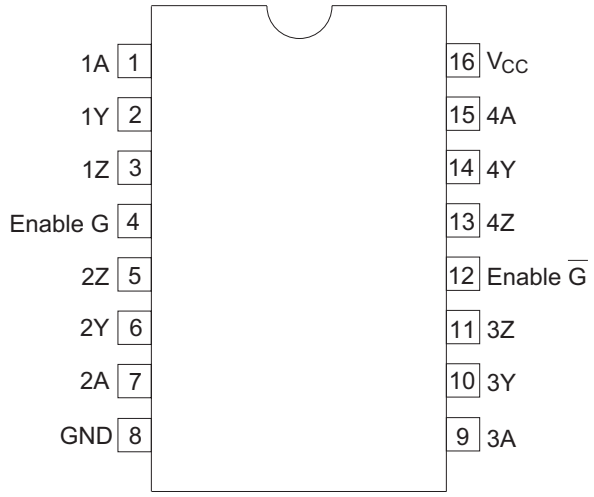
Features

- TTL input compatibility
- Propagation delay time: 6 ns typ
- Output to output skew: 0.5 ns typ
- High output impedance in power off conditions
- Meets EIA standard RS-422A
- Operates from a single 5 V supply
- Three state outputs
- Low power dissipation with CMOS process
- Power up and power down protection
- Pin to pin compatible with HD26LS31

- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD26C31FPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)

Pin Arrangement



(Top view)

Function Table

Input	Enables		Outputs	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H : High level
L : Low level
X : Irrelevant
Z : High impedance

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Supply Voltage*[2]	V_{CC}	–0.5 to 7.0	V
Input Voltage	V_{IN}	–1.5 to V_{CC} +1.5	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Power Dissipation	P_T	500	mW
Storage Temperature Range	Tstg	–65 to 150	°C
Lead Temperature*[3]	Tlead	260	°C
Output Current	I_{OUT}	±150	mA
Supply Current	I_{CC}	±150	mA

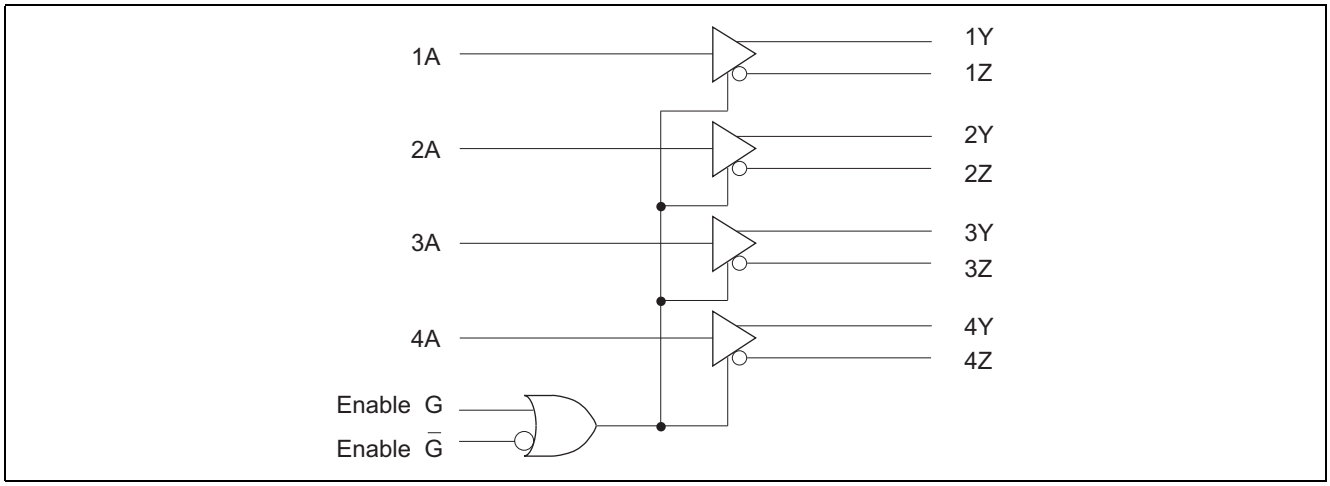
Notes: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.
2. The values is defined as of ground terminal.
3. The values at 1.6 mm away from the package within 10 second, when soldering.

Recommended Operating Conditions (Ta = –40°C to +85°C)

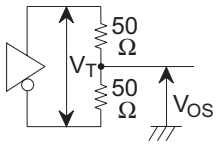
Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IN}	0	—	V_{CC}	V
Output Voltage	V_{OUT}	0	—	V_{CC}	V
Operating Temperature	Ta	–40	25	85	°C
Input Rise/Fall Time*[1]	t_r, t_f	—	—	500	ns

Note: 1. This guarantees maximum limit when one input switches.

Logic Diagram



Electrical Characteristics (Ta = –40°C to +85°C)

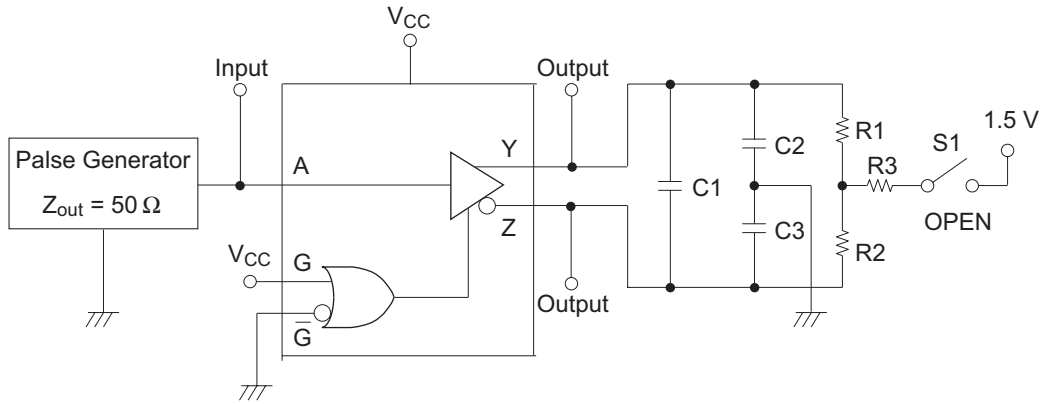
Item	Symbol	Min	Typ	Max	Unit	Conditions
Input Voltage	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8	V	
Output Voltage	V_{OH}	2.4	3.4	—	V	V_{IN} = V_{IH} or V_{IL}, I_{OH} = –20 mA
	V_{OL}	—	0.2	0.4	V	V_{IN} =V_{IH} or V_{IL}, I_{OL} = 20 mA
Differential Output Voltage	V_T	2.0	3.1	—	V	R_L = 100 Ω 
Difference In Differential Output	$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	—	—	0.4	V	
Common ModeOutput Voltage	V_{OS}	—	1.8	3.0	V	
Difference In Output Common Mode	$\lvert V_{OS} - \overline{V_{OS}} \rvert$	—	—	0.4	V	
Input Current	I_{IN}	—	—	±1.0	µA	V_{IN} = V_{CC}, GND, V_{IH} or V_{IL}
Supply Current	I_{CC}	—	200	500	µA	I_{OUT} = 0 µA, V_{IN} = V_{CC} or GND
	I_{CC}*[2]	—	0.8	2.0	mA	I_{OUT}=0 µA, V_{IN} = 2.4 V or 0.5 V
Off State Output Current	I_{OZ}	—	±0.5	±5.0	µA	V_{OUT} = V_{CC} or GND, $\overline{G}$ = V_{IL}, G = V_{IH}
Short Circuit Output Current	I_{SC}*[3]	–30	—	–150	mA	V_{IN} = V_{CC} or GND
Output Current with Power Off	I_{OFF}	—	—	100	µA	V_{CC} = 0 V, V_{OUT} = 6 V
	I_{OFF}	—	—	–100	µA	V_{CC} = 0 V, V_{OUT} = –0.25 V

Notes: 1. All typical values at V_{CC} = Ta = 25°C.
2. 1 input: V_{IN} = 2.4 V or 0.5 V, other inputs: V_{IN} = V_{CC} or GND
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics (Ta = –40°C to +85°C, V_{CC} = 5 V ± 10%)

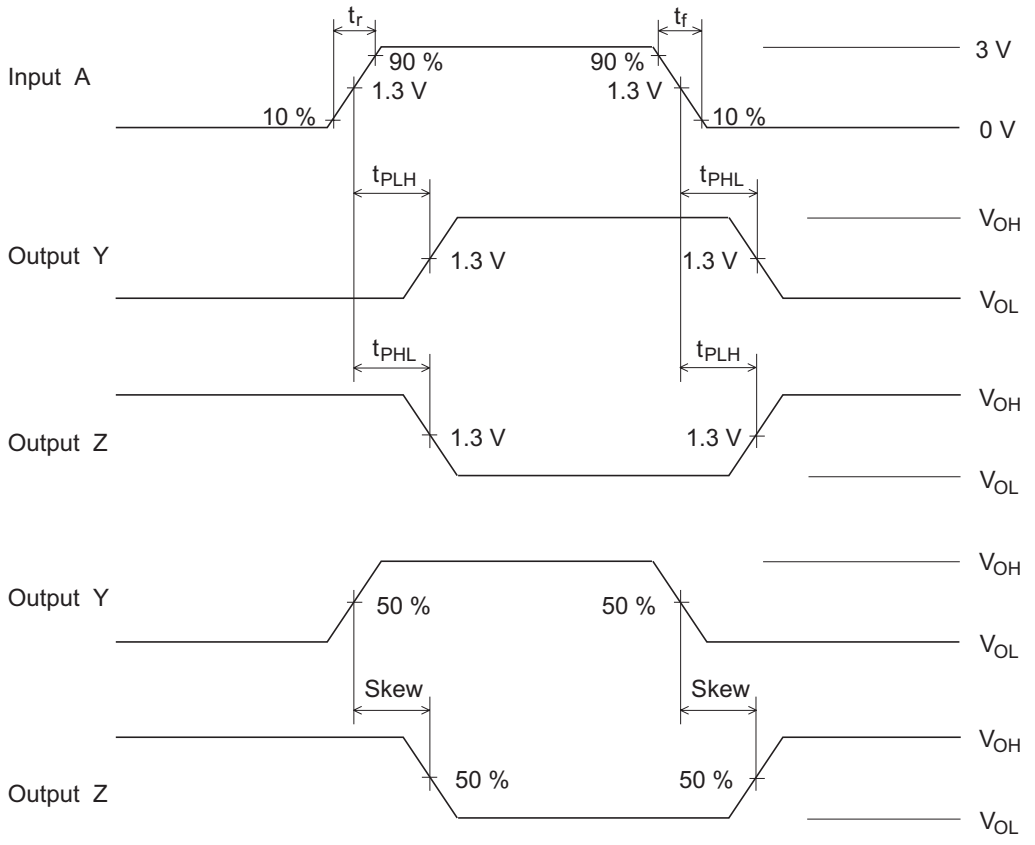
Item	Symbol	Min	Typ	Max	Unit	Conditions
Propagation Delay Time	t_{PLH}	2.0	6.0	11.0	ns	Test Circuit (1)
	t_{PHL}	2.0	6.0	11.0	ns	
Output To Output Skew	Skew	—	0.5	2.0	ns	
Differential Output Transition Time	t_{TLH}		6.0	10.0	ns	Test Circuit (3)
	t_{THL}		6.0	10.0	ns	
Output Enable Time	t_{ZL}		11.0	19.0	ns	Test Circuit (2)
	t_{ZH}	—	13.0	21.0	ns	
Output Disable Time	t_{LZ}	—	5.0	9.0	ns	
	t_{HZ}	—	7.0	11.0	ns	
Power Dissipation Capacitance	C_{PD}	—	50.0	—	pF	
Input Capacitance	C_{IN}	—	6.0	—	pF	

Test Circuit 1



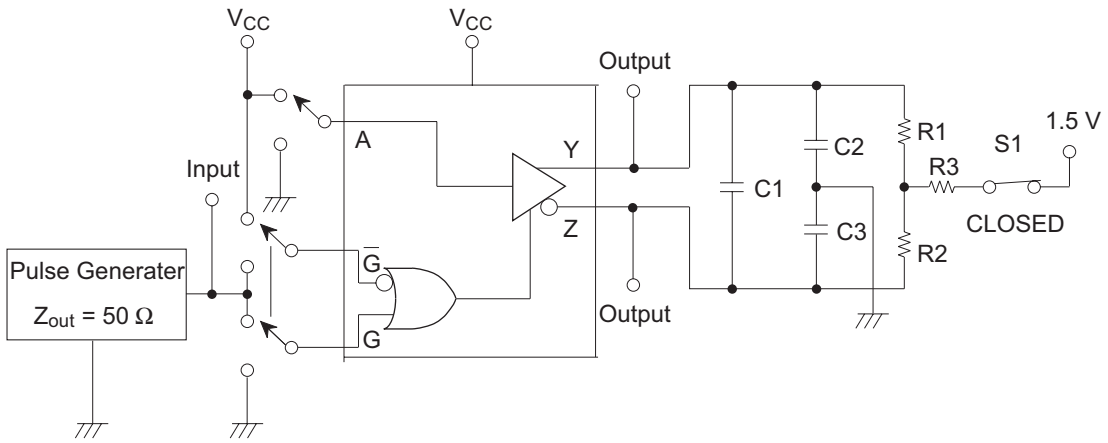
Note: 1. C1, C2 and C3 (40 pF) include probe and jig capacitance.
R1 = R2 = 50 Ω, R3 = 500 Ω

Waveforms 1



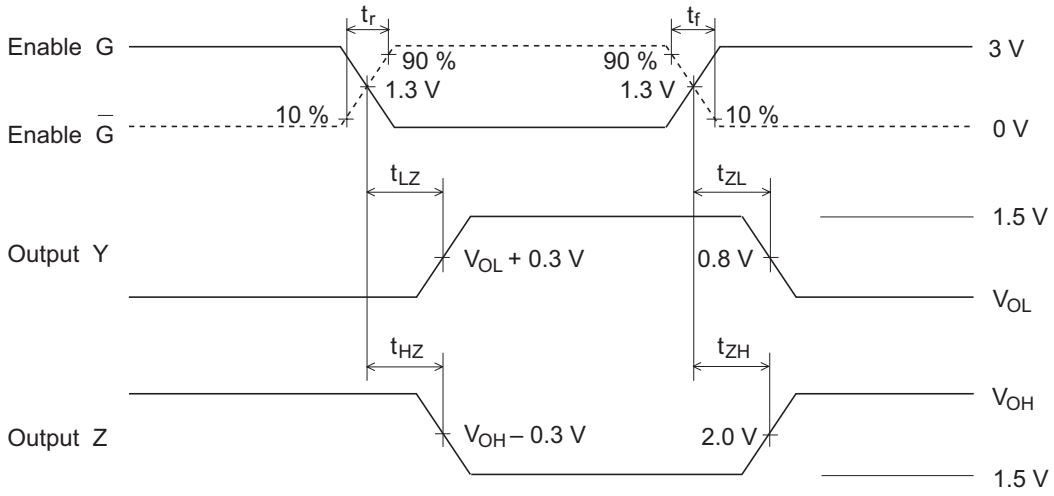
Notes: 1. $t_r \leq 6$ ns, $t_f \leq 6$ ns
2. Input waveforms: PRR = 1 MHz, duty cycle 50%

Test Circuit 2



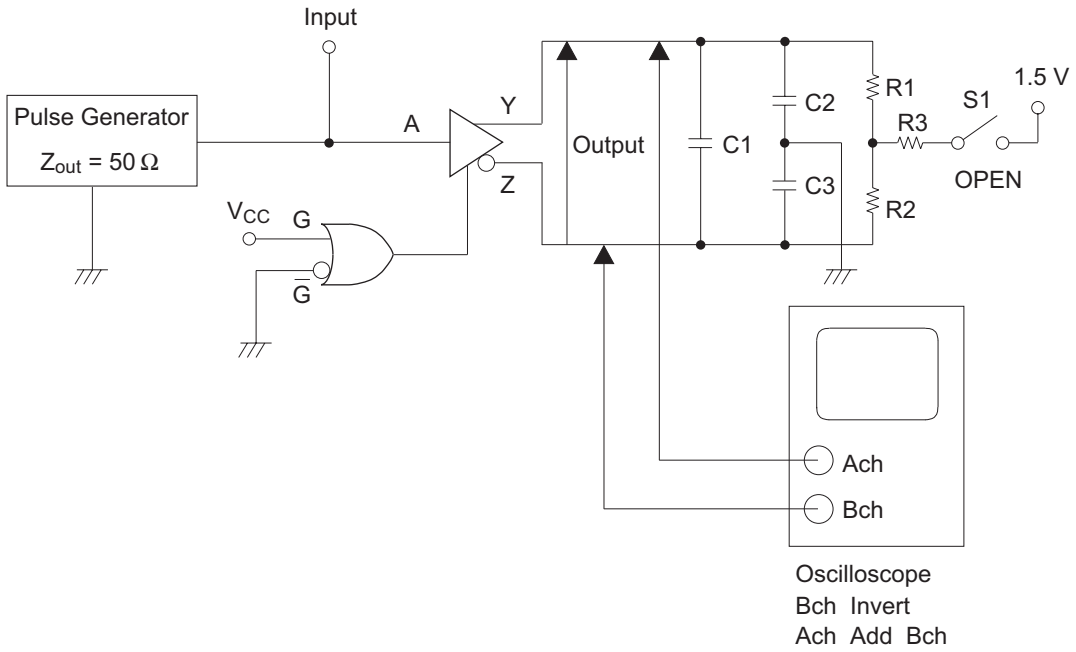
Notes: 1. $t_r \leq 6$ ns, $t_f \leq 6$ ns
2. Input waveforms: PRR = 1 MHz, duty cycle 50%

Waveforms 2



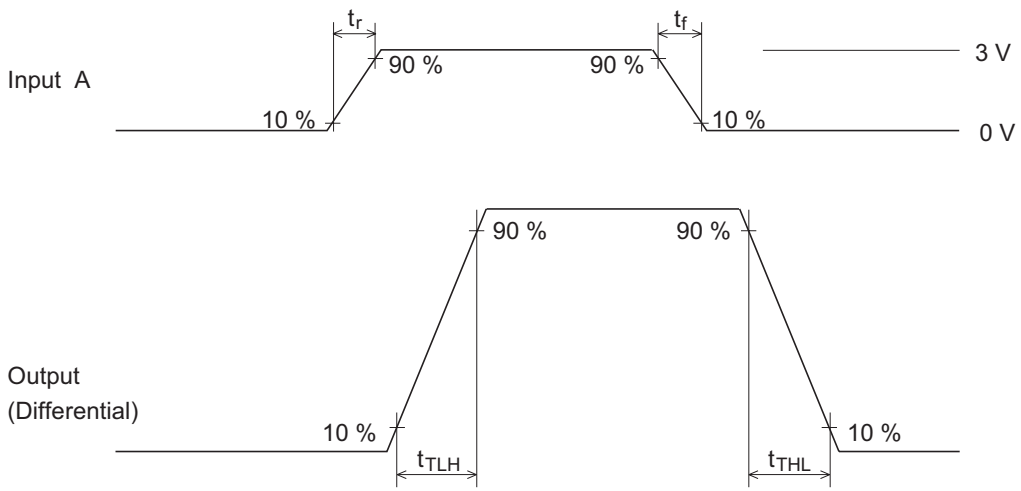
Notes: 1. $t_r \leq 6$ ns, $t_f \leq 6$ ns
2. Input waveforms: PRR = 1 MHz, duty cycle 50%

Test Circuit 3



Note: 1. C1, C2 and C3 (40 pF) include probe and jig capacitance.
R1 = R2 = 50 Ω, R3 = 500 Ω

Waveforms 3



Notes: 1. $t_r \leq 6$ ns, $t_f \leq 6$ ns
2. Input waveforms: PRR = 1 MHz, duty cycle 50%

HD26C31 Line Driver Applications

The HD26C31 is a line driver that meets the EIA RS-422A conditions, and has been designed to supply a high current for differential signals to a bus line. Its features are listed below.

- Operates on a single 5 V power supply.
- High output impedance when power is off
- Sink current and source current both 20 mA
- On-chip power up/down protection circuit

As shown by the logic diagram, the enable function is common to all four drivers, and either active-high or active-low can be selected.

The output section consists of two output stages (the Y side and Z side), each of which has the same sink current and source current capacity.

Connection of a termination resistance when the HD26C31 is used as a balanced differential type driver is shown.

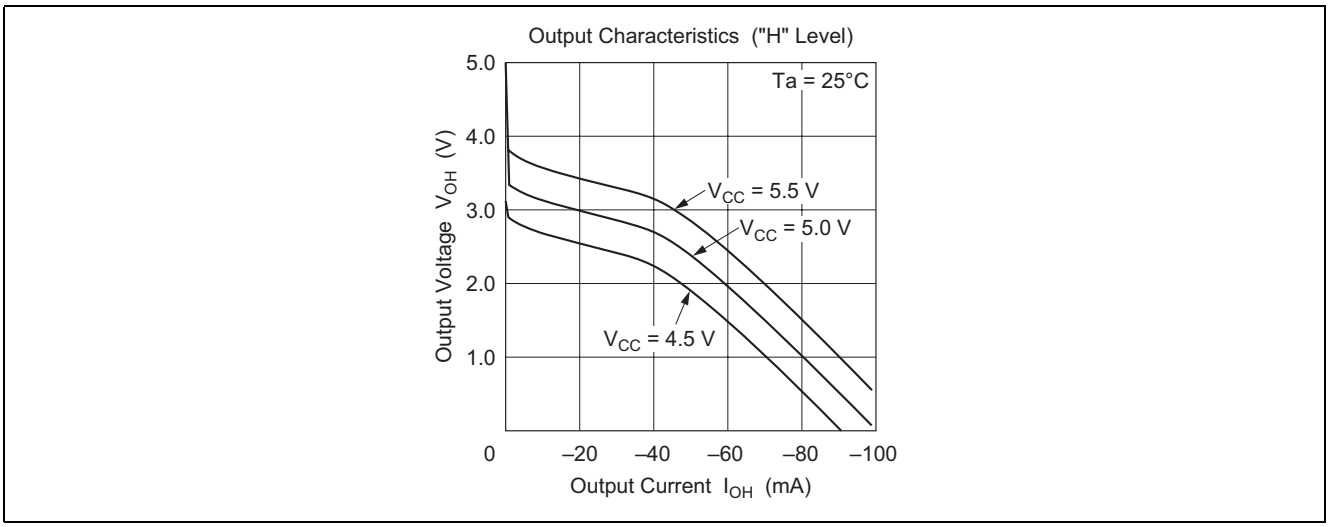


Figure 1 I_{OH} vs. V_{OH} Characteristics

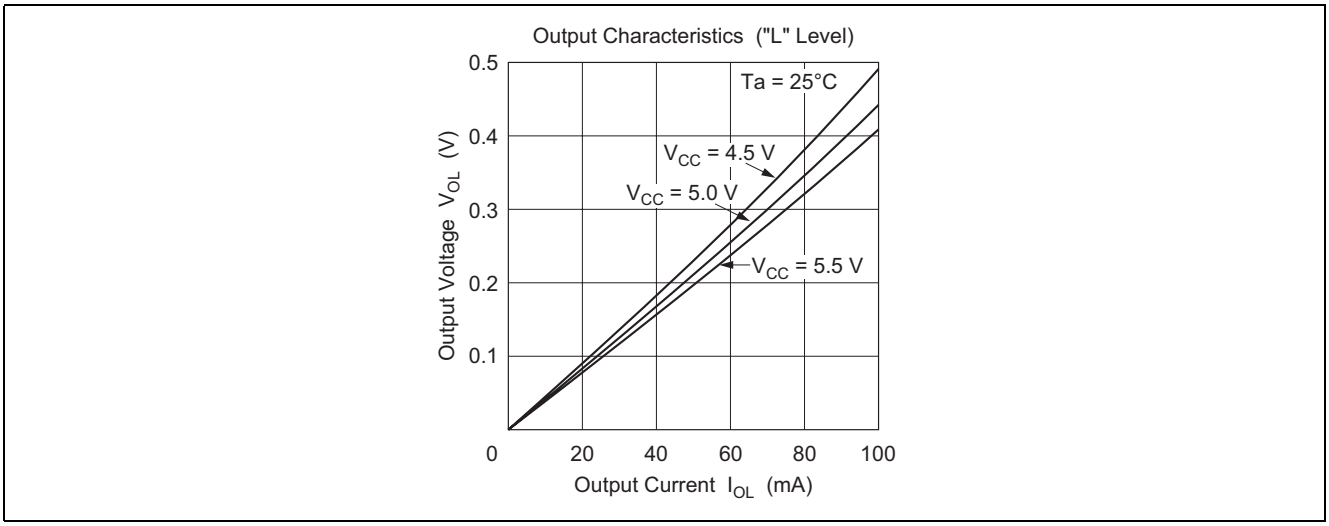


Figure 2 I_{OL} vs. V_{OL} Characteristics

When termination resistance R_T is connected between the two transmission lines, as shown in figure 3 the current path situation is that current I_{OH} on the side outputting a high level (in this case, the Y output) flows to the side outputting a low level (in this case, the Z output) via R_T, with the result that the low level rise is large.

If termination resistance R_T is dropped to GND on both transmit lines, as shown in figure 4 the current path situation is that the current that flows into the side outputting a low level (in this case, the Z output) is only the input bias current from the receiver. As this input bias current is small compared with the signal current, it has almost no effect on the differential input signal at the receiver end.

Figure 5 shows the output voltage characteristic when termination resistance R_T is varied.

Also, when used in a party line system, etc., the low level rises further due to the receiver input bias current, so that it is probably advisable to drop the termination resistance to GND.

However, the fact that it is possible to make the value of R_T equal to the characteristic impedance of the transmission line offers the advantage of being able to hold the power dissipation on the side outputting a high level to a lower level than in the above case.

Consequently, the appropriate use must be decided according to the actual operating conditions (transmission line characteristics, transmission distance, whether a party line is used, etc.).

Figure 6 shows the output characteristics when termination resistance R_T is varied.

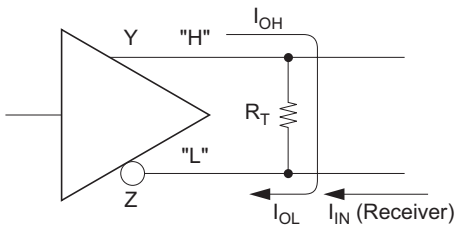


Figure 3 Example of Driver Use-1

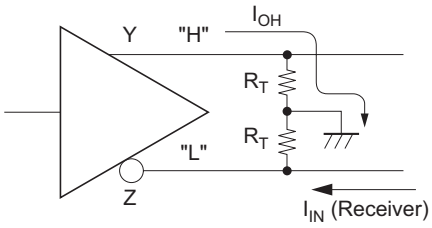


Figure 4 Example of Driver Use-2

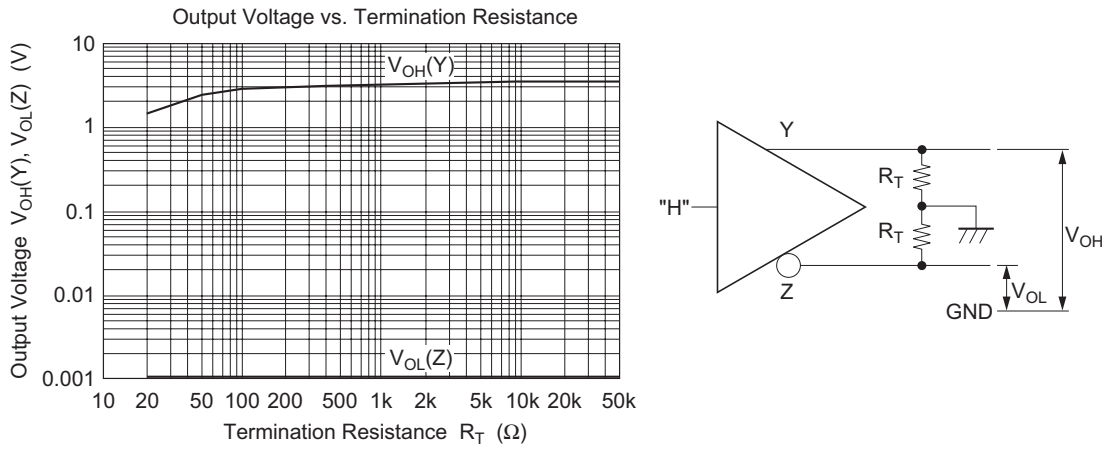


Figure 5 Termination Resistance vs. Output Voltage Characteristics

A feature of termination implemented as shown in figure 7 is that power dissipation is low when the duty of the transmitted signal is high.

However, care is required, since if R_T is sufficiently small, when the output on the pulled-up side goes high, a large current will flow and the output low level will rise.

Figure 8 shows the output characteristics when termination resistance R_T is varied.

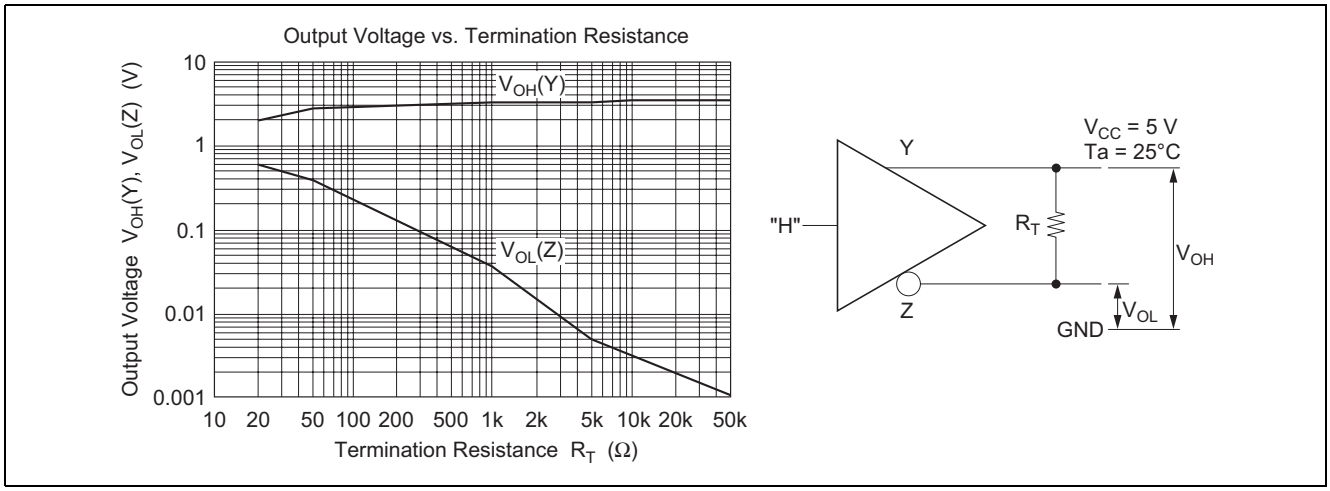


Figure 6 Termination Resistance vs. Output Voltage Characteristics

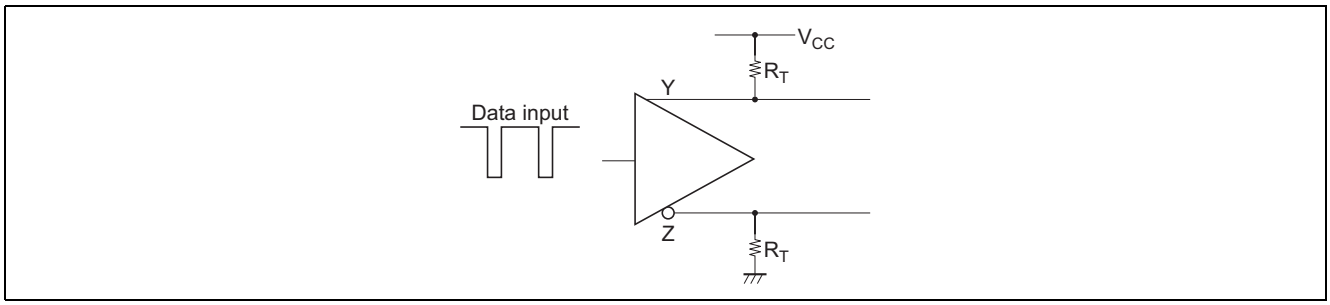


Figure 7 Example of Driver Use-3

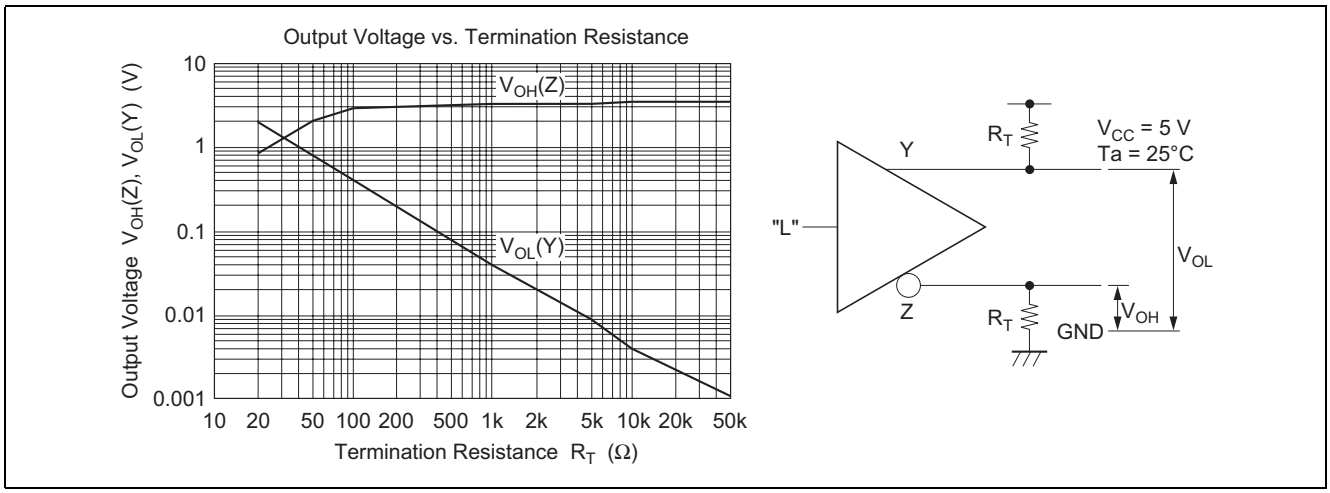
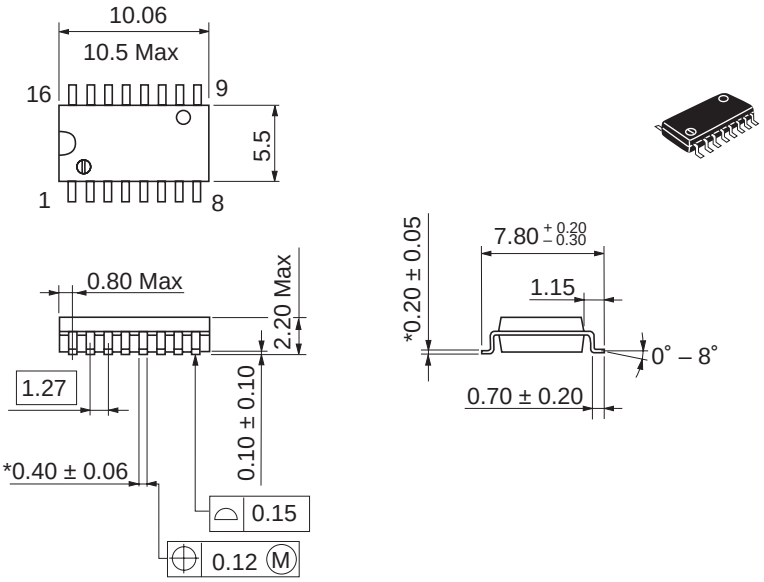


Figure 8 Termination Resistance vs. Output Voltage Characteristics

Package Dimensions

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

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Colophon .1.0