# ANADIGICS

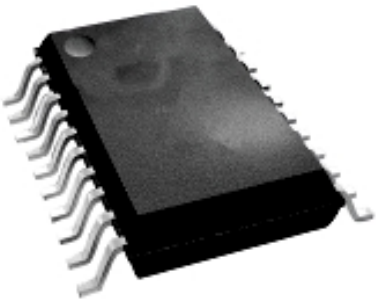
# ARA2008

## Reverse Amplifier with Step Attenuator

**ADVANCED PRODUCT INFORMATION - Rev 0.0**

### FEATURES

- Low cost integrated amplifier with step attenuator
- Attenuation Range: 0-58 dB, adjustable in 1dB increments via a 3 wire serial control
- Meets DOCSIS distortion requirements at +60dBmV output signal level
- Low distortion and low noise
- Frequency range: 5-100MHz
- 5 Volt operation
- -40 to +85 $^0$C temperature range



**20 Pin SSOP Package**

### APPLICATIONS

- MCNS/DOCSIS Compliant Cable Modems
- CATV Interactive Set-Top Box
- Telephony over Cable Systems
- OpenCable Set-Top Box
- Residential Gateway

### PRODUCT DESCRIPTION

The ARA2008 is designed to provide the reverse path amplification and output level control functions in a CATV Set-Top Box or Cable Modem. It incorporates a digitally controlled precision step attenuator that is preceded by an ultra low noise amplifier stage, and followed by an ultra-linear output driver amplifier. This device uses a balanced circuit design that exceeds the MCNS/DOCSIS requirement for harmonic performance at a +60dBmV output level while only requiring a single polarity +5V supply. Both the input and output are matched to 75 ohms with an appropriate transformer. The precision attenuator provides up to 58 dB of attenuation in 1 dB increments via a three-wire serial interface. With external passive components, this device meets IEC 1000-4-12 and ANSI/IEEE C62.41-1991 100KHz ringwave tests, as well as IEC1000-4-5 1.2/50μS surge tests. The ARA2008 is offered in a 20-pin SSOP package.

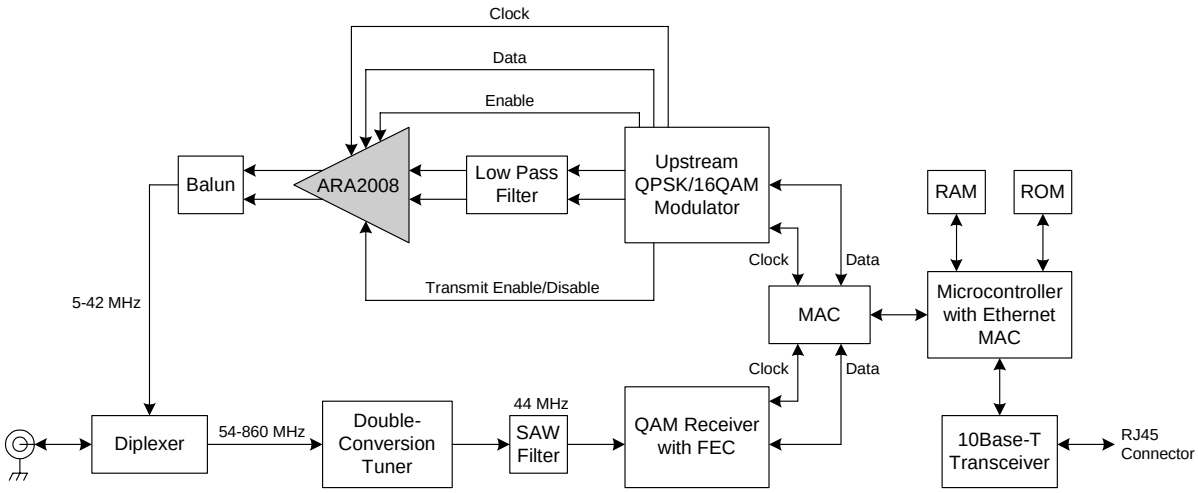



**Figure 1. Cable Modem or Set Top Box Application Diagram**

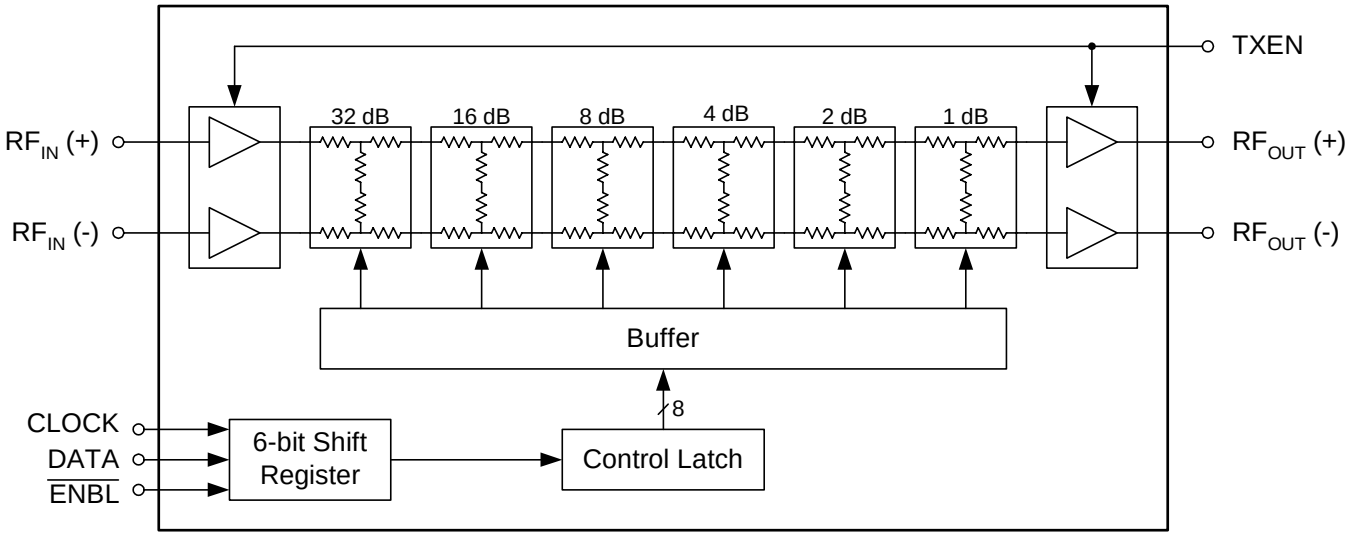



**Figure 2: Functional Block Diagram**

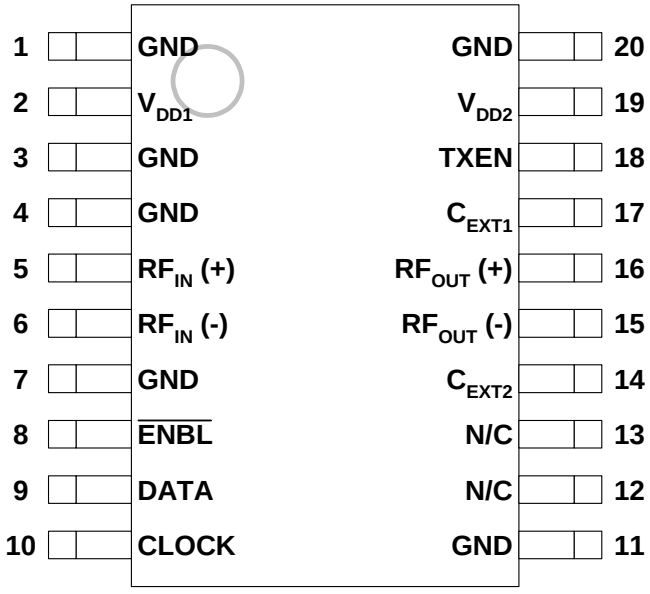



**Figure 3: Pin Out - SSOP Package**

**Table 1: Pin Description - SSOP Package**

| PIN | NAME | DESCRIPTION | PIN | NAME | DESCRIPTION |
|---|---|---|---|---|---|
| 1 | GND | Ground | 11 | GND | Ground |
| 2 | $V_{DD1}$ | Supply | 12 | N/C | No connection |
| 3 | GND | Ground | 13 | N/C | No connection |
| 4 | GND | Ground | 14 | $C_{EXT2}$ | External Capacitor |
| 5 | $RF_{IN}$ (+) | RF (+) Input | 15 | $RF_{OUT}$ (-) | RF (-) Output |
| 6 | $RF_{IN}$ (-) | RF (-) Input | 16 | $RF_{OUT}$ (+) | RF (+) Output |
| 7 | GND | Ground | 17 | $C_{EXT1}$ | External Capacitor |
| 8 | $\overline{ENBL}$ | Enable | 18 | TXEN | Transmit Enable |
| 9 | DATA | Data | 19 | $V_{DD2}$ | Supply |
| 10 | CLOCK | Clock | 20 | GND | Ground |

## ELECTRICAL CHARACTERISTICS

**Table 2: Absolute Minimum and Maximum Ratings**

| PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|
| Supply: $V_{DD}$ (pins 2, 15, 16, 19) | 0 | 9 | VDC |
| RF Power at Inputs (pins 5, 6) | - | +60 | dBmV |
| Digital Interface (pins 8, 9, 10) | -0.5 | $V_{DD}$+0.5 | V |
| Storage Temperature | -55 | +200 | $^0$C |
| Soldering Temperature | - | 260 | $^0$C |
| Soldering Time | - | 5 | Sec |

**Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.**

**Table 3: Operating Ranges**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Supply: $V_{DD}$ (pins 2, 15, 16, 19) | 4.5 | 5 | 7 | VDC |
| Digital Interface (pins 8, 9, 10) | 0 | - | $V_{DD}$ | V |
| Case Temperature | -40 | 25 | 85 | $^0$C |

**The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.**

**Table 4: DC Electrical Specifications**
**$T_A$=25°C; $V_{DD}$ = +5.0 VDC**

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| Total Supply Current (pins 2, 15, 16, 19) | -<br>- | 135<br>15 | -<br>- | mA | Tx enabled (TXEN high)<br>Tx disabled (TXEN low) |
| Total Power Consumption | -<br>- | 675<br>75 | -<br>- | mW | Tx enabled (TXEN high)<br>Tx disabled (TXEN low) |

**Table 5: Digital Interface Specifications**
**$T_A$=25°C; $V_{DD}$ = +5.0 VDC**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Logic High Input Voltage: $V_{IN,HIGH}$ | 2.0 | - | $V_{DD}$ | V |
| Logic Low Input Voltage: $V_{IN,LOW}$ | 0 | - | 0.8 | V |

**Table 6: AC Electrical Specifications**
**$T_A$=25°C; $V_{DD}$ = +5.0 VDC**

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| Gain (10 MHz) | - | 29 | - | dB | 0 dB attenuation setting |
| Gain Flatness | - | 1.5 | - | dB | 5 to 65 MHz |
| Gain Variation over Temperature | - | -0.006 | - | dB/°C | |
| Attenuation Step Size | - | 1 | - | dB | Monotonic |
| Maximum Attenuation | 58 | - | - | dB | |
| 2nd Harmonic Distortion Level (10 MHz) | - | - | -53 | dBc | +60 dBmV into 75 Ohms |
| 3rd Harmonic Distortion Level (10 MHz) | - | - | -53 | dBc | +60 dBmV into 75 Ohms |
| 3rd Order Output Intercept | 78 | - | - | dBmV | |
| 1 dB Gain Compression Point | - | 68.5 | - | dBmV | |
| Noise Figure | - | 3.0 | - | dB | Includes input balun loss |
| Output Noise Power<br>Active / No Signal / Min. Atten. Set.<br>Active / No Signal / Max. Atten. Set. | <br>-<br>- | <br>-<br>- | <br>-38.5<br>-53.8 | dBmV | Any 160 kHz bandwidth from 5 to 42 MHz |
| Isolation (45 MHz) in Tx disable mode | - | 60 | - | dB | |
| Differential Input Impedance (Tx enabled) | - | 300 | - | Ohms | |
| Input Impedance (Tx enabled) | - | 75 | - | Ohms | with transformer |
| Input Return Loss (75 Ohms) | - | -15 | - | dB | |
| Differential Output Impedance | - | 300 | - | Ohms | |
| Output Impedance | - | 75 | - | Ohms | with transformer |
| Output Return Loss (75 Ohms) | - | -15 | - | dB | |
| Output Voltage Transient<br>Tx enable / Tx disable | -<br>- | -<br>4 | 100<br>7 | mVp-p | 0 dB attenuator setting<br>24 dB attenuator setting |

## LOGIC PROGRAMMING

### Programming Instructions

The programming word is set through a 6 bit shift register via the data, clock and enable lines. The data is entered in order with the most significant bit (MSB) first and the least significant bit (LSB) last. The enable line must be low for the duration of the data entry, then set high to latch the shift register. The rising edge of the clock pulse shifts each data value into the register.

**Table 7: Programming Word**

| DATA BIT | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|
| **Value** | P5 | P4 | P3 | P2 | P1 | P0 |

**Table 8: Data Description**

| VALUE | FUNCTION (0 = on, 1 = bypass) |
|---|---|
| P5 | 32 dB Attenuator Bit |
| P4 | 16 dB Attenuator Bit |
| P3 | 8 dB Attenuator Bit |
| P2 | 4 dB Attenuator Bit |
| P1 | 2 dB Attenuator Bit |
| P0 | 1 dB Attenuator Bit |

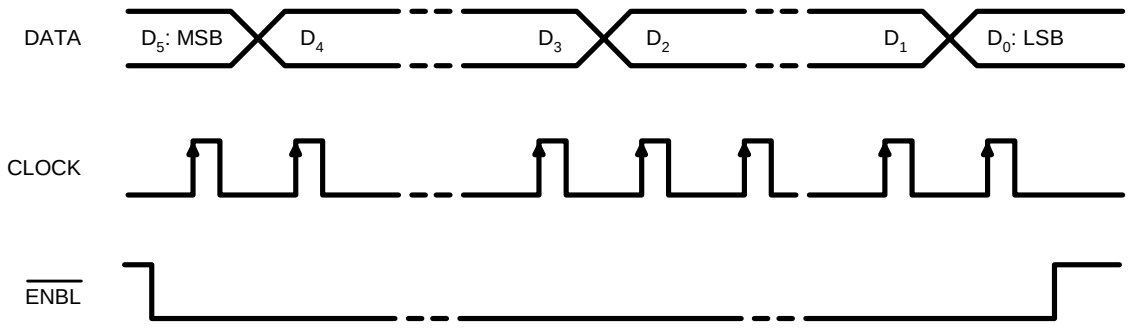



**Figure 4: Serial Data Input Timing**

## APPLICATION INFORMATION

### Output Transformer

Matching the output of the ARA2008 to a 75 Ohm load is accomplished using a 2:1 turns ratio transformer. In addition to providing an impedance transformation, this transformer provides the bias to the output amplifier stage via the center tap.

The transformer also cancels even mode distortion products and common mode signals, such as the voltage transients that occur while enabling and disabling the amplifiers. As a result, care must be taken when selecting the transformer to be used at the output. It must be capable of handling the RF and DC power requirements without saturating the core, and it must have adequate isolation and good phase and amplitude balance. It also must operate over the desired frequency and temperature range for the intended application.

### ESD Sensitivity

Electrostatic discharges can cause permanent damage to this device. Electrostatic charges accumulate on test equipment and the human body, and can discharge without detection. Although the ARA2008 has some built-in ESD protection, proper precautions and handling are strongly recommended. Refer to the ANADIGICS application note on ESD precautions.

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