

CSD18511Q5A 40V N 沟道 NexFET™ 功率 MOSFET

1 特性

- 低 $R_{DS(on)}$
- 低热阻
- 雪崩额定值
- 逻辑电平
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 5mm x 6mm 塑料封装

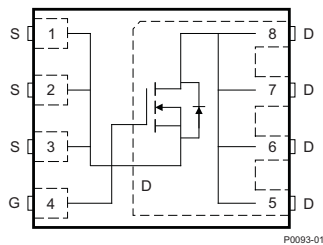
2 应用范围

- 直流 - 直流转换
- 次级侧同步整流
- 电池电机控制

3 说明

这款 40V, 1.9mΩ, SON 5mm × 6mm NexFET™ 功率 MOSFET 的设计旨在追求以最大限度降低功率转换应用中的功率损耗。

俯视图



P0093-01

产品概要

$T_A = 25^\circ\text{C}$		典型值		单位
V_{DS}	漏源电压	40		V
Q_g	栅极电荷总量 (10V)	63		nC
Q_{gd}	栅极电荷 (栅极到漏极)	11.2		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 4.5\text{V}$	2.7	mΩ
		$V_{GS} = 10\text{V}$	1.9	mΩ
$V_{GS(th)}$	阈值电压	1.8		V

订购信息⁽¹⁾

器件	数量	介质	封装	出货
CSD18511Q5A	2500	13 英寸卷带	SON 5mm × 6mm 塑料封装	卷带封装
CSD18511Q5AT	250	7 英寸卷带		

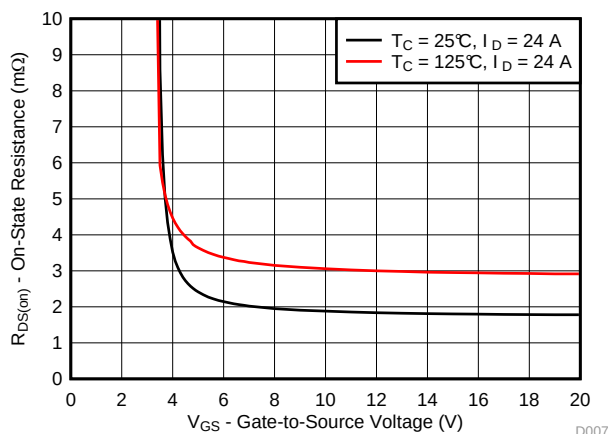
(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	40	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流 (受封装限制)	100	A
	持续漏极电流 (受芯片限制), $T_C = 25^\circ\text{C}$ 时测得	159	
	持续漏极电流 ⁽¹⁾	27	
I_{DM}	脉冲漏极电流 ⁽²⁾	400	A
P_D	功率耗散 ⁽¹⁾	3.1	W
	功率耗散, $T_C = 25^\circ\text{C}$	104	
T_J, T_{stg}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量, 单一脉冲 $I_D = 56\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	157	mJ

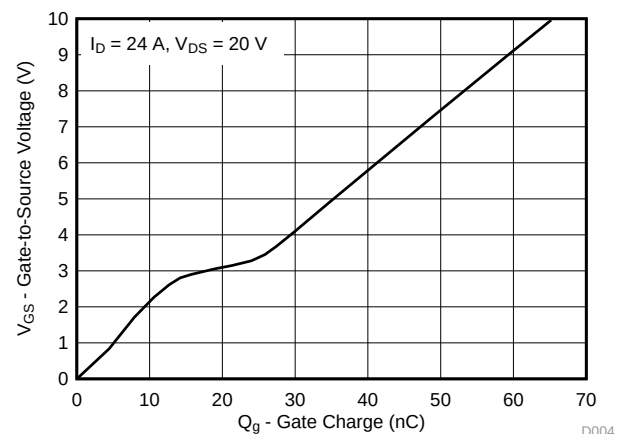
(1) $R_{\theta JA} = 42^\circ\text{C/W}$, 这是在一块厚度为 0.06 英寸 (1.52mm) 的 FR4 印刷电路板 (PCB) 上的一英寸², 2 盎司铜过渡垫片上测得的典型值。

(2) 最大 $R_{\theta JC} = 1.2^\circ\text{C/W}$, 脉冲持续时间 $\leq 100\mu\text{s}$, 占空比 $\leq 1\%$

 $R_{DS(on)}$ 与 V_{GS} 间的关系

D007

栅极电荷



D004



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4 修订历史记录

日期	修订版本	注释
2016 年 12 月	*	最初发布。

5 Specifications

5.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

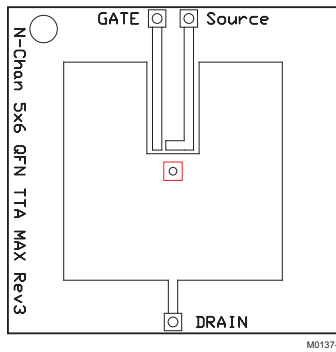
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
STATIC CHARACTERISTICS							
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _D = 250 μA	40			V	
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 32 V	1			μA	
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V	100			nA	
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.5	1.8	2.4	V	
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 4.5 V, I _D = 24 A	2.7			3.5	mΩ
		V _{GS} = 10 V, I _D = 24 A	1.9			2.3	mΩ
g _{fs}	Transconductance	V _{DS} = 20 V, I _D = 24 A	5.2			S	
DYNAMIC CHARACTERISTICS							
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz	4500			5850	pF
C _{oss}	Output Capacitance		452			588	pF
C _{rss}	Reverse Transfer Capacitance		238			309	pF
R _G	Series Gate Resistance		0.7			1.4	Ω
Q _g	Gate Charge Total (10 V)	V _{DS} = 20 V, I _D = 24 A	63			82	nC
Q _g	Gate Charge Total (4.5 V)		31			41	nC
Q _{gd}	Gate Charge Gate-to-Drain		11.2				nC
Q _{gs}	Gate Charge Gate-to-Source		13.2				nC
Q _{g(th)}	Gate Charge at V _{th}		8.2				nC
Q _{oss}	Output Charge	V _{DS} = 20 V, V _{GS} = 0 V	20				nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 20 V, V _{GS} = 10 V, I _{DS} = 24 A, R _G = 0	6				ns
t _r	Rise Time		15				ns
t _{d(off)}	Turn Off Delay Time		24				ns
t _f	Fall Time		5				ns
DIODE CHARACTERISTICS							
V _{SD}	Diode Forward Voltage	I _{DS} = 24 A, V _{GS} = 0 V	0.75			1	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 20 V, I _F = 24 A, di/dt = 300 A/μs	17				nC
t _{rr}	Reverse Recovery Time		14				ns

5.2 Thermal Information

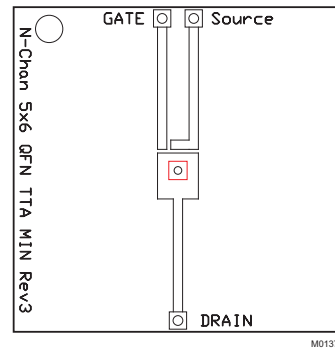
($T_A = 25^\circ\text{C}$ unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance ⁽¹⁾			1.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾			50	

- $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches $\times$ 1.5-inches (3.81-cm $\times$ 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



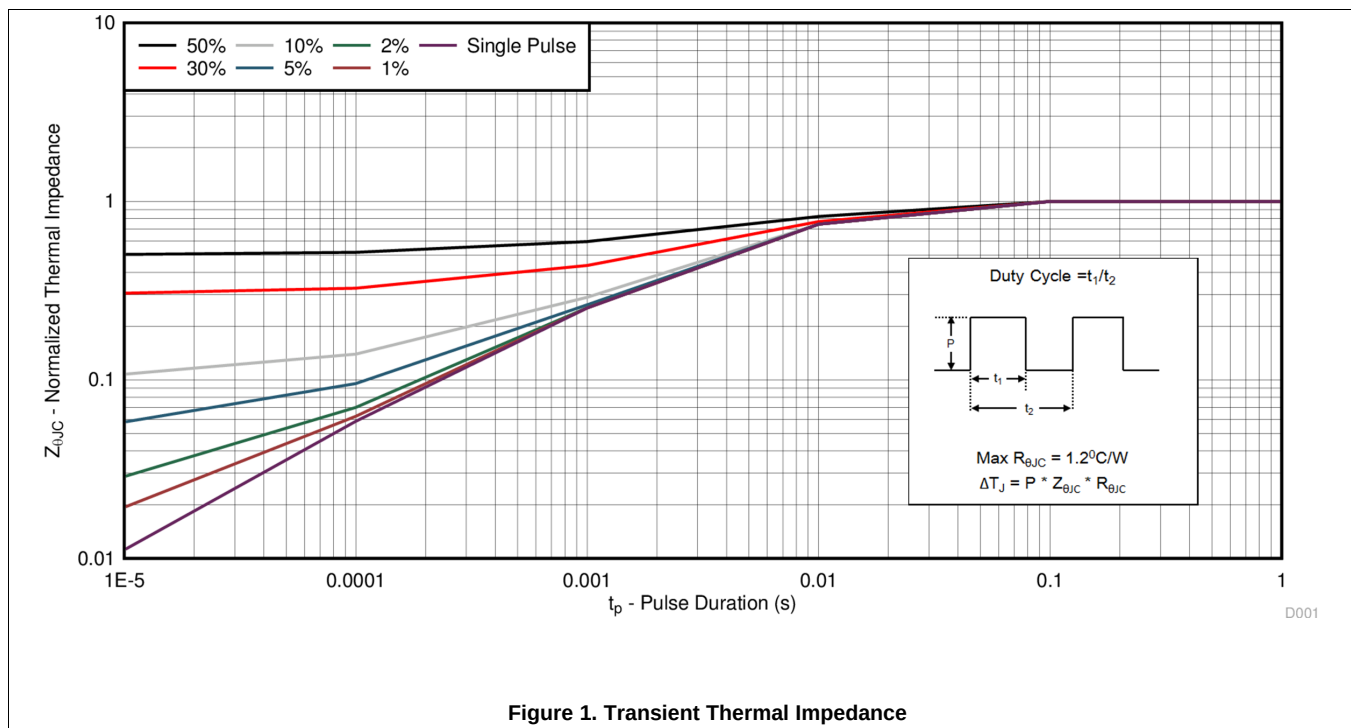
Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45-cm²) of
2-oz. (0.071-mm thick)
Cu.



Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz.
(0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$ (unless otherwise stated)



Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

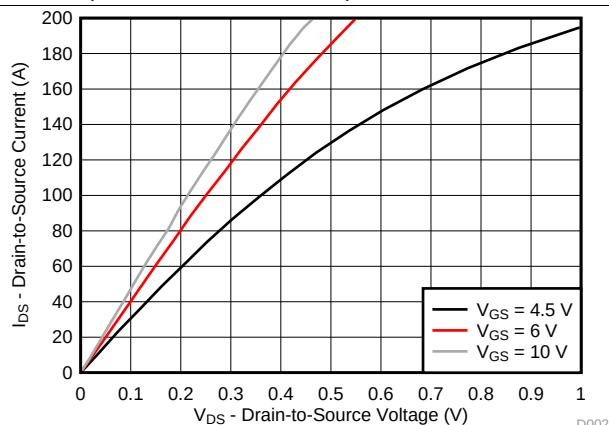


Figure 2. Saturation Characteristics

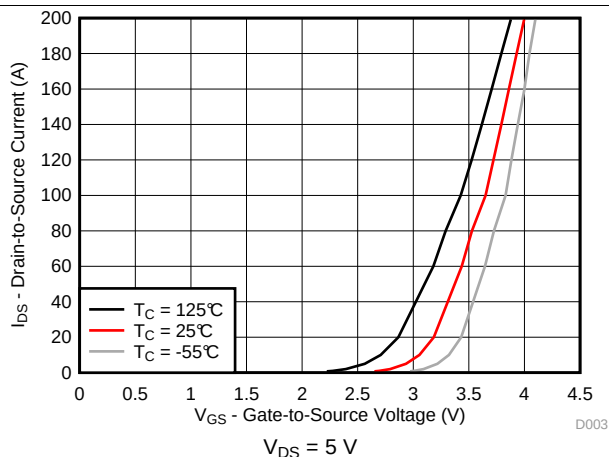


Figure 3. Transfer Characteristics

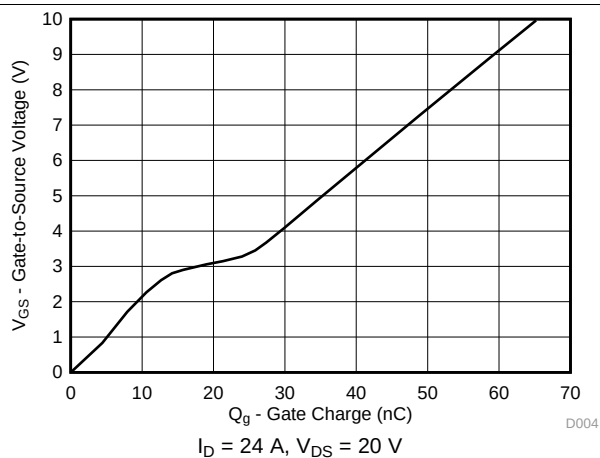


Figure 4. Gate Charge

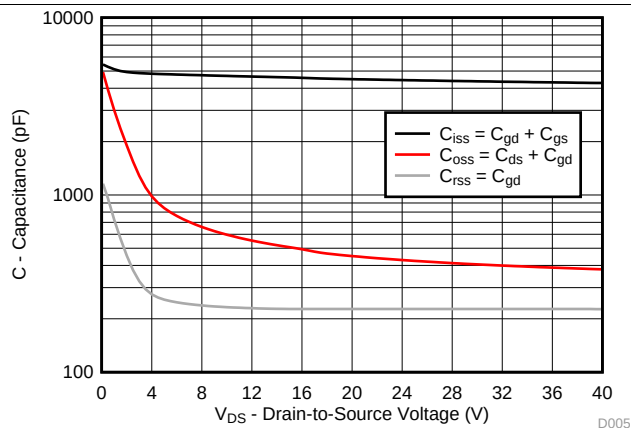


Figure 5. Capacitance

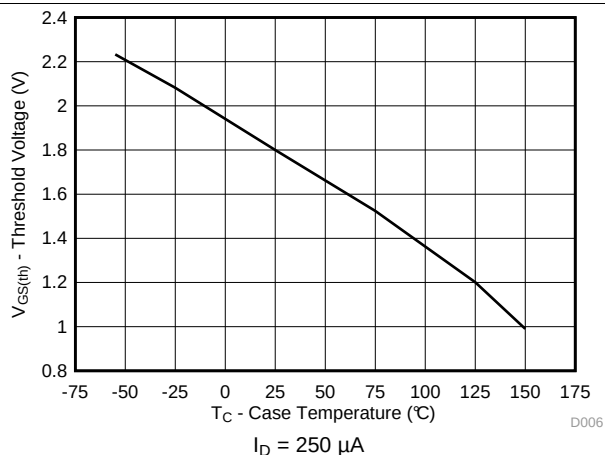


Figure 6. Threshold Voltage vs Temperature

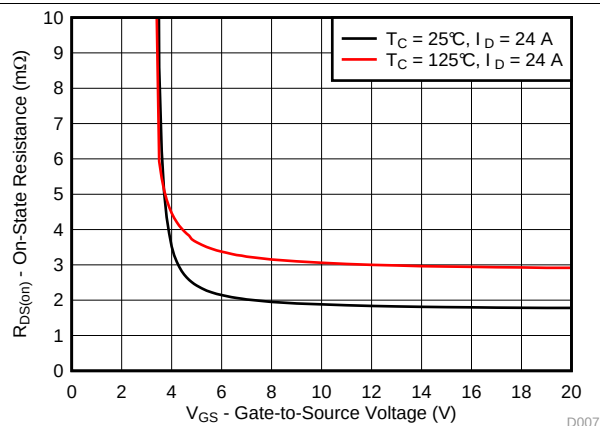


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

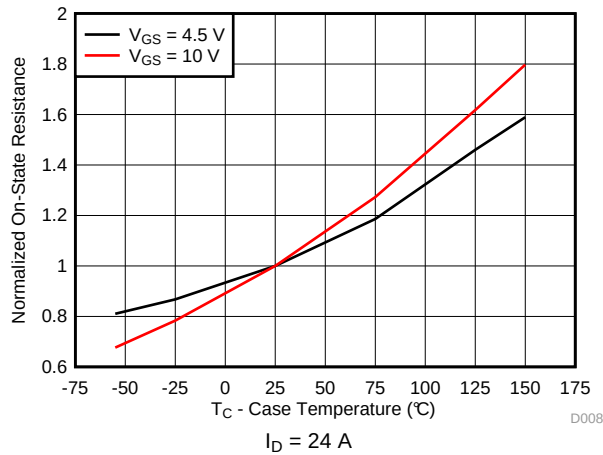


Figure 8. Normalized On-State Resistance vs Temperature

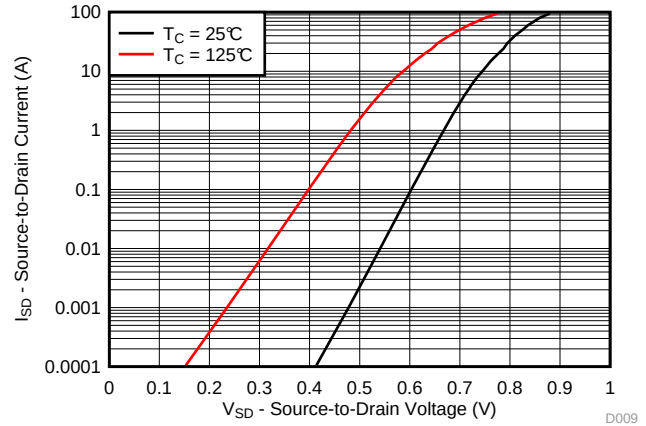


Figure 9. Typical Diode Forward Voltage

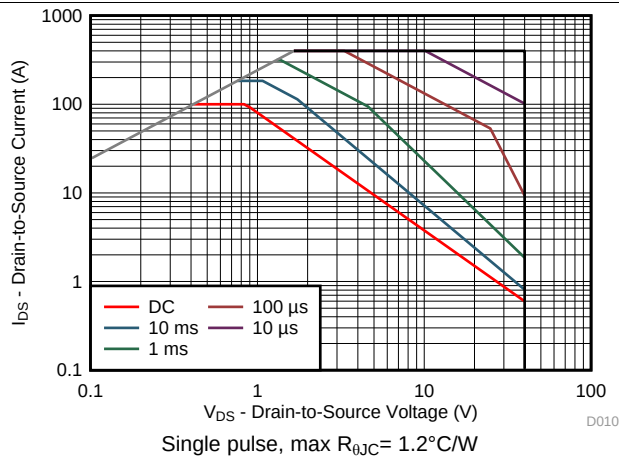


Figure 10. Maximum Safe Operating Area

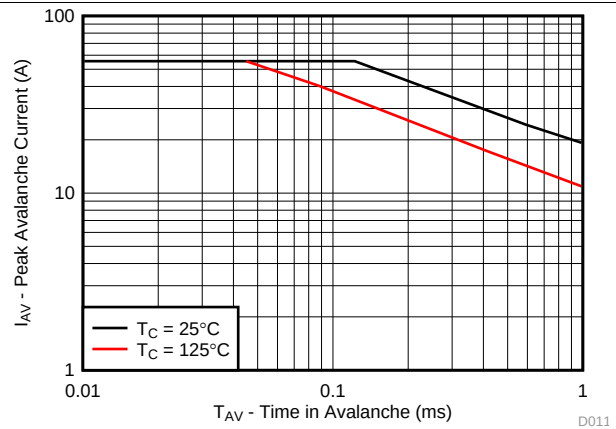


Figure 11. Single Pulse Unclamped Inductive Switching

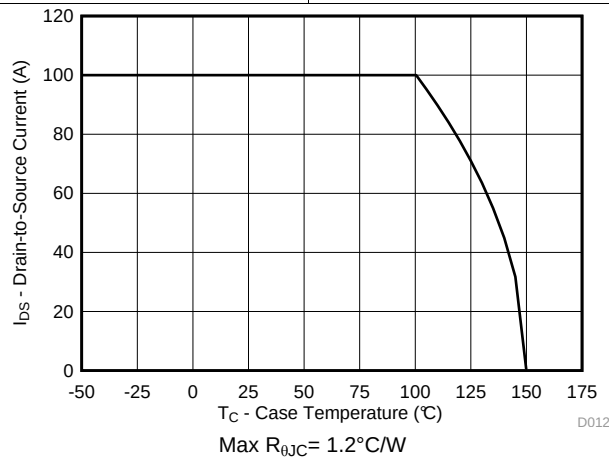


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

6.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 商标

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6.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

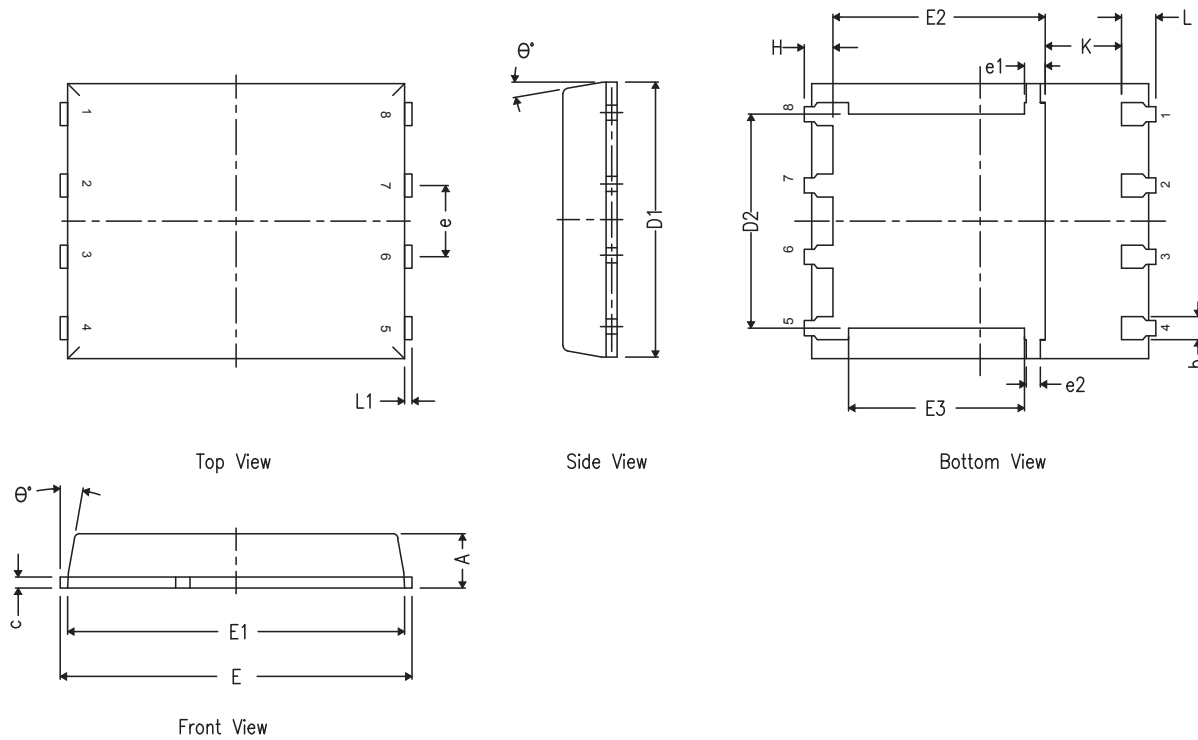
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

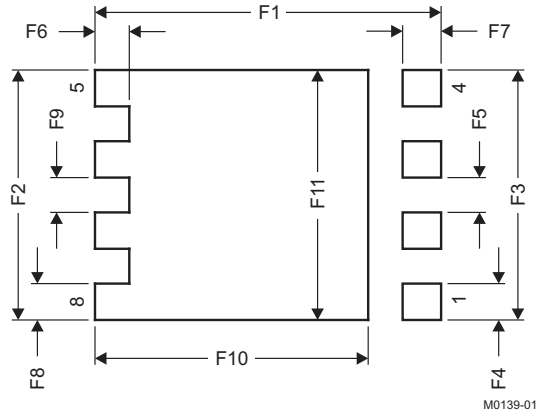
以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

7.1 Q5A 封装尺寸



DIM	毫米		
	最小值	标称值	最大值
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
E3	3.03	3.13	3.23
e	1.17	1.27	1.37
e1	0.27	0.37	0.47
e2	0.15	0.25	0.35
H	0.41	0.56	0.71
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°	-	12°

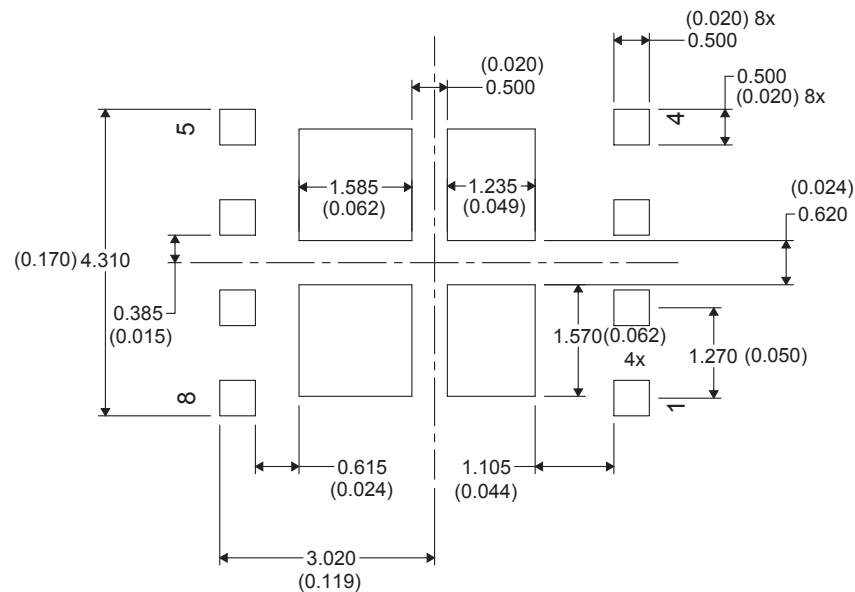
7.2 建议印刷电路板 (PCB) 布局



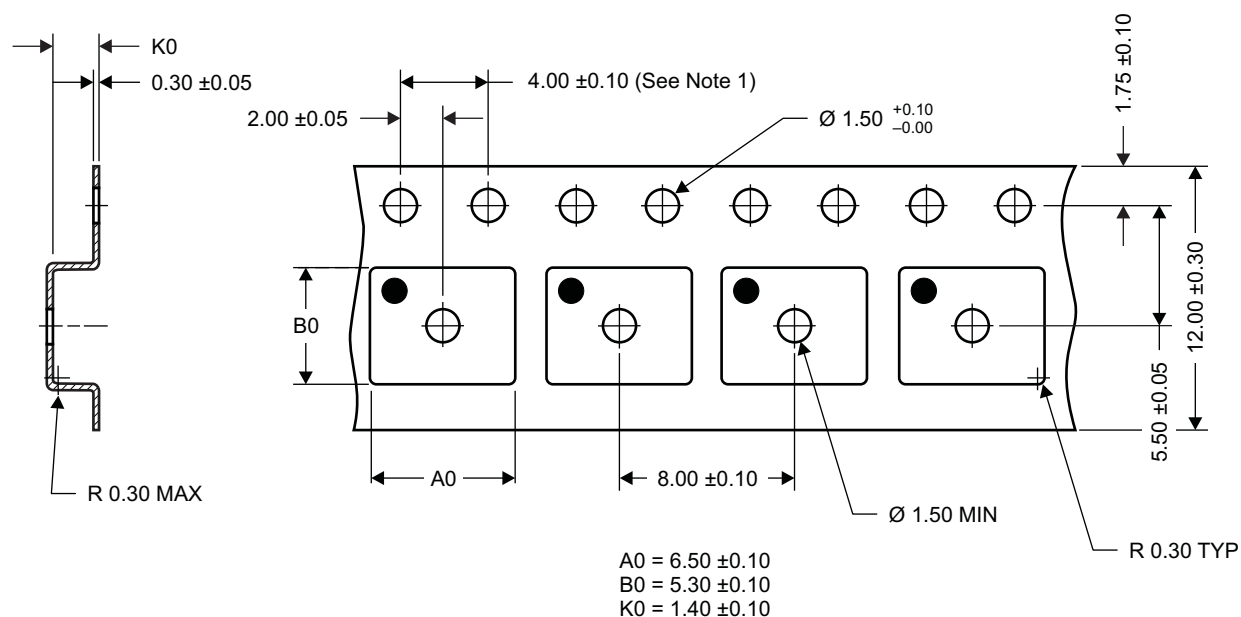
DIM	毫米		英寸	
	最小值	最大值	最小值	最大值
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线, 请参见《应用说明》[SLPA005 - 通过 PCB 布局布线技巧来减少振铃](#)。

7.3 建议模板开口



7.4 Q5A 卷带信息



M0138-01

注:

1. 10 链轮孔距累积容差 ± 0.2
2. 每 100mm 长度的翘曲不能超过 1mm, 在 250mm 长度上不累积 (Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm)
3. 材料: 黑色抗静电聚苯乙烯
4. 全部尺寸单位为 mm (除非另外注明)
5. 高于孔眼底部 0.3mm 的平面上测量得到 $A0$ 和 $B0$ 值.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18511Q5A	ACTIVE	VSONP	DQJ	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD18511	Samples
CSD18511Q5AT	ACTIVE	VSONP	DQJ	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD18511	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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