APPLICATION NOTE

AVAILABLE

AN63

8051 Microcontroller Family Compatible

64K X88C64 8192 x 8 Bit

E² Micro-Peripheral

FEATURES

- **CONCURRENT READ WRITE™**
  - **—Dual Plane Architecture**
    - **—Isolates Read/Write Functions Between Planes**
    - **—Allows Continuous Execution of Code From One Plane While Writing in the Other Plane**
- **Multiplexed Address/Data Bus**
  - **—Direct Interface to Popular 8051 Family**
- **High Performance CMOS**
  - **—Fast Access Time, 120ns**
  - **—Low Power**
    - **—60mA Active Maximum**
    - **—500μA Standby Maximum**
- **Software Data Protection**
- **Block Protect Register**
  - **—Individually Set Write Lock Out in 1K Blocks**
- **Toggle Bit Polling**
  - **—Early End of Write Detection**
- **Page Mode Write**
  - **—Allows up to 32 Bytes to be Written in One Write Cycle**
- **High Reliability**
  - **—Endurance: 100,000 Write Cycle**
  - **—Data Retention: 100 Years**

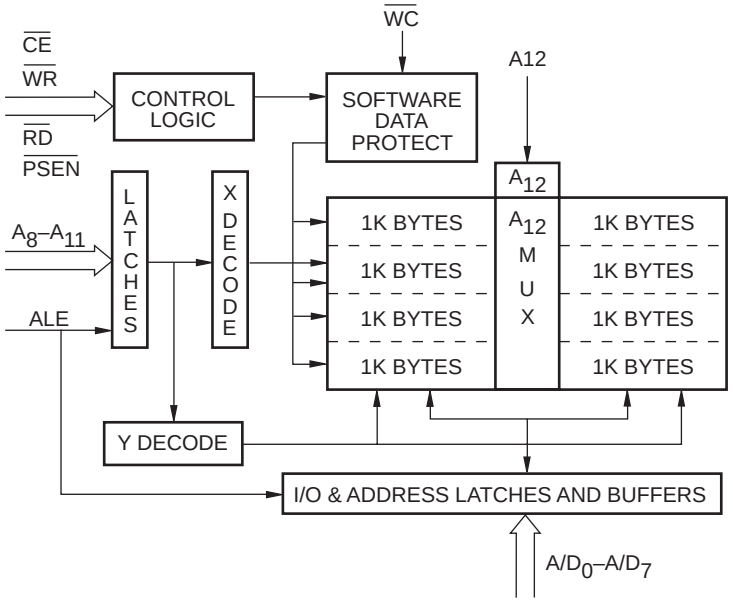
DESCRIPTION

The X88C64 is an 8K x 8 E^2PROM fabricated with advanced CMOS Textured Poly Floating Gate Technology. The X88C64 features a Multiplexed Address and Data bus allowing a direct interface to a variety of popular single-chip microcontrollers operating in expanded multiplexed mode without the need for additional interface circuitry.

The X88C64 is internally configured as two independent 4K x 8 memory arrays. This feature provides the ability to perform nonvolatile memory updates in one array and continue operation out of code stored in the other array; effectively eliminating the need for an auxiliary memory device for code storage.

To write to the X88C64, a three-byte command sequence must precede the byte(s) being written. The X88C64 also provides a second generation software data protection scheme called Block Protect. Block Protect can provide write lockout of the entire device or selected 1K blocks. There are eight 1K x 8 blocks that can be write protected individually in any combination required by the user. Block Protect, in addition to Write Control input, allows the different segments of the memory to have varying degrees of alterability in normal system operation.

FUNCTIONAL DIAGRAM



3867 FHD F02

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PIN DESCRIPTIONS

Address/Data (A/D_0–A/D_7)

Multiplexed low-order addresses and data. The Addresses flow into the device while ALE is HIGH. After ALE transitions from a HIGH to LOW the addresses are latched. Once the addresses are latched these pins input data or output data depending on $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, and $\overline{CE}$.

Addresses (A_8–A_{12})

High order addresses flow into the device when ALE is HIGH and are latched when ALE goes LOW.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH and ALE is LOW, the X88C64 is placed in the low power standby mode.

Program Store Enable ($\overline{PSEN}$)

When the X88C64 is to be used in a 8051 based system, $\overline{PSEN}$ is tied directly to the microcontroller's $\overline{PSEN}$ output.

Read ($\overline{RD}$)

When the X88C64 is to be used in a 8051 based system, $\overline{RD}$ is tied directly to the microcontroller's $\overline{RD}$ output.

Write ($\overline{WR}$)

When the X88C64 is to be used in a 8051 based system, $\overline{WR}$ is tied directly to the microcontroller's $\overline{WR}$ output.

Address Latch Enable (ALE)

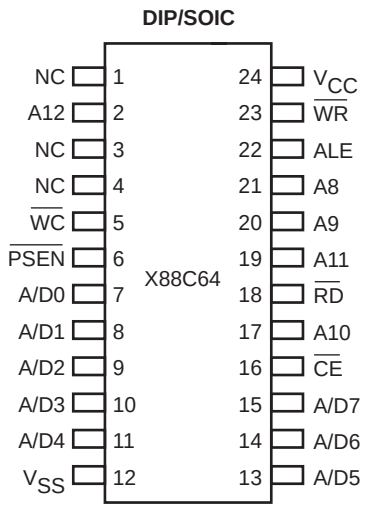
Addresses flow through the latches to address decoders when ALE is HIGH and are latched when ALE transitions from a HIGH to LOW.

Write Control ($\overline{WC}$)

The Write Control allows external circuitry to abort a page load cycle once it has been initiated. This input is useful in applications in which a power failure or processor RESET could interrupt a page load cycle. In this case, the microcontroller might drive all signals HIGH, causing bad data to be latched into the E^2PROM. If the Write Control input is driven HIGH (before t_{BLC} Max) after Write ($\overline{WR}$) goes HIGH, the write cycle will be aborted.

When $\overline{WC}$ is LOW (tied to V_{SS}) the X88C64 will be enabled to perform write operations. When $\overline{WC}$ is HIGH normal read operations may be performed, but all attempts to write to the device will be disabled.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
ALE	Address Latch Enable
A/D_0–A/D_7	Address Inputs/Data I/O
A_8–A_{12}	Address Inputs
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
$\overline{PSEN}$	Program Store Enable Input
$\overline{CE}$	Chip Enable
$\overline{WC}$	Write Control
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

3867 PGM T01.1

PRINCIPLES OF OPERATION

The X88C64 is a highly integrated peripheral device for a wide variety of single-chip microcontrollers. The X88C64 provides 8K bytes of E²PROM which can be used either for Program Storage, Data Storage, or a combination of both in systems based upon Harvard (80XX) architectures. The X88C64 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the Address/Data bus to provide a “Seamless” interface.

The interface inputs on the X88C64 are configured such that it is possible to directly connect them to the proper interface signals of the appropriate single-chip microcontroller. In the Harvard type system, the reading of data from the chip is controlled either by the $\overline{PSEN}$ or the $\overline{RD}$ signal, which essentially maps the X88C64 into both the Program and the Data Memory address map.

The X88C64 is internally organized as two independent planes of 4K bytes of memory with the A_{12} input selecting which of the two planes of memory are to be accessed. While the processor is executing code out of one plane, write operations can take place in the other plane, allowing the processor to continue execution of code out of the X88C64 during a byte or page write to the device.

The X88C64 also features an advanced implementation of the Software Data Protection scheme, called Block Protect, which allows the device to be broken into 8 independent sections of 1K bytes. Each of these sections can be independently enabled for write operations; thereby allowing certain sections of the device to be secured so that updates can only occur in a controlled environment (e.g. in an automotive application, only at an authorized service center). The desired set-up configuration is stored in a nonvolatile register, ensuring the configuration data will be maintained after the device is powered down.

The X88C64 also features a Write Control input ($\overline{WC}$), which serves as an external control over the completion of a previously initiated page load cycle.

The X88C64 also features the industry standard E²PROM characteristics such as byte or page mode write and Toggle Bit Polling.

DEVICE OPERATION

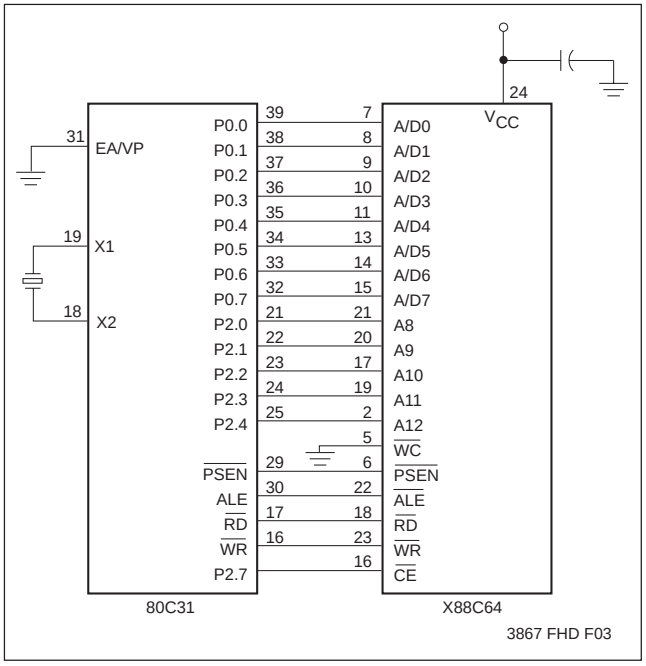
MODES

Mixed Program/Data Memory

By properly assigning the address spaces, a single X88C64 can be used as both the Program and Data Memory. This would be accomplished by connecting all of the 8051 control outputs to the corresponding inputs of the X88C64.

In this configuration, one plane of memory could be dedicated to Program Storage and the other plane dedicated to Data Storage. The Data Storage can be fully protected by enabling block protect write lockout.

TYPICAL APPLICATION



Program Memory Mode

This mode of operation is read-only. The $\overline{PSEN}$ and $\overline{ALE}$ inputs of the X88C64 are tied directly to the $\overline{PSEN}$ and ALE outputs of the microcontroller. The $\overline{RD}$ and $\overline{WR}$ inputs are tied HIGH.

When ALE is HIGH, the A/D_0–A/D_7 and A_8–A_{12} addresses flow into the device. The addresses, both low and high order, are latched when ALE transitions LOW (V_{IL}). $\overline{PSEN}$ will then go LOW and after t_{PLDV}, valid data is presented on the A/D_0–A/D_7 pins. $\overline{CE}$ must be LOW during the entire operation.

Data Memory Mode

This mode of operation allows both read and write functions. The $\overline{PSEN}$ input is tied to V_{IH} or to V_{CC} through a pull-up resistor. The ALE, $\overline{RD}$, and $\overline{WR}$ inputs are tied directly to the microcontroller's ALE, $\overline{RD}$, and $\overline{WR}$ outputs.

Read

This operation is quite similar to the Program Memory read. A HIGH to LOW transition on ALE latches the addresses and the data will be output on the AD pins after $\overline{RD}$ goes LOW (t_{RLDV}).

Write

A write is performed by latching the addresses on the falling edge of ALE. Then $\overline{WR}$ is strobed LOW followed by valid data being presented at the A/D_0–A/D_7 pins. The data will be latched into the X88C64 on the rising edge of $\overline{WR}$. To write to the X88C64, a three-byte command sequence must precede the byte(s) being written. (See Software Data Protection.)

MODE SELECTION

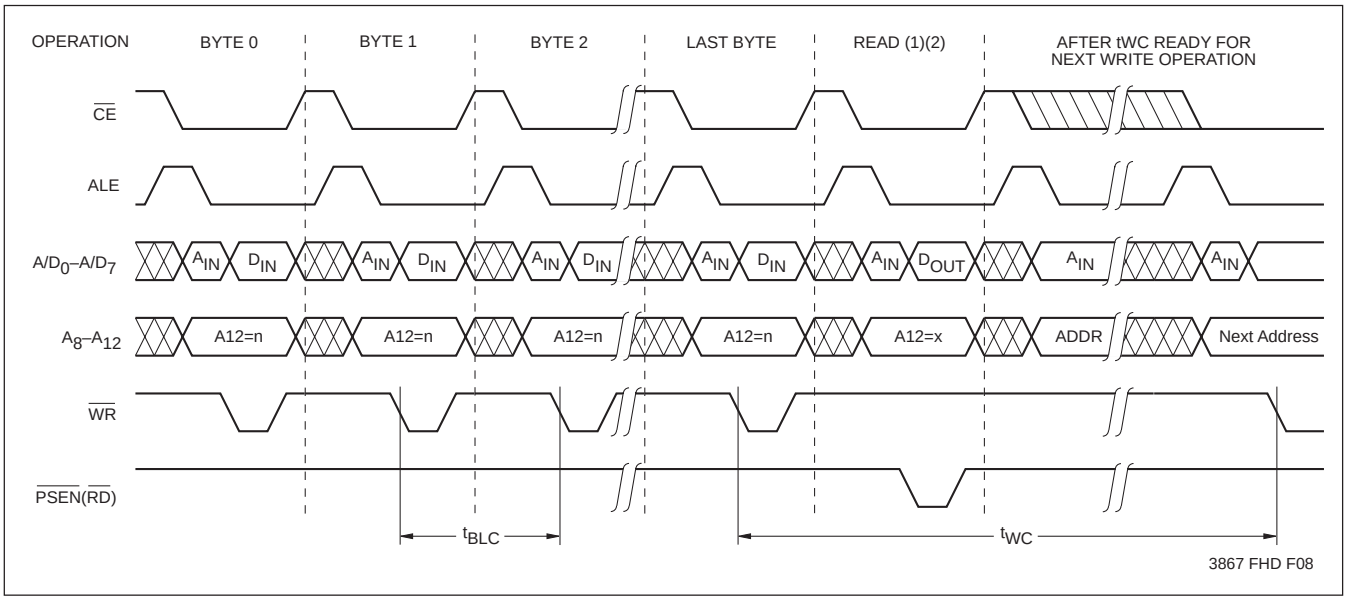
$\overline{CE}$	$\overline{PSEN}$	$\overline{RD}$	$\overline{WR}$	Mode	I/O	Power
V_{CC}	X	X	X	Standby	High Z	Standby (CMOS)
HIGH	X	X	X	Standby	High Z	Standby (TTL)
LOW	LOW	HIGH	HIGH	Program Fetch	D_{OUT}	Active
LOW	HIGH	LOW	HIGH	Data Read	D_{OUT}	Active
LOW	HIGH	HIGH	↓	Write	D_{IN}	Active

3867 PGM T02.2

PAGE WRITE OPERATION

Regardless of the microcontroller employed, the X88C64 supports page mode write operations. This allows the microcontroller to write from one to thirty-two bytes of data to the X88C64. Each individual write within a page write operation must conform to the byte write timing requirements. The falling edge of $\overline{WR}$ starts a timer delaying the internal programming cycle 100µs. Therefore, each successive write operation must begin within 100µs of the last byte written. The following waveforms illustrate the sequence and timing requirements.

Page Write Timing Sequence for $\overline{WR}$ Controlled Operation



Notes: (1) For each successive write within a page write cycle A_5–A_{12} must be the same.

(2) Although it is not illustrated, the microcontroller may interleave read operations between the individual byte writes within the page write operation. Two responses are possible:

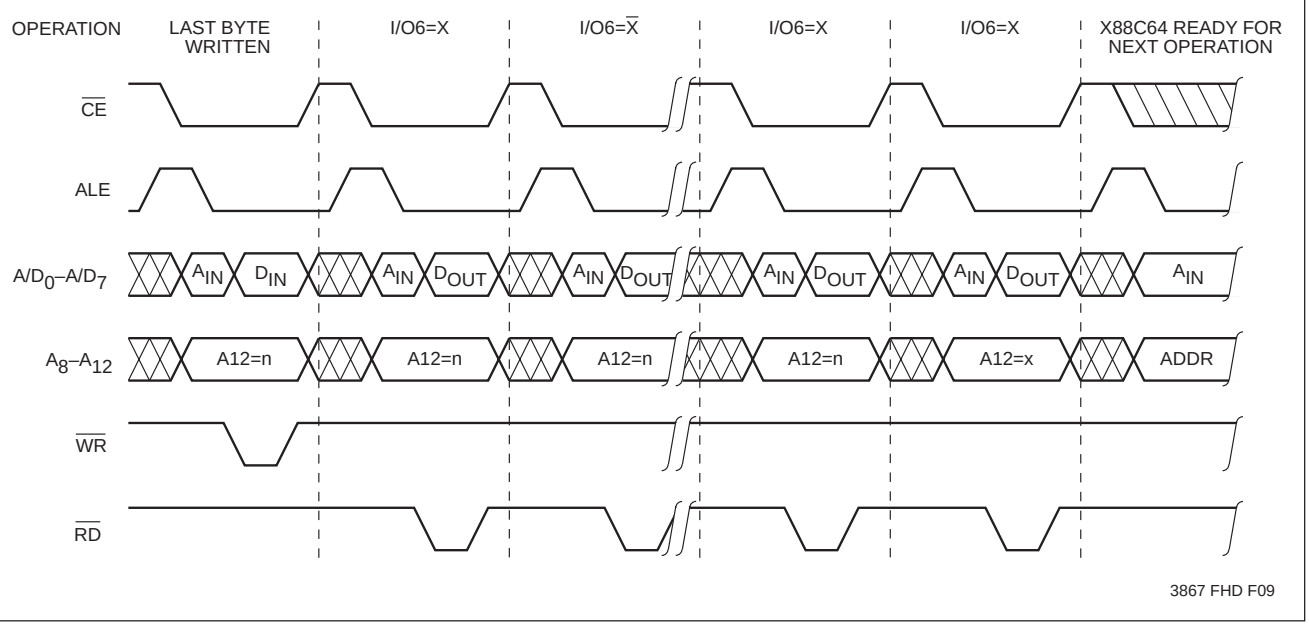
a. Reading from the same plane being written (A_{12} of Read = A_{12} of Write) is effectively a Toggle Bit Polling operation.

b. Reading from the opposite plane being written (A_{12} of Read ≠ A_{12} of Write) true data will be returned, facilitating the use of a single memory component as both program and data storage.

TOGGLE BIT POLLING

Because the X88C64 typical nonvolatile write cycle time is less than the specified 5ms, Toggle Bit Polling has been provided to determine the early completion of write. During the internal programming cycle I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete, the toggling will cease and the device will be accessible for additional read or write operations. Due to the dual plane architecture, reads for polling must occur in the plane that was written; that is, the state of A_{12} during a write must match the state of A_{12} during Toggle Bit Polling.

Toggle Bit Polling $\overline{RD}/\overline{WR}$ Control



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

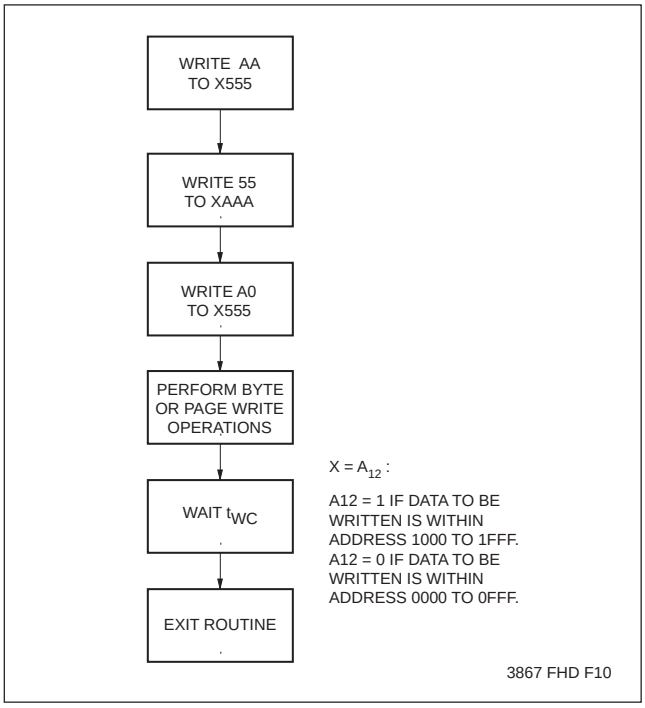
DATA PROTECTION

The X88C64 provides two levels of data protection through software control. There is a global software data protection feature similar to the industry standard for E²PROMs and a new Block Protect write lockout protection providing a secondary level of data security.

SOFTWARE DATA PROTECTION

Software Data Protection (SDP) is employed to protect the entire array against inadvertent writes. To write to the X88C64, a three-byte command sequence must precede the byte(s) being written. All write operations, both the command sequence and any data write operations, must conform to the page write timing requirements.

Writing with SDP

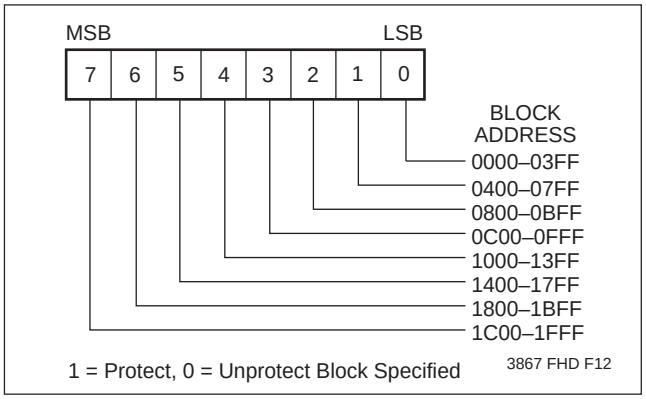


Block Protect Write Lockout

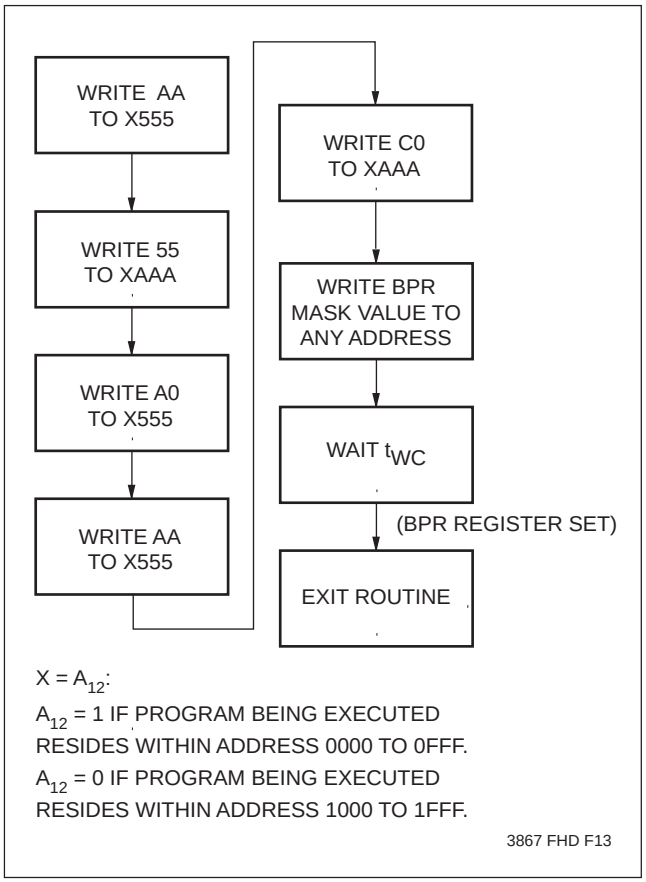
The X88C64 provides a secondary level of data security referred to as Block Protect write lockout. This is accessed through an extension of the SDP command sequence. Block Protect allows the user to lockout writes to any 1K x 8 blocks of memory. Unlike SDP which prevents inadvertent writes, but still allows easy system access to writing the memory, Block Protect will lockout all attempts unless it is specifically disabled by the host. This could be used to set a higher level of protection in a system where a portion of the memory is used for Program Storage and another portion is used as Data Storage.

Setting write lockout is accomplished by writing a five-byte command sequence, opening access to the Block Protect Register (BPR). After the fifth byte is written, the user writes to the BPR, selecting which blocks to protect or unprotect. All write operations, both the command sequence and writing the data to the BPR, must conform to the page write timing requirements.

Block Protect Register Format



Setting BPR Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3867 PGM T03.1

Supply Voltage	Limits
X88C64	5V ±10%

3867 PGM T04.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active)		60	mA	$\overline{CE}$ = $\overline{RD}$ = V_{IL}, All I/O's = Open,Other Inputs = V_{CC}
$I_{SB1(CMOS)}$	V_{CC} Current (Standby)		500	µA	$\overline{CE}$ = V_{CC} – 0.3V, All I/O's = Open,Other Inputs = V_{CC} – 0.3V, ALE = V_{IL}
$I_{SB2(TTL)}$	V_{CC} Current (Standby)		6	mA	$\overline{CE}$ = V_{IH}, All I/O's = Open, Other Inputs = V_{IH}, ALE = V_{IL}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{RD}$ = V_{IH} = $\overline{PSEN}$
V_{IL}(3)	Input LOW Voltage	–1	0.8	V	
V_{IH}(3)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400 µA

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance	6	pF	V_{IN} = 0V

3867 PGM T06

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-Up to Read	1	ms
t_{PUW}(4)	Power-Up to Write	5	ms

3867 PGM T07

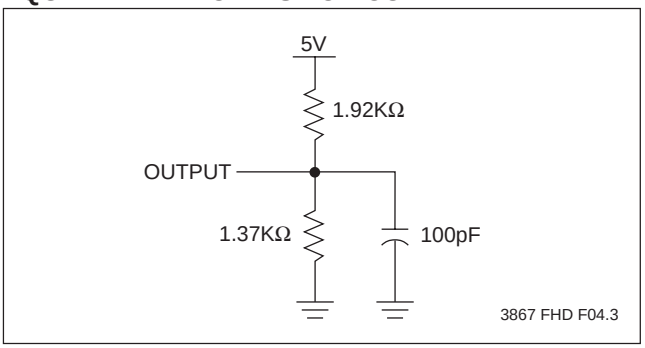
Notes: (3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3867 PGM T08.1

EQUIVALENT A.C. TEST CIRCUIT



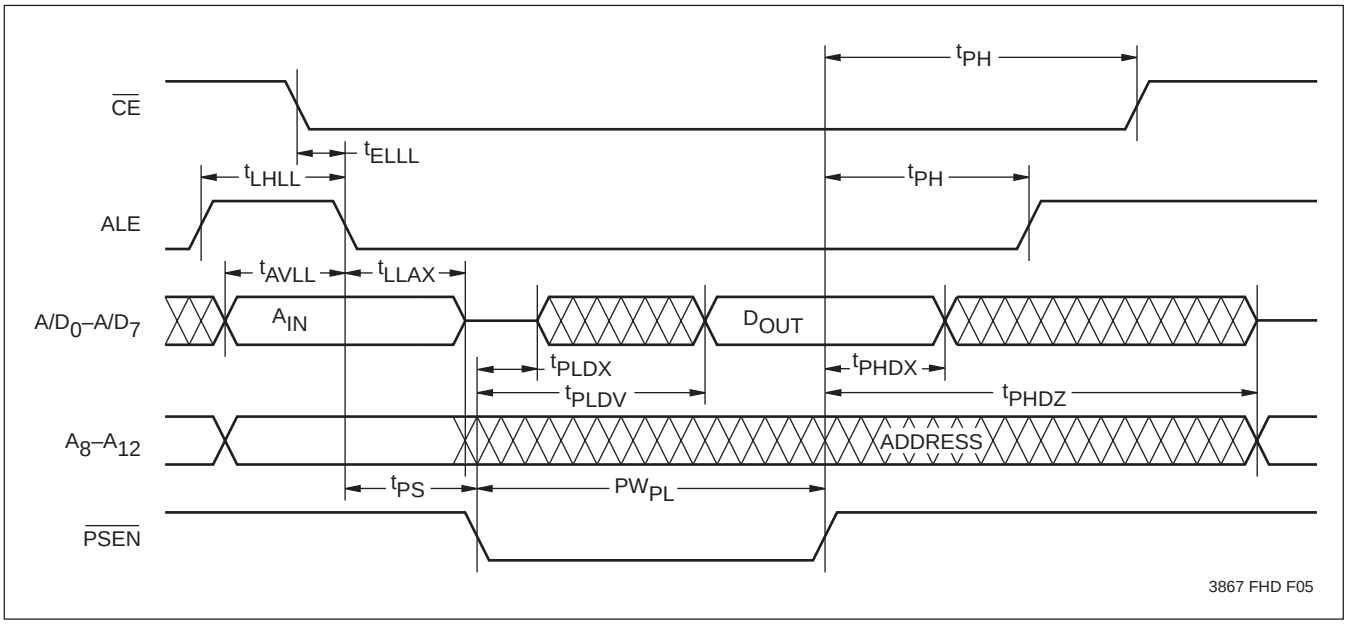
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

$\overline{\text{PSEN}}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{PLDV}	$\overline{\text{PSEN}}$ Read Access Time		120	ns
t_{PHDX}	Data Hold Time	0		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
PW_{PL}	$\overline{\text{PSEN}}$ Pulse Width	150		ns
t_{PS}	$\overline{\text{PSEN}}$ Setup Time	30		ns
t_{PH}	$\overline{\text{PSEN}}$ Hold Time	20		ns
t_{PHDZ} (5)	$\overline{\text{PSEN}}$ Disable to Output in High Z		50	ns
t_{PLDX} (5)	$\overline{\text{PSEN}}$ to Output in Low Z	10		ns

3867 PGM T09

$\overline{\text{PSEN}}$ Controlled Read Timing Diagram



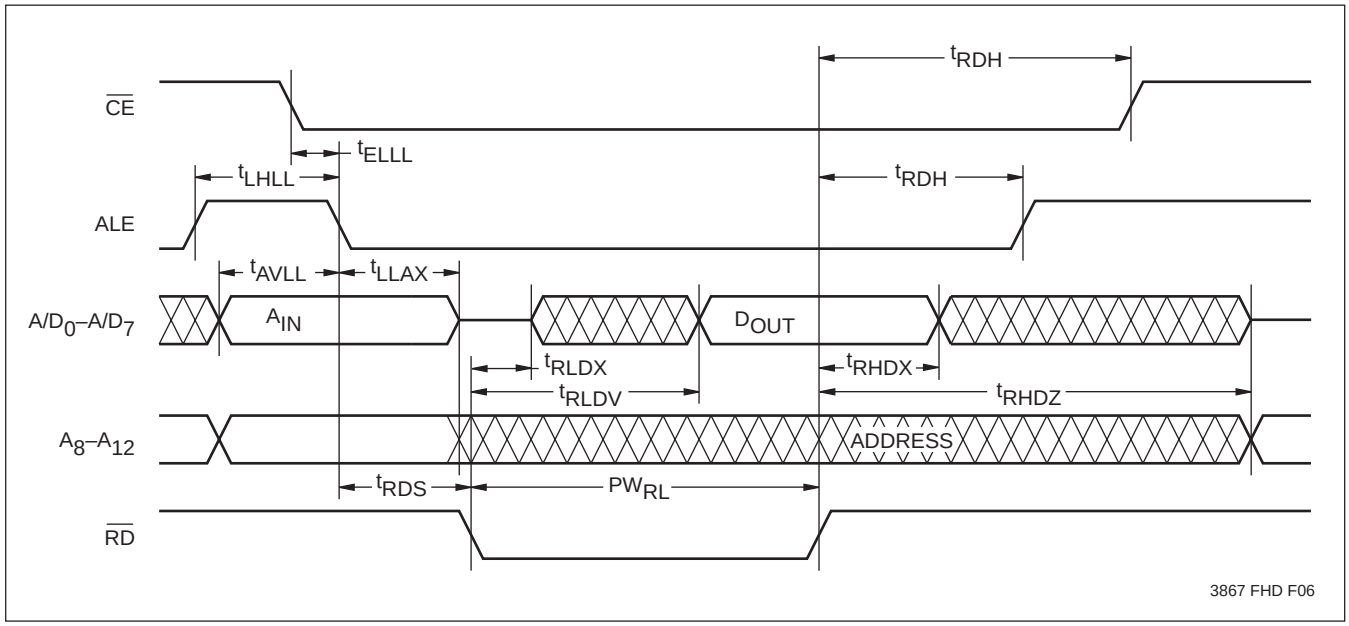
Note: (5) This parameter is periodically sampled and not 100% tested.

$\overline{RD}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{RLDV}	$\overline{RD}$ Read Access Time		120	ns
t_{RHDX}	Data Hold Time	0		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
PW_{RL}	$\overline{RD}$ Pulse Width	150		ns
t_{RDS}	$\overline{RD}$ Setup Time	30		ns
t_{RDH}	$\overline{RD}$ Hold Time	20		ns
t_{RHDZ} (6)	$\overline{RD}$ Disable to Output in High Z		50	ns
t_{RLDX} (6)	$\overline{RD}$ to Output in Low Z	0		ns

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$\overline{RD}$ Controlled Read Timing Diagram



3867 FHD F06

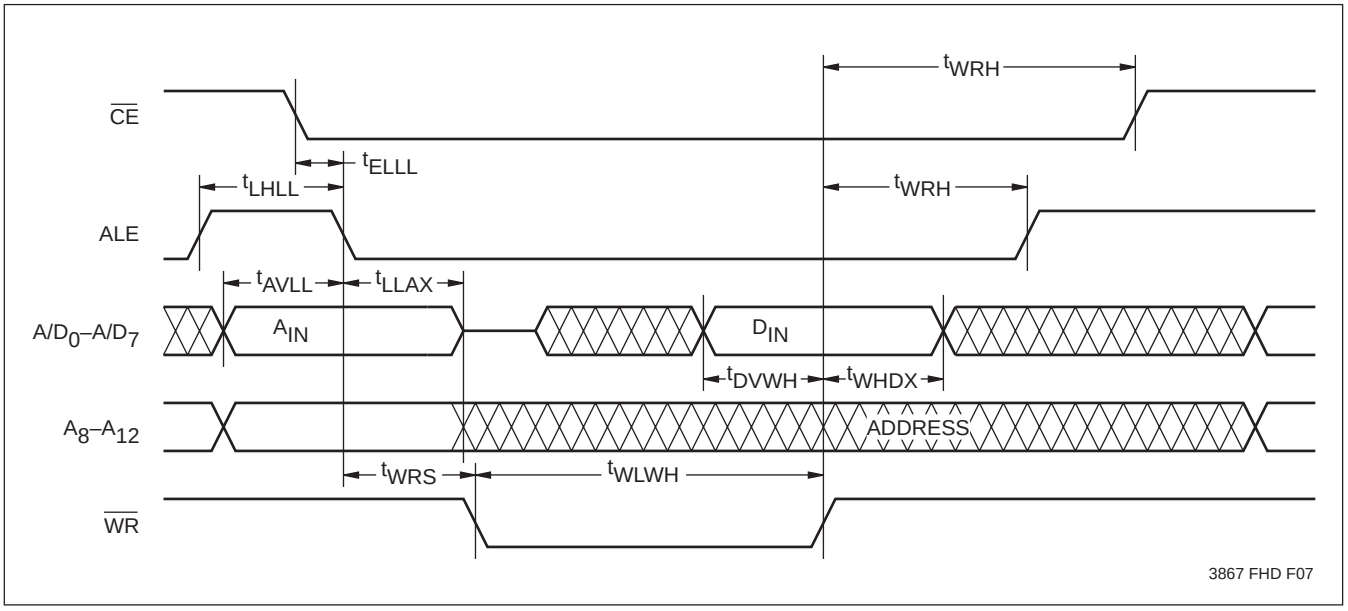
Note: (6) This parameter is periodically sampled and not 100% tested.

$\overline{WR}$ Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{DVWH}	Data Setup Time	50		ns
t_{WHDX}	Data Hold Time	30		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	120		ns
t_{WRS}	$\overline{WR}$ Setup Time	30		ns
t_{WRH}	$\overline{WR}$ Hold Time	20		ns
t_{BLC}	Byte Load Time (Page Write)	0.5	100	µs
t_{WC} (7)	Write Cycle Time		5	ms

3867 PGM T11

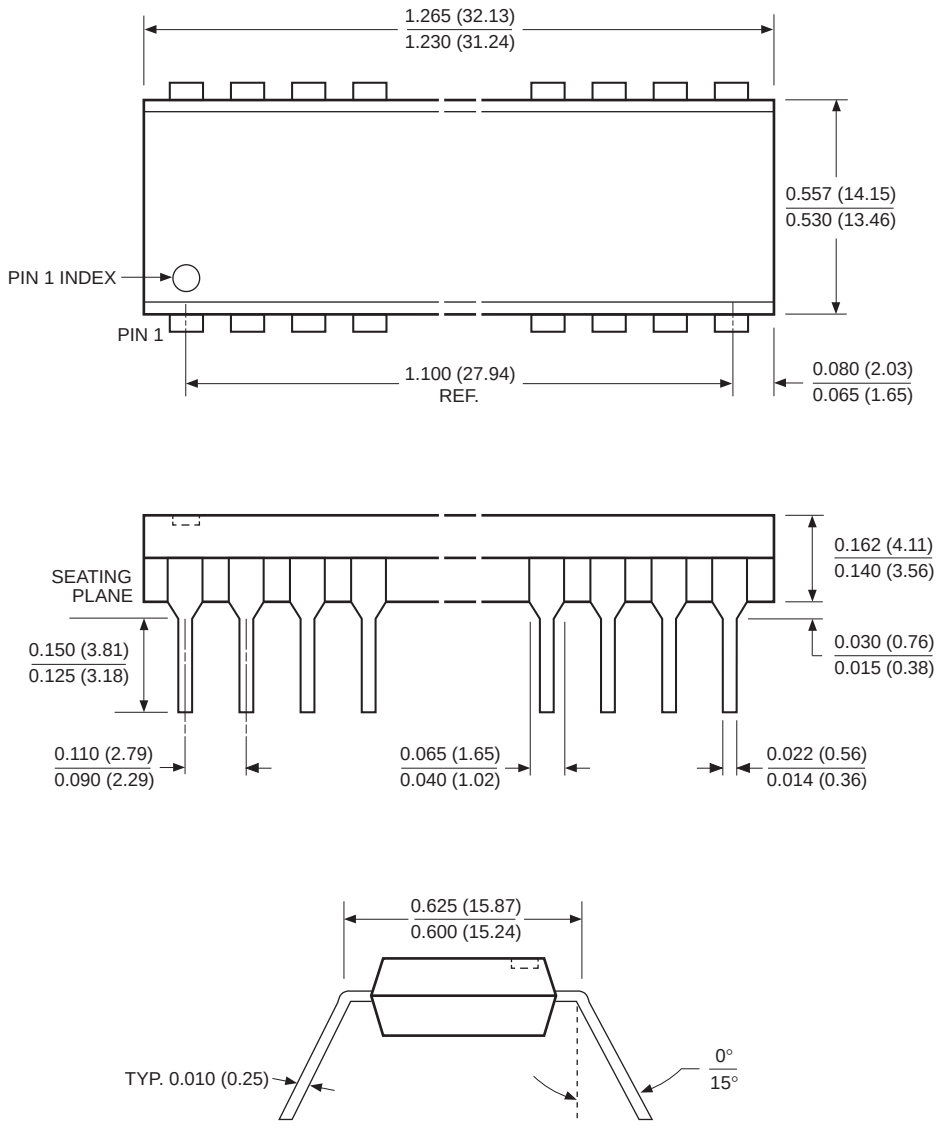
$\overline{WR}$ Controlled Write Timing Diagram



Note: (7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

PACKAGING INFORMATION

24-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



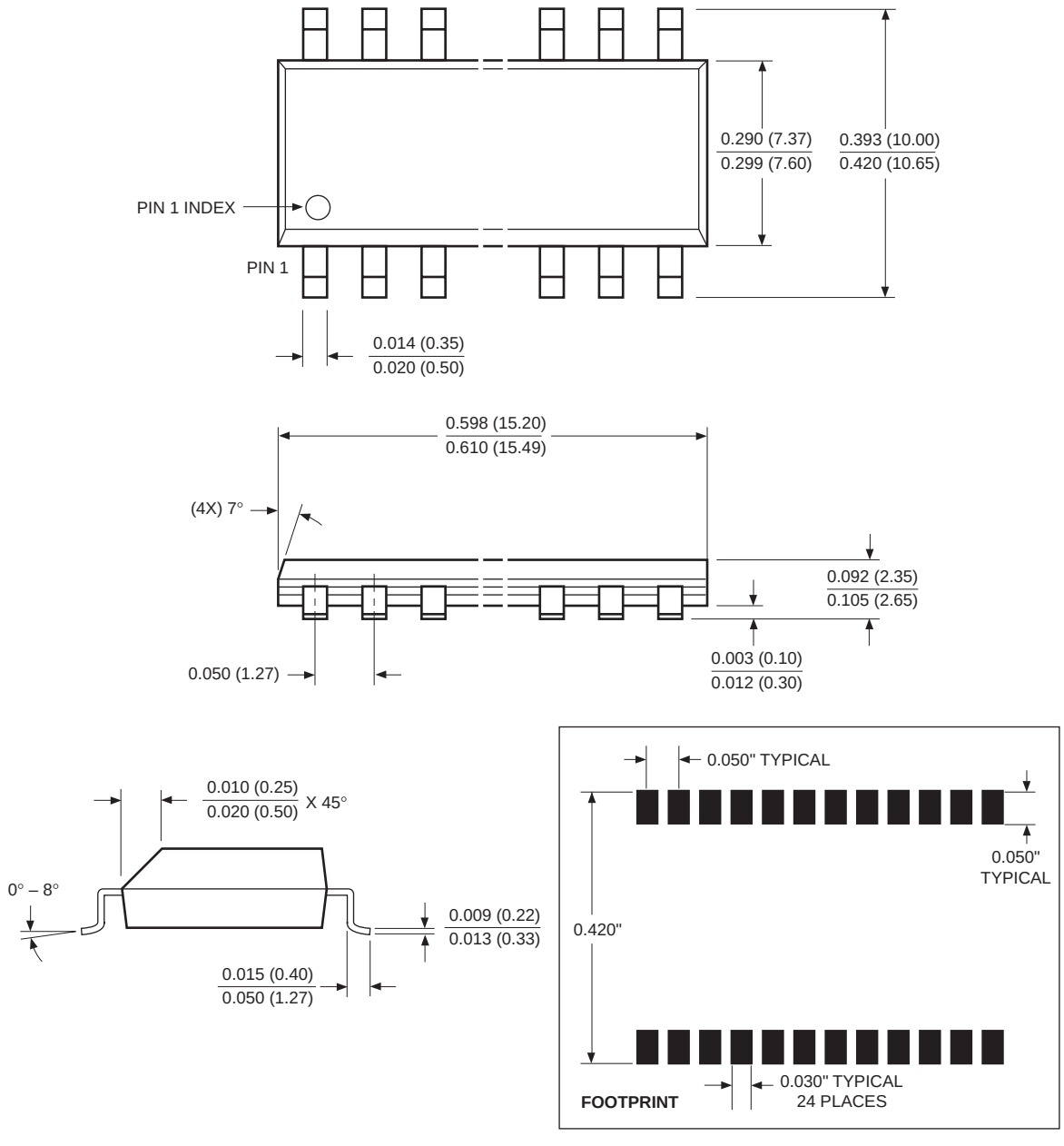
NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F03

PACKAGING INFORMATION

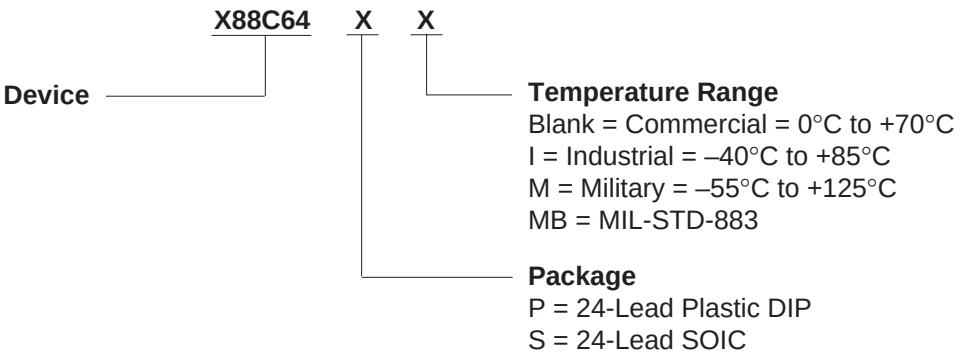
24-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F24

ORDERING INFORMATION



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US. PATENTS

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LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its satety or effectiveness.