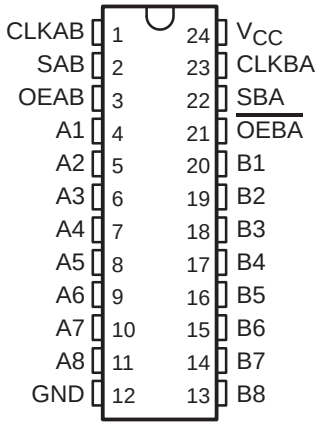
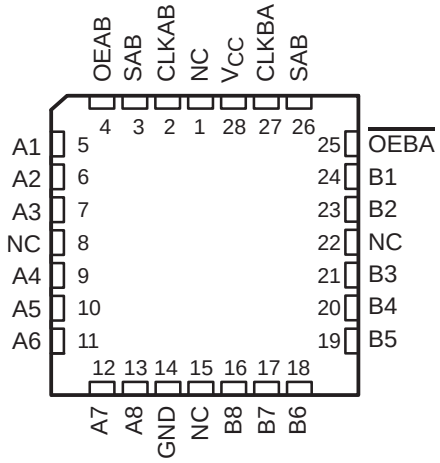
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 1 V at $V_{CC}$ = 5 V, $T_A$ = 25°C**
- **High-Drive Outputs (–32-mA $I_{OH}$, 64-mA $I_{OL}$)**
- **Multiplexed Real-Time and Stored Data**
- **Inverting Data Paths**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs**

**SN54ABT651 . . . JT PACKAGE**
**SN74ABT651 . . . DB, DW, NT, OR PW PACKAGE**
**(TOP VIEW)**




**SN54ABT651 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. The select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT651 devices.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it also is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all the other data sources to the two sets of bus lines are at high impedance, each set remains at its last state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

## description (continued)

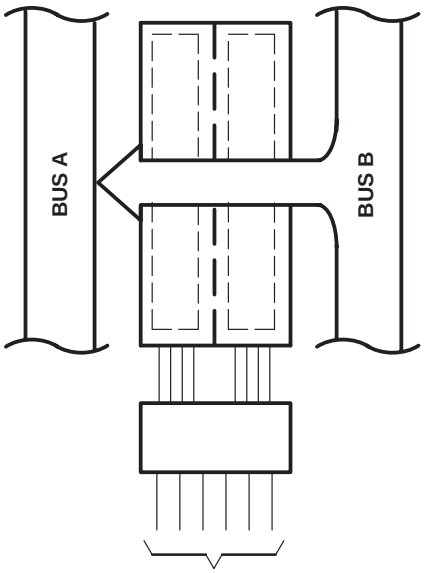
The SN54ABT651 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT651 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | | | | | DATA I/O | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| L | H | H or L | H or L | X | X | Input | Input | Isolation |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| X | H | ↑ | H or L | X | X | Input | Unspecified† | Store A, hold B |
| H | H | ↑ | ↑ | X‡ | X | Input | Output | Store A in both registers |
| L | X | H or L | ↑ | X | X | Unspecified† | Input | Hold A, store B |
| L | L | ↑ | ↑ | X | X‡ | Output | Input | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real-time $\overline{B}$ data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored $\overline{B}$ data to A bus |
| H | H | X | X | L | X | Input | Output | Real-time $\overline{A}$ data to B bus |
| H | H | H or L | X | H | X | Input | Output | Stored $\overline{A}$ data to B bus |
| H | L | H or L | H or L | H | H | Output | Output | Stored $\overline{A}$ data to B bus and stored $\overline{B}$ data to A bus |

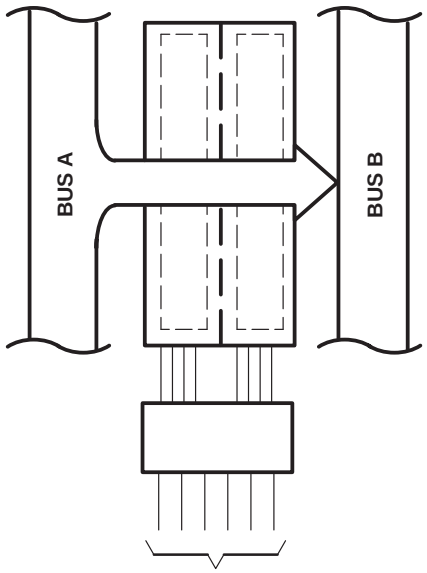
† The data output functions may be enabled or disabled by a variety of level combinations at OEAB or $\overline{OEBA}$. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

‡ When select control is low, clocks can occur simultaneously if allowances are made for propagation delays from A to B (B to A) plus setup and hold times. When select control is high, clocks must be staggered to load both registers.



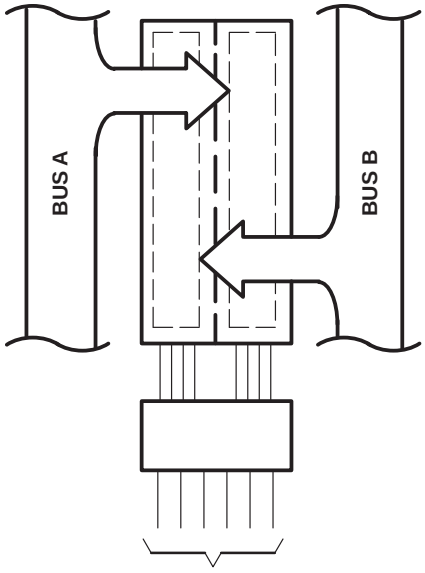

| 3 | 21 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
| L | L | X | X | X | L |

**REAL-TIME TRANSFER**
**BUS B TO BUS A**



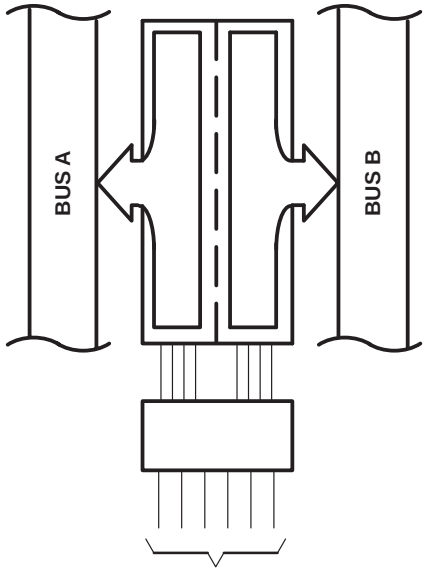

| 3 | 21 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
| H | H | X | X | L | X |

**REAL-TIME TRANSFER**
**BUS A TO BUS B**




| 3 | 21 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
| X | H | ↑ | X | X | X |
| L | X | X | ↑ | X | X |
| L | H | ↑ | ↑ | X | X |

**STORAGE FROM A, B, OR A AND B**



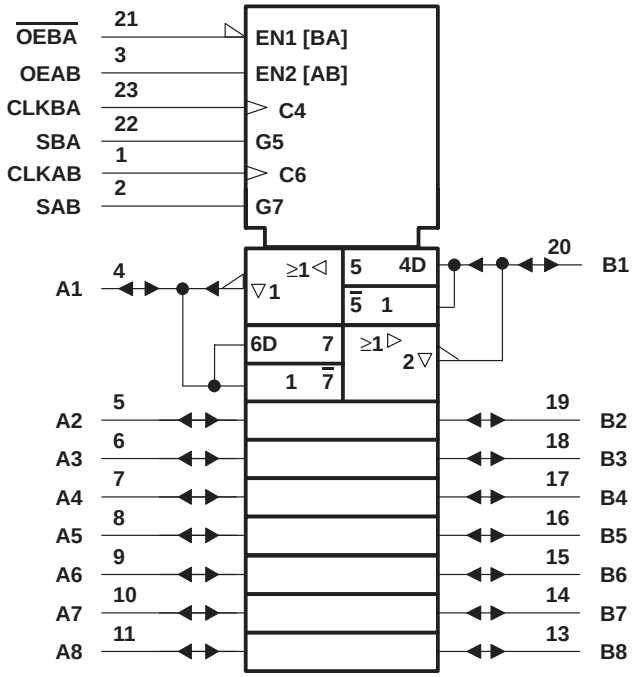

| 3 | 21 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
| H | L | H or L | H or L | H | H |

**TRANSFER STORED DATA TO A AND/OR B**

Pin numbers are for the DB, DW, JT, NT, and PW packages.

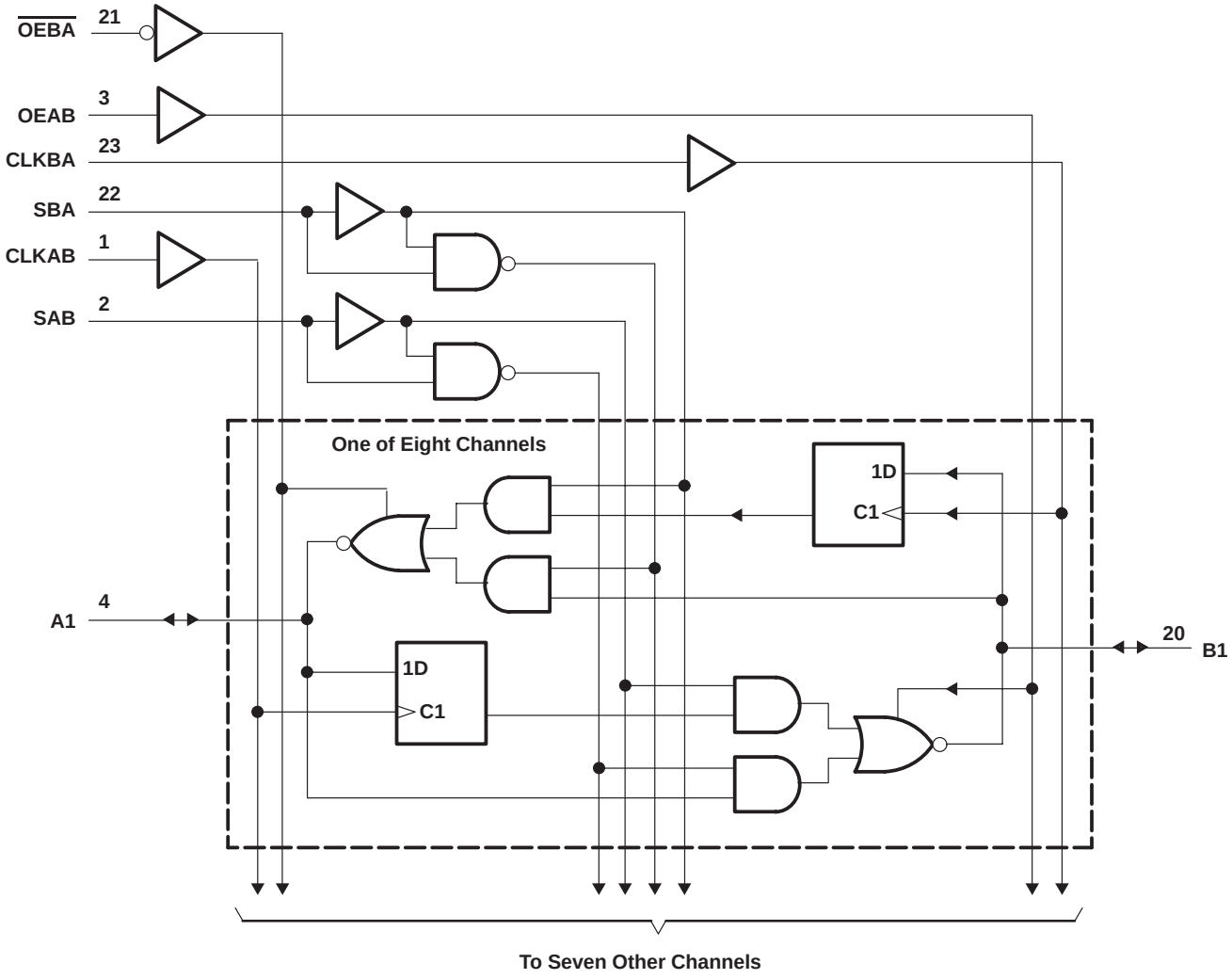
**Figure 1. Bus-Management Functions**

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, NT, and PW packages.

## logic diagram (positive logic)




Pin numbers shown are for the DB, DW, JT, NT, and PW packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ . . . . . –0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT651 . . . . . 96 mA
SN74ABT651 . . . . . 128 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –18 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 104°C/W
DW package . . . . . 81°C/W
NT package . . . . . 67°C/W
PW package . . . . . 120°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | SN54ABT651 | | SN74ABT651 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 5 | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |



NOTE 3: All unused pins (control or I/O) of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABT651 | | SN74ABT651 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | 2 | | | 2 | | | | |
| | | | $I_{OH}$ = –32 mA | 2* | | | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| $V_{hys}$ | | | | | 100 | | | | | | mV |
| $I_I$ | Control inputs | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | | | | | ±100 | | ±100 | | ±100 | |
| $I_{OZH}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | 50 | | 50 | µA |
| $I_{OZL}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –50 | | –50 | | –50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 4.5 V | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | | $V_{CC}$ = 5.5 V, $V_O$ = 5.5 V | Outputs high | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –100 | –180 | –50 | –180 | –50 | –180 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | | 250 | | 250 | | 250 | µA |
| | | | Outputs low | | | 30 | | 30 | | 30 | mA |
| | | | Outputs disabled | | | 250 | | 250 | | 250 | µA |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | 6 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | 7.5 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

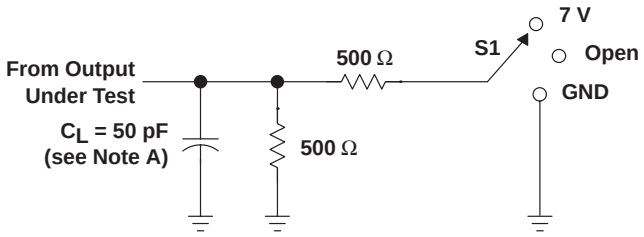
| | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54ABT651 | | SN74ABT651 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 125 | | 125 | | 125 | MHz |
| $t_w$ | Pulse duration, CLK high or low | 4 | | 4 | | 4 | | ns |
| $t_{su}$ | Setup time, A or B before CLKAB↑ or CLKBA↑ | 3 | | 3 | | 3 | | ns |
| $t_h$ | Hold time, A or B after CLKAB↑ or CLKBA↑ | 0 | | 0 | | 0 | | ns |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 2)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT651 | | SN74ABT651 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 125 | | | 125 | | 125 | | MHz |
| $t_{PLH}$ | CLKBA or CLKAB | A or B | 2.2 | 4 | 5.1 | 2.2 | 5.9 | 2.2 | 5.6 | ns |
| $t_{PHL}$ | | | 1.7 | 4 | 5.1 | 1.7 | 5.9 | 1.7 | 5.6 | |
| $t_{PLH}$ | A or B | B or A | 1.5 | 4 | 5.1 | 1.5 | 6.4 | 1.5 | 6.2 | ns |
| $t_{PHL}$ | | | 1.5 | 3.3 | 4.6 | 1.5 | 5.6 | 1.5 | 5.4 | |
| $t_{PLH}$ | SAB or SBA† | A or B | 1.5 | 4 | 5.1 | 1.5 | 6.8 | 1.5 | 6.5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.6 | 4.9 | 1.5 | 6.2 | 1.5 | 5.9 | |
| $t_{PZH}$ | $\overline{OEBA}$ | A | 1.3 | 3.6 | 4.6 | 1.3 | 5.9 | 1.3 | 5.8 | ns |
| $t_{PZL}$ | | | 2.5 | 5.7 | 6.8 | 2.5 | 8.9 | 2.5 | 8.5 | |
| $t_{PHZ}$ | $\overline{OEBA}$ | A | 1.5 | 3.2 | 4.5 | 1.5 | 6.2 | 1.5 | 5 | ns |
| $t_{PLZ}$ | | | 1.5 | 3 | 3.8 | 1.5 | 4.3 | 1.5 | 4.1 | |
| $t_{PZH}$ | OEAB | B | 1.8 | 4.3 | 6.1 | 1.8 | 6.7 | 1.8 | 6.5 | ns |
| $t_{PZL}$ | | | 2.9 | 5.5 | 6.5 | 2.9 | 7.6 | 2.9 | 7.4 | |
| $t_{PHZ}$ | OEAB | B | 1.5 | 3.3 | 4.5 | 1.5 | 6.5 | 1.5 | 5.5 | ns |
| $t_{PLZ}$ | | | 1.5 | 3.4 | 4.4 | 1.5 | 5.2 | 1.5 | 5.1 | |

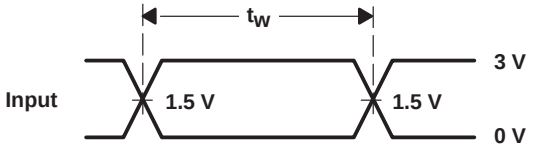
† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

## PARAMETER MEASUREMENT INFORMATION

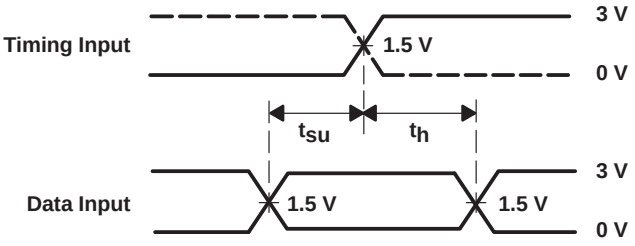



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

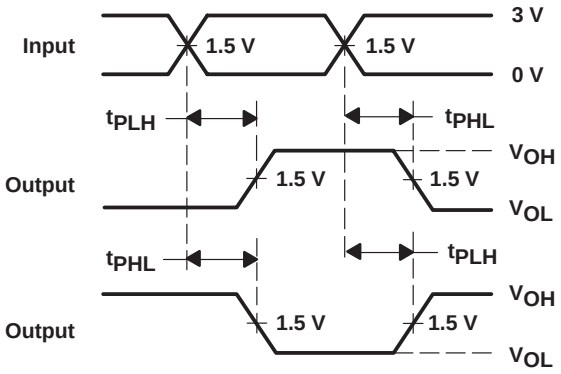
LOAD CIRCUIT



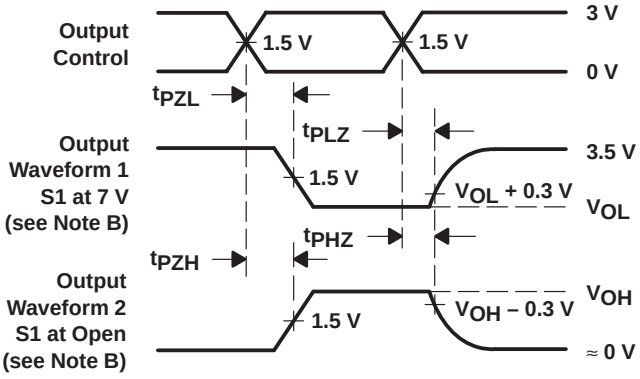

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ABT651DW | ACTIVE | SOIC | DW | 24 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ABT651 | Samples |
| SN74ABT651DWR | ACTIVE | SOIC | DW | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ABT651 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

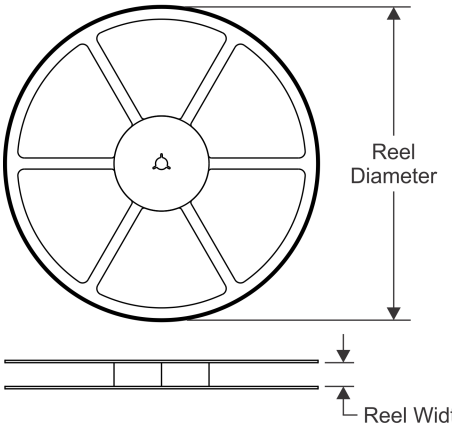
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

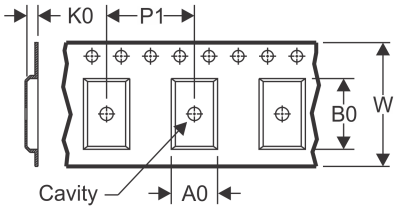
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

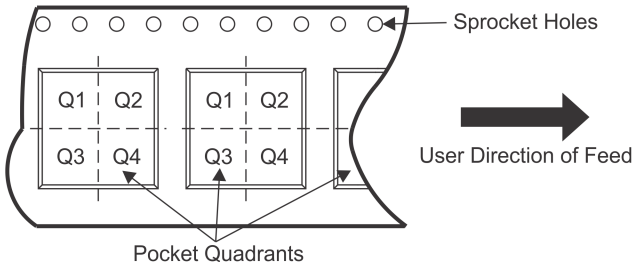



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

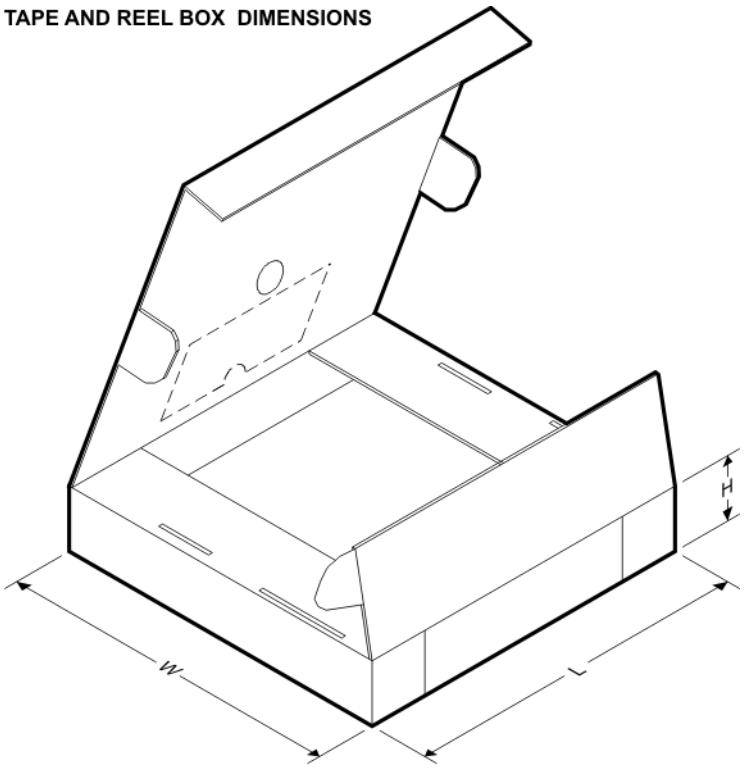
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ABT651DWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |

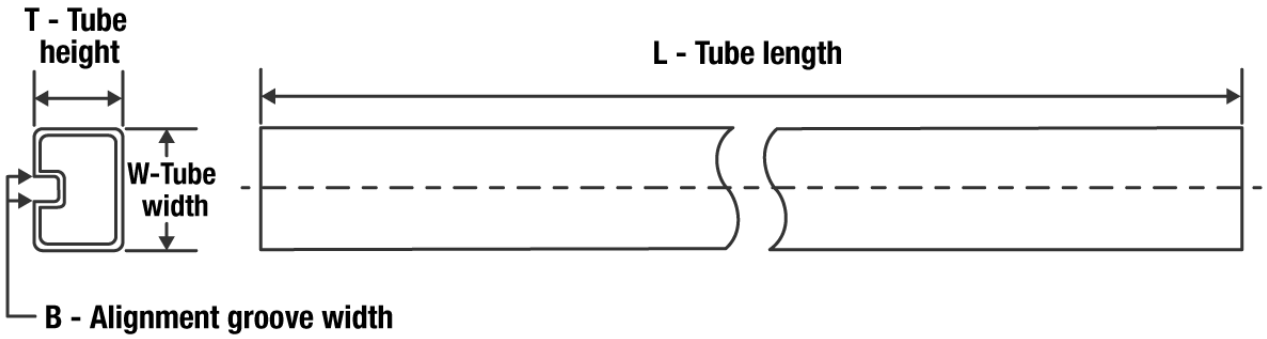
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ABT651DWR | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74ABT651DW | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |

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