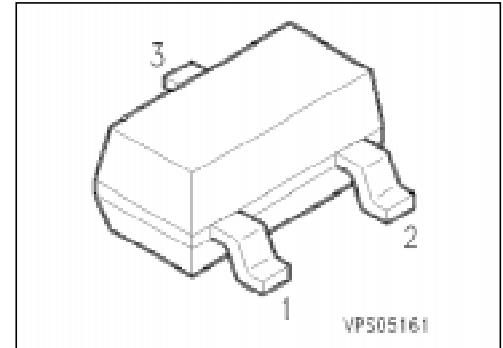


## Silicon N Channel MOS FET Triode

**BF 543**

### Preliminary Data

- For RF stages up to 300 MHz preferably in FM applications
- $I_{DSS} = 4 \text{ mA}$ ,  $g_{fs} = 12 \text{ mS}$



**ESD:** Electrostatic discharge sensitive device, observe handling precautions!

Type	Marking	Ordering Code (tape and reel)	Pin Configuration			Package <sup>1)</sup>
			1	2	3	
BF 543	LDs	Q62702-F1372	G	D	S	SOT-23

### Maximum Ratings

Parameter	Symbol	Values	Unit
Drain-source voltage	$V_{DS}$	20	V
Drain current	$I_D$	30	mA
Gate-source peak current	$\pm I_{GSM}$	10	
Total power dissipation, $T_A \leq 60 \text{ }^\circ\text{C}$	$P_{tot}$	200	mW
Storage temperature range	$T_{stg}$	- 55 ... + 150	$^\circ\text{C}$
Channel temperature	$T_{ch}$	150	
Ambient temperature range	$T_A$	- 55 ... + 150	

### Thermal Resistance

Junction - ambient <sup>2)</sup>	$R_{th \text{ JA}}$	$\leq 450$	K/W
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<sup>1)</sup> For detailed information see chapter Package Outlines.

<sup>2)</sup> Package mounted on alumina 15 mm × 16.7 mm × 0.7 mm.

## Electrical Characteristics

at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

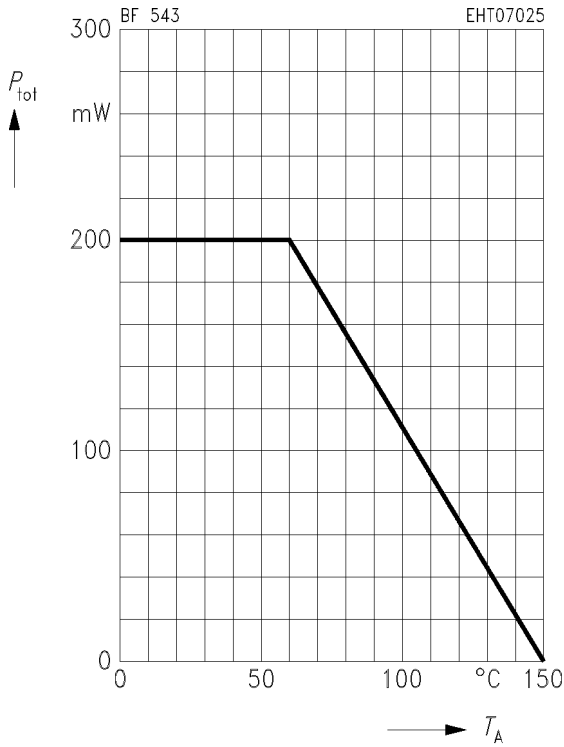
### DC Characteristics

Drain-source breakdown voltage $I_D = 10\text{ }\mu\text{A}$ , $-V_{GS} = 4\text{ V}$	$V_{(BR)DS}$	20	–	–	V
Gate-source breakdown voltage $\pm I_{GS} = 10\text{ mA}$ , $V_{DS} = 0$	$\pm V_{(BR)GSS}$	7	–	12	
Gate cutoff current $\pm V_{GS} = 6\text{ V}$ , $V_{DS} = 0$	$\pm I_{GSS}$	–	–	50	nA
Drain current $V_{DS} = 10\text{ V}$ , $V_{GS} = 0$	$I_{DSS}$	2.0	4	6.0	mA
Gate-source pinch-off voltage $V_{DS} = 10\text{ V}$ , $I_D = 20\text{ }\mu\text{A}$	$-V_{GS(p)}$	–	0.7	1.5	V

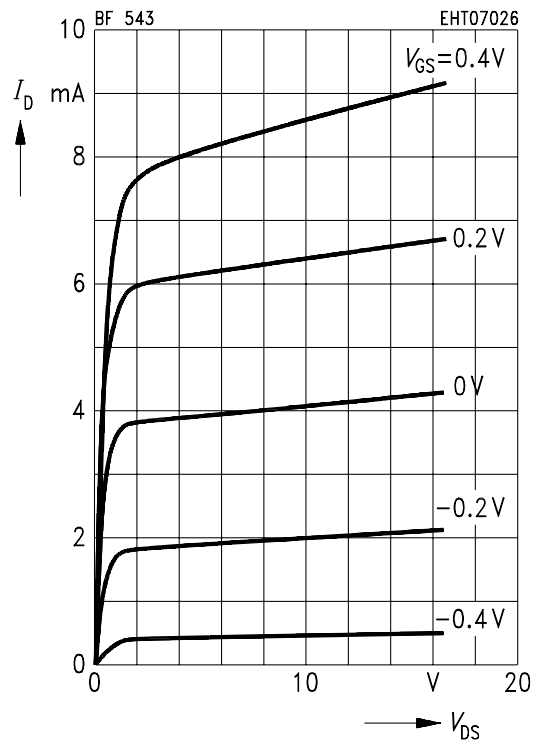
### AC Characteristics

Forward transconductance $V_{DS} = 10\text{ V}$ , $I_D = 4\text{ mA}$ , $f = 1\text{ kHz}$	$g_{fs}$	9.5	12	–	mS
Gate-1 input capacitance $V_{DS} = 10\text{ V}$ , $I_D = 4\text{ mA}$ , $f = 1\text{ MHz}$	$C_{gss}$	–	2.7	–	pF
Reverse transfer capacitance $V_{DS} = 10\text{ V}$ , $I_D = 4\text{ mA}$ , $f = 1\text{ MHz}$	$C_{dg}$	–	18	–	fF
Output capacitance $V_{DS} = 10\text{ V}$ , $I_D = 4\text{ mA}$ , $f = 1\text{ MHz}$	$C_{dss}$	–	0.9	–	pF
Power gain (test circuit) $V_{DS} = 10\text{ V}$ , $I_D = 4\text{ mA}$ , $f = 200\text{ MHz}$ $G_G = 2\text{ mS}$ , $G_L = 0.5\text{ mS}$	$G_p$	–	22	–	dB
Noise figure (test circuit) $V_{DS} = 10\text{ V}$ , $I_D = 4\text{ mA}$ , $f = 200\text{ MHz}$ $G_G = 2\text{ mS}$ , $G_L = 0.5\text{ mS}$	$F$	–	1	–	

Total power dissipation  $P_{tot} = f(T_A)$

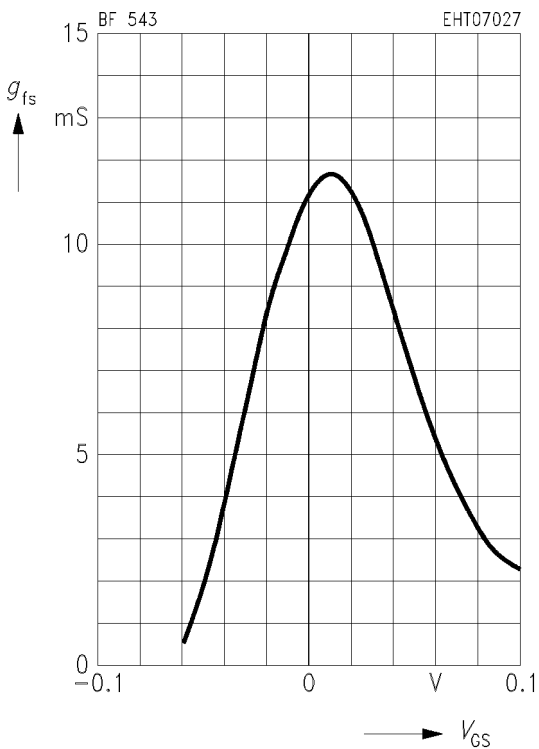


Typ. output characteristics  $I_D = f(V_{DS})$



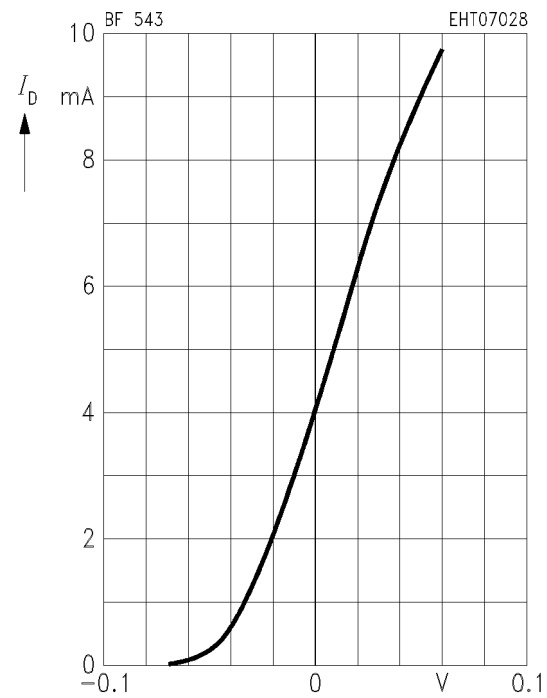
Gate transconductance  $g_{fs} = f(V_{GS})$

$V_{DS} = 10V, I_{DSS} = 4mA, f = 1kHz$



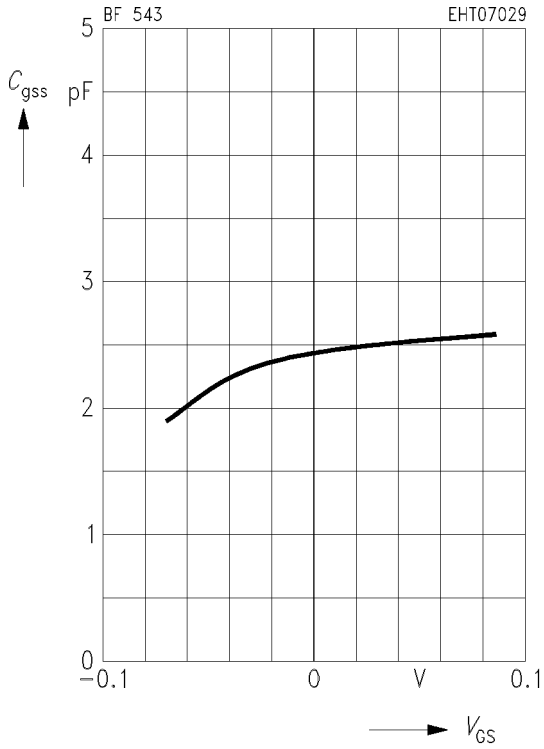
Drain current  $I_D = f(V_{GS})$

$V_{DS} = 10V$



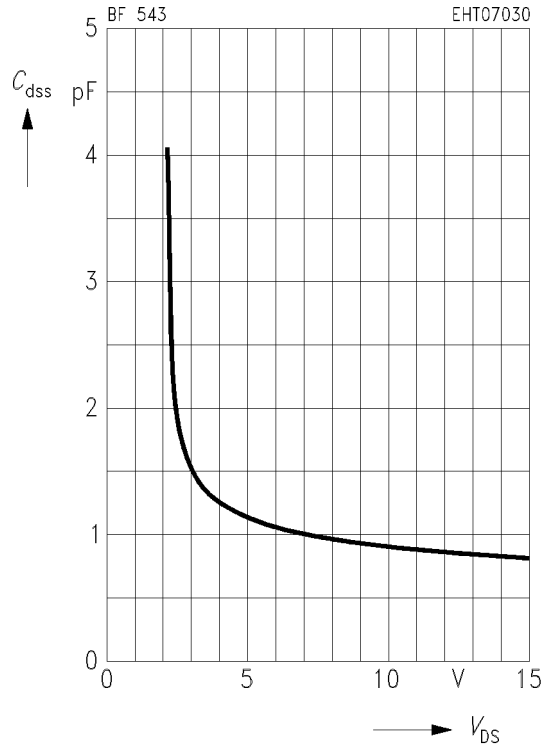
**Gate input capacitance  $C_{gss} = f(V_{GS})$**

$V_{DS} = 10\text{ V}$ ,  $I_{DSS} = 4\text{ mA}$ ,  $f = 1\text{ MHz}$



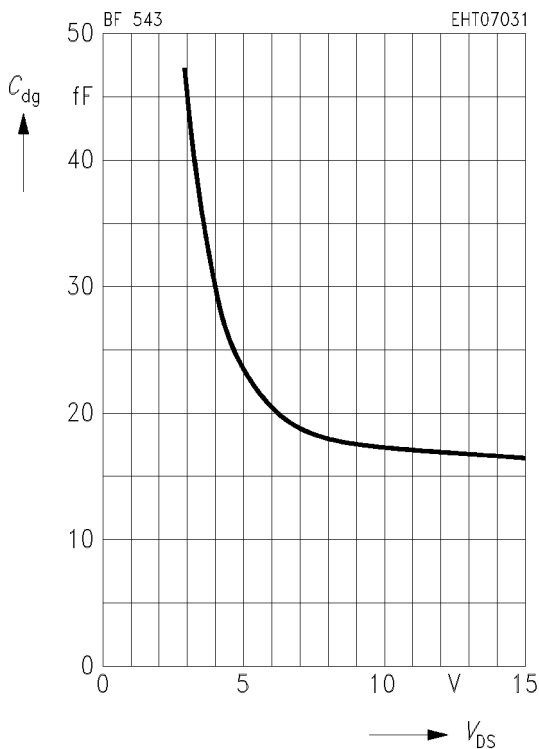
**Output capacitance  $C_{dss} = f(V_{DS})$**

$V_{GS} = 0$ ,  $I_{DSS} = 4\text{ mA}$ ,  $f = 1\text{ MHz}$



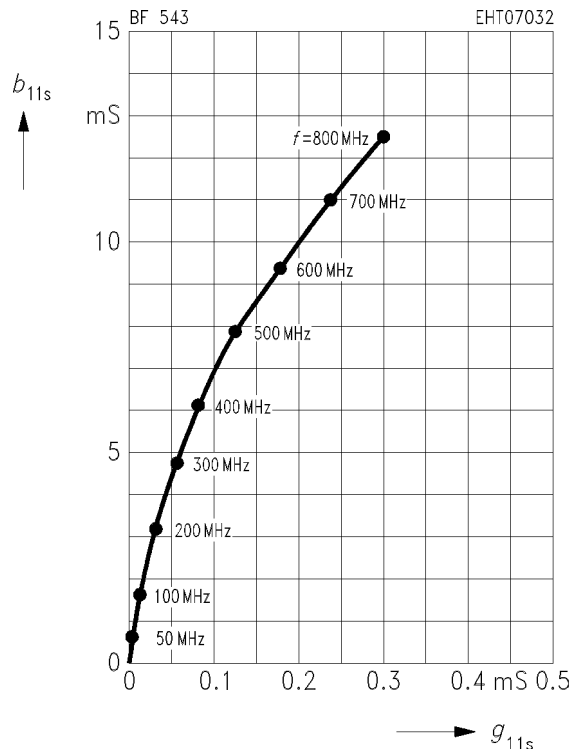
**Reverse transfer capacitance  $C_{dg} = f(V_{DS})$**

$V_{GS} = 0$ ,  $I_{DSS} = 4\text{ mA}$ ,  $f = 1\text{ MHz}$

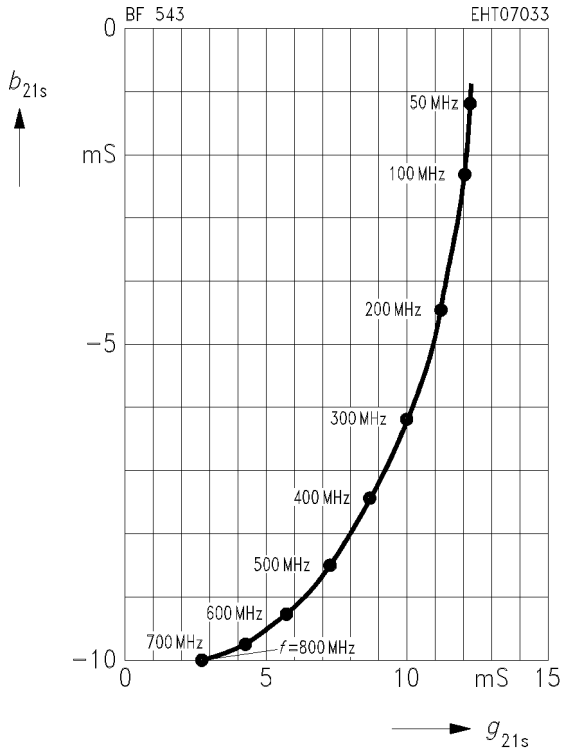


**Gate 1 input admittance  $y_{11s} = f(f)$**

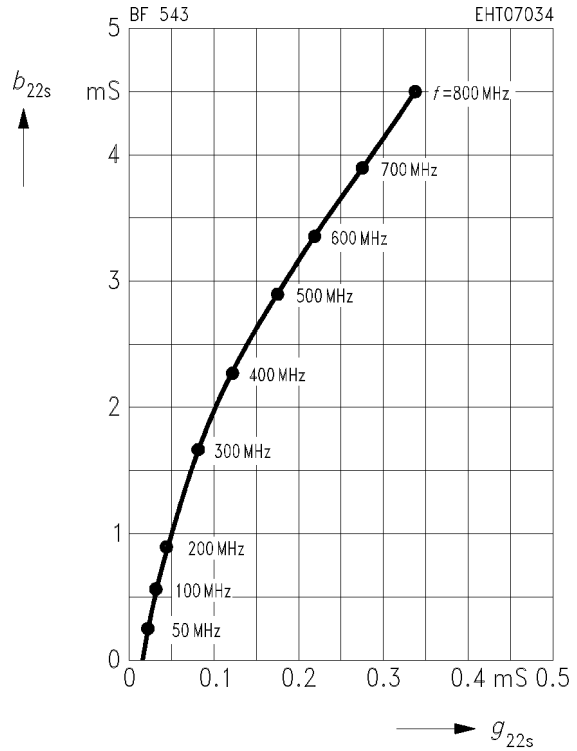
$V_{DS} = 10\text{ V}$ ,  $I_{DSS} = 4\text{ mA}$ ,  $V_{GS} = 0$   
(source circuit)



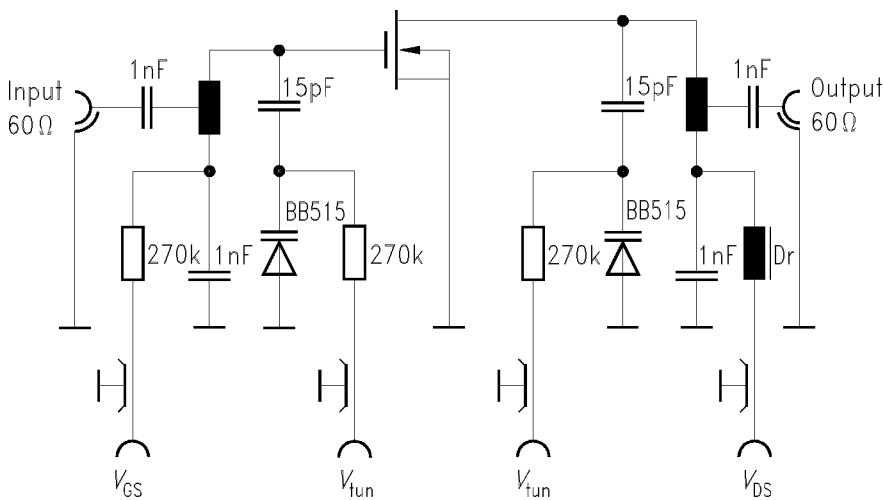
**Gate 1 transconductance  $y_{21s}$**   
 $V_{DS} = 10\text{ V}$ ,  $I_{DSS} = 4\text{ mA}$ ,  $V_{GS} = 0$   
 (source circuit)



**Output admittance  $y_{22s}$**   
 $V_{DS} = 10\text{ V}$ ,  $I_{DSS} = 10\text{ mA}$ ,  $V_{GS} = 0$   
 (source circuit)



**Test circuit for power gain  $G_p$  and noise figure  $F$**   
 $f = 200\text{ MHz}$ ,  $G_G = 2\text{ mS}$ ,  $G_L = 0.5\text{ mS}$



EHM07001