PanelBus ™ HDCP Digital Receiver

Check for Samples: TFP501

FEATURES

- **Supports Pixel Rates Up to 165 MHz (including 1080p and WUXGA at 60Hz)**
- **Digital Visual Interface (DVI) and High-Bandwidth Digital Content Proataection (HDCP) Specification Compliant** (1)
- **Encrypted External HDCP Device Key Storage for Exceptional Security and Ease of Implementation**
- **True-Color, 24 Bits/Pixel, 48-bit Dual Pixel Output Mode, 16.7M Colors at 1 or 2 Pixels Per Clock**
- **Laser Trimmed (50-Ω) Input Stage for Optimum Fixed Impedance Matching**
- **Skew Tolerant up to One Pixel Clock Cycle (High Clock and Data Jitter Tolerance)**
- **4x Over-Sampling for Reduced Bit-Error Rates and Better Performance Over Longer Cables**
- **Reduced Power Consumption From 1.8-V Core Operation With 3.3-V I/O's and Supplies** (2)
- **Reduced Ground-Bounce Using Time Staggered Pixel Outputs**
- **Lowest Noise and Best Power Dissipation Using TI 100-pin TQFP PowerPAD ™Packaging**
- **Advanced Technology Using TI's 0.18-mm EPIC-5™ CMOS Process**
- **Supports Hot Plug Detection**

(1) The digital visual interface (DVI) specification is an industry standard developed by the digital display working group (DDWG) for high-speed digital connection to digital displays. The high-bandwidth digital content protection system (HDCP) is an industry standard for protecting DVI outputs from being copied. HDCP was developed by Intel Corporation and is licensed by the Digital Content Protection, LLC. The TFP501 is compliant to the DVI Rev. 1.0 and HDCP Rev. 1.0 specifications.

(2) The TFP501 has an internal voltage regulator that provides the 1.8 V core power supply from the externally supplied 3.3 V supplies.

DESCRIPTION

The TFP501 is a Texas Instruments *PanelBus* flat panel display product, part of a comprehensive family of end-to-end DVI 1.0-compliant solutions. Targeted primarily at desktop LCD monitors, DLP and LCD projectors, and digital TVs, the TFP501 finds applications in any design requiring high-speed digital interface with the additional benefit of an extremely robust and innovative encryption scheme for digital content protection.

The TFP501 supports display resolutions up to 1080p and WUXGA in 24-bit true color pixel format. The TFP501 offers design flexibility to drive one or two pixels per clock, supports TFT or DSTN panels, and provides an option for time staggered pixel outputs for reduced ground-bounce.

PowerPAD advanced packaging technology results in best-of-class power dissipation, footprint, and ultra-low ground inductance.

The TFP501 combines *PanelBus* circuit innovation and unique implementation for HDCP key protection with TI's advanced 0.18 µm EPIC-5 CMOS process technology to achieve a completely secure, reliable, low-powered, low noise, high-speed digital interface solution.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

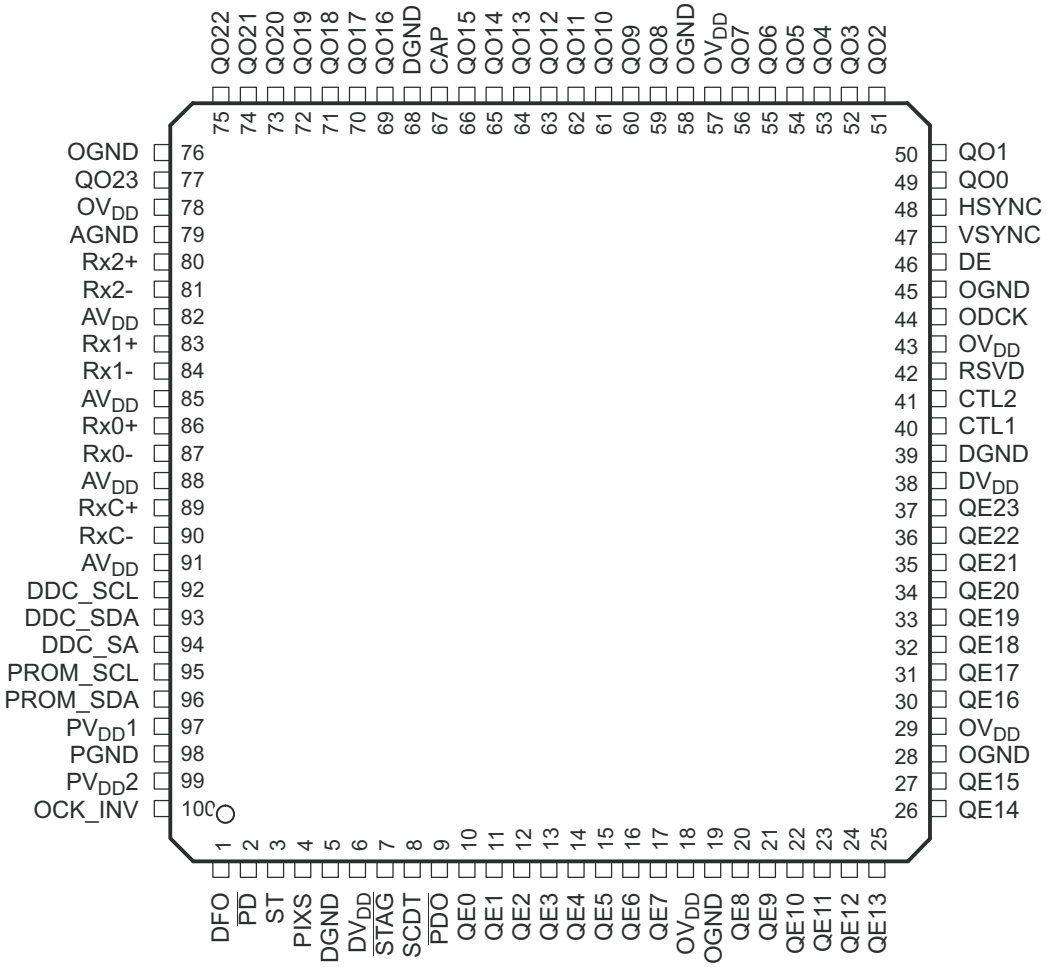
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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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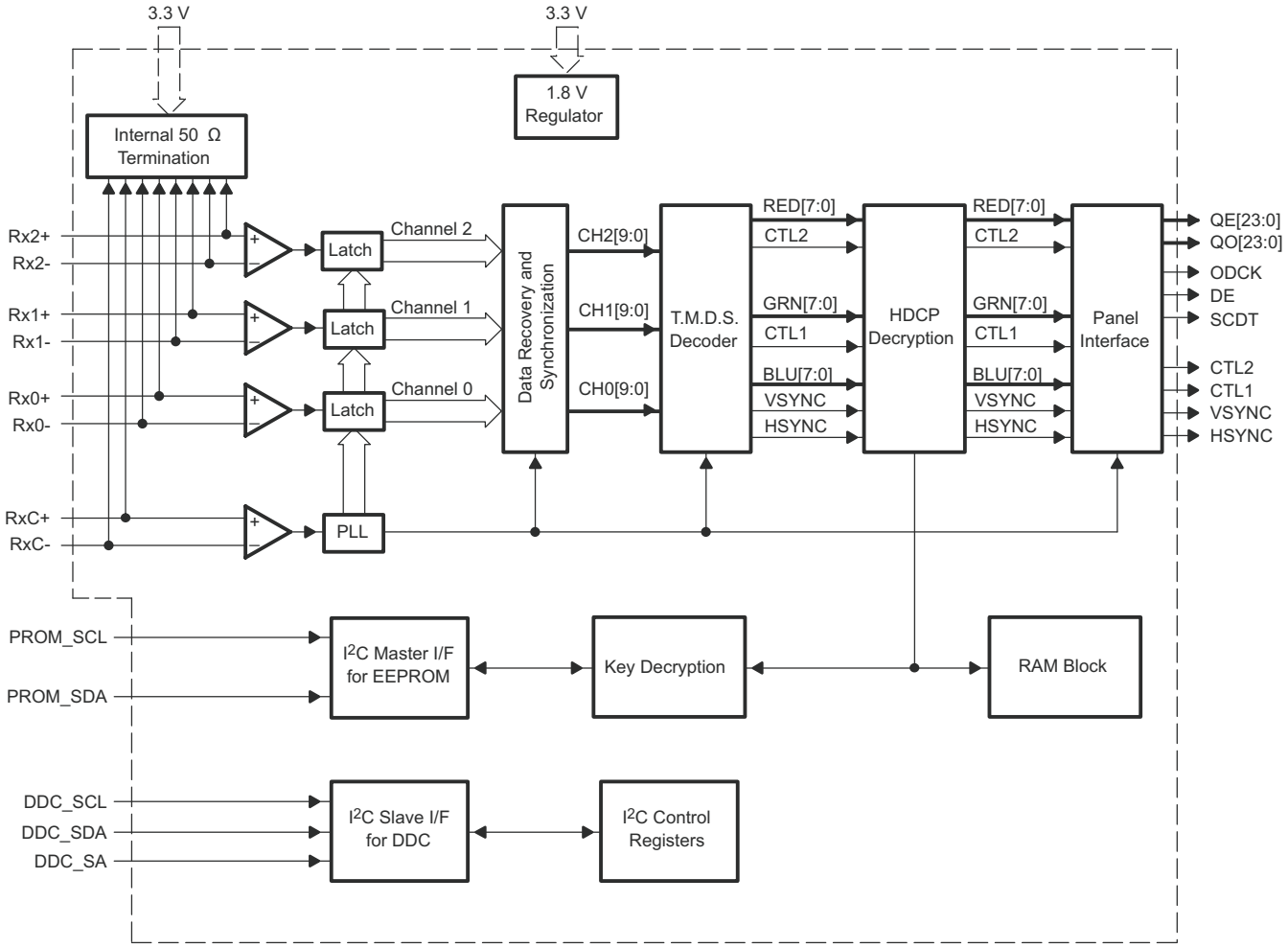
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TQFP PACKAGE
(TOP VIEW)



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FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	79		Analog Ground - Ground reference and current return for analog circuitry.
AV_{DD}	82, 85, 88, 91		Analog V_{DD} – Power supply for analog circuitry. Nominally 3.3 V
CAP	67	O	Bypass capacito r– 4.7 µF tantalum and 0.01 µF ceramic capacitors connected to ground.
CTL[2:1]	41, 40	O	General-purpose control signals – Used for user defined control. In normal mode CTL1 is not powered down via $\overline{PDO}$.
DDC_SA	94	I	Display data channel_serial address – I^2C Slave address bit A0 for display data channel (DDC). Refer to I^2C Interface section for more details.
DDC_SCL	92	I/O	Display data channel_serial clock – I^2C Clock for the DDC. External pullup resistors = 10 kΩ and 3.3 V tolerant.
DDC_SDA	93	I/O	Display data channel_serial data – I^2C Data for the DDC. External pullup resistors = 10 kΩ and 3.3 V tolerant.
DE	46	O	Output data enable – Used to indicate time of active video display versus nonactive display or blanking interval. During blanking, only HSYNC, VSYNC, and CTL1-2 are transmitted. During times of active display, or nonblanking, only pixel data, QE[23:0] and QO[23:0], is transmitted. High : active display interval Low: blanking interval
DFO	1	I	Output clock data format – Controls the output clock (ODCK) format for either TFT or DSTN panel support. For TFT support ODCK clock runs continuously. For DSTN support ODCK only clocks when DE is high; otherwise, ODCK is held low when DE is low. High : DSTN support/ODCK held low when DE = low Low: TFT support/ODCK runs continuously.
DGND	5, 39, 68		Digital ground – Ground reference and current return for digital core

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PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DV_{DD}	6, 38		Digital V_{DD} – Power supply for digital core. Nominally 3.3 V
HSYNC	48	O	Horizontal sync output
OCK_INV	100	I	ODCK Polarity - Selects ODCK edge on which pixel data (QE[23:0] and QO[23:0]) and control signals (HSYNC, VSYNC, DE, CTL1-2) are latched. Normal Mode: High : Latches output data on rising ODCK edge Low : Latches output data on falling ODCK edge
ODCK	44	O	Output data clock – Pixel clock. All pixel outputs QE[23:0] and QO[23:0] (if in 2-pixel/clock mode) along with DE, HSYNC, VSYNC and CTL[2:1] are synchronized to this clock.
OGND	19, 28 ,45, 58, 76		Output driver ground – Ground reference and current return for digital output drivers
OV_{DD}	18, 29, 43, 57, 78		Output driver VDD – Power supply for output drivers. Nominally 3.3 V
$\overline{PD}$	2	I	Power down – An active low signal that controls the TFP501 power-down state. During power down all output buffers are switched to a high-impedance state and brought low through a weak pulldown. All analog circuits are powered down and all inputs are disabled, except for $\overline{PD}$. If $\overline{PD}$ is left unconnected an internal pullup defaults the TFP501 to normal operation. High : Normal operation Low: Power down
$\overline{PDO}$	9	I	Output drive power down – An active low signal that controls the power-down state of the output drivers. During output drive power down, the output drivers (except SCDT and CTL1) are driven to a high-impedance state. A weak pulldown slowly pulls these outputs to a low level. When $\overline{PDO}$ is left unconnected an internal pullup defaults the TFP501 to normal operation. High : Normal operation/output drivers on Low: Output drive power down.
PGND	98		PLL ground – Ground reference and current return for internal PLL
PIXS	4	I	Pixel select – Selects between one or two pixel per clock output modes. During 2-pixel/clock mode, both even pixels, QE[23:0], and odd pixels, QO[23:0], are output in tandem on a given clock cycle. During 1 pixel/clock, even and odd pixels are output sequentially, one at a time, with the even pixel first, on the even pixel bus, QE[23:0]. (The first pixel per line is pixel-0, the even pixel. The second pixel per line is pixel-1, the odd pixel.) High : 2-pixel/clock Low: 1-pixel/clock
PROM_SCL	95	I/O	EEPROM_serial clock – I^2C clock for EEPROM interface data. External pullup resistors = 10 kΩ and 3.3 V tolerant.
PROM_SDA	96	I/O	EEPROM_serial data – I^2C data for EEPROM interface data. External pullup resistors = 10 kΩ and 3.3 V tolerant.
PV_{DD} (1, 2)	97, 99	V_{DD}	PLL V_{DD} – Power supply for internal PLL
QE[0:7]	10–17	O	Even blue pixel output – Output for even and odd green pixels when in 1-pixel/clock mode. Output for even only blue pixel when in 2-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QE0/pin 10 MSB: QE7/pin 17
QE[8:15]	20–27	O	Even green pixel output – Output for even and odd green pixels when in 1-pixel/clock mode. Output for even only green pixel when in 2-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QE8/pin 20 MSB: QE15/pin 27
QE[16:23]	30–37	O	Even red pixel output – Output for even and odd red pixels when in 1-pixel/clock mode. Output for even only red pixel when in 2-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QE16/pin 30 MSB: QE23/pin 37
QO[0:7]	49–56	O	Odd blue pixel output – Output for odd only blue pixel when in 2-pixel/clock mode. Not used, and held low, when in 1-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QO0/pin 49 MSB: QO7/pin 56
QO[8:15]	59–66	O	Odd green pixel output - Output for odd only green pixel when in 2-pixel/clock mode. Not used, and held low, when in 1-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QO8/pin 59 MSB: QO15/pin 66
QO[16:23]	69–75, 77	O	Odd red pixel output - Output for odd only red pixel when in 2-pixel/clock mode. Not used, and held low, when in 1-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QO16/pin 69 MSB: QO23/pin 77
RSVD	42	O	Reserved – Must be tied high for normal operation.
Rx2+	80	I	Channel-2 positive receiver input – Positive side of channel-2 TMDS low voltage signal differential input pair. Channel-2 receives red pixel data in active display and CTL2 control signals in blanking.

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PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
Rx2–	81	I	Channel-2 negative receiver input – Negative side of channel-2 TMDS low voltage signal differential input pair.
Rx1+	83	I	Channel-1 positive receiver input – Positive side of channel-1 TMDS low voltage signal differential input pair. Channel-1 receives green pixel data in active display and CTL1 control signals in blanking.
Rx1-	84	I	Channel-1 negative receiver input – Negative side of channel-1 TMDS low voltage signal differential input pair.
Rx0+	86	I	Channel-0 positive receiver input – Positive side of channel-0. TMDS low voltage signal differential input pair. Channel-0 receives blue pixel data in active display and HSYNC, VSYNC control signals in blanking.
Rx0-	87	I	Channel-0 negative receiver input – Negative side of channel-0. TMDS low voltage signal differential input pair.
RxC+	89	I	Clock positive receiver input – Positive side of reference clock. TMDS low voltage signal differential input pair.
RxC-	90	I	Clock negative receiver input – Negative side of reference clock. TMDS low voltage signal differential input pair.
SCDT	8	O	Sync detect – Output to signal when the link is active or inactive. The link is considered to be active when DE is actively switching. The TFP501 monitors the state DE to determine link activity. SCDT can be tied externally to $\overline{PDO}$ to power down the output drivers when the link is inactive. High: Active link Low: Inactive link
ST	3	I	Output drive strength select – Selects output drive strength for high or low current drive. (See dc specifications for I_{OH} and I_{OL} vs ST state). High : High drive strength Low : Low drive strength
$\overline{STAG}$	7	I	Staggered pixel select – An active low signal used in the 2-pixel/clock pixel mode (PIXS = high). Time staggers the even and odd pixel outputs to reduce ground bounce. Normal operation outputs the odd and even pixels simultaneously. High : Normal simultaneous even/odd pixel output Low: Time staggered even/odd pixel output
VSYNC	47	O	Vertical sync output

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
DV_{DD}, AV_{DD}, OV_{DD}, PV_{DD}	Supply voltage range		-0.3	4	V
	Input voltage range, logic/analog signals		-0.3	4	V
	Operating ambient temperature range		0	70	°C
T_{stg}	Storage temperature range		–65	150	°C
T_c	Case temperature for 10 seconds			260	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C
	ESD protection, all pins	Human Body Model		25	kV
	JEDEC latchup (EIA/JESD78)			100	mA

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD} (DV_{DD}, AV_{DD}, PV_{DD}, OV_{DD})	Supply voltage	3	3.3	3.6	V
$t_{(pixel)}$ (1)	Pixel time	6.06		40	ns
RT	Single ended analog input termination resistance (2)	45	50	57	Ω
T_A	Operating free-air temperature	0	25	70	°C

(1) t_{pix} is the pixel time defined as the period of the RxC clock input. The period of the output clock, ODCK is equal to $t_{(pixel)}$ when in 1-pixel/clock mode and 2 $t_{(pixel)}$ when in 2-pixel/clock mode.
(2) The TFP501 is internally optimized using a laser trim process to precisely fix the single-ended termination impedance, R_T to 50 Ω ±10%.

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DC DIGITAL I/O ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level digital input voltage (CMOS Inputs)(1)			0.7 DV_{DD}			V
V_{IL}	Low level digital input voltage (CMOS Inputs)(1)					0.3 DV_{DD}	V
V_{OH}	High level output drive current(2)	DV_{DD} = 3 V, V_{OH} = –5 V,	ST = High	2.4			V
		DV_{DD} = 3 V, V_{OH} = –3 V,	ST = Low	2.4			
V_{OL}	Low level digital output voltage (2)	DV_{DD} = 3.6 V, I_{OL} = 10 mA,	ST = High			0.4	V
		DV_{DD} = 3.6 V, I_{OL} = –3 V,	ST = Low			0.4	
$I_{OH(D)}$	High level output drive current (2)	ST = High, V_{OH} = 2.4 V		–5	–12	–18	mA
		ST = Low, V_{OH} = 2.4 V		–3	–7	–12	
$I_{OL(D)}$	Low level output drive current(2)	ST = High, V_{OH} =0.4 V		10	13	19	mA
		ST = Low, V_{OH} = 0.4 V		5	7	11	
I_{IH}	High level digital input current (1)	V_{IH} = DV_{DD}				±20	µA
I_{IL}	Low level digital input current (1)	V_{IL} = 0.0				±60	µA
I_{OZ}	Hi-Z output leakage current	$\overline{PD}$ = Low or $\overline{PDO}$ = Low				±20	µA

(1) Digital inputs are labeled I in I/O column of Pin Functions Table.
(2) Digital outputs are labeled O in I/O column of Pin Functions Table.

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DC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ID(1)}$	Analog input differential voltage(1)		150		1200	mV
V_{IC}	Analog input common mode voltage(1)		AV_{DD}–0.3		AV_{DD}–0.037	V
$V_{I(OC)}$	Open circuit analog input voltage		AV_{DD}–0.01		AV_{DD}+0.01	V
$I_{DD(2PIX)}$	Normal 2-pix/clock power supply current (2)	ODCK = 82.5 MHz, 2-pix/clock			460	mA
$I_{(PD)}$	Power down current (3)	$\overline{PD}$ = Low			10	mA
$I_{(PDO)}$	Output drive power down current(3)	$\overline{PDO}$ = Low		35		mA

(1) Specified as dc characteristic with no overshoot or undershoot.
(2) Alternating 2-pixel black/2-pixel white pattern. ST = high, $\overline{STAG}$ = high, QE[23:0] and QO[23:0] C_L = 10 pF.
(3) Analog inputs are open circuit (transmitter is disconnected from TFP501).

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AC ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{ID(2)}$	Differential input sensitivity(1)			150			mV_{p-p}
$V_{ID(3)}$	Maximum differential input					1560	mV_{p-p}
$t_{sk(D)}$	Analog input intra-pair (+ to –) differential skew(2)					0.4 $t_{(bit)}$(3)	ns
$t_{sk(CC)}$	Analog input intra-pair or channel to channel skew(2)					1.0 $t_{(pixel)}$(4)	ns
	Worst case differential input clock jitter tolerance(5)(2)	112 MHz, 1 pixel/clock			200		ps
$t_{r(1)}$	Rise time of data and control signals(6)(7)	ST = Low,	C_L = 10 pF			1.9	ns
		ST = High,	C_L = 10 pF			1.9	
$t_{f(1)}$	Fall time of data and control signals(6)(7)	ST = Low,	C_L = 10 pF			1.9	ns
		ST = High,	C_L = 10 pF			1.9	
$t_{r(2)}$	Rise time of ODCK clock(6)	ST = Low,	C_L = 5 pF			1.9	ns
		ST = High,	C_L = 10 pF			1.9	
$t_{f(2)}$	Fall time of ODCK clock(6)	ST = Low,	C_L = 5 pF			1.9	ns
		ST = High,	C_L = 10 pF			1.9	
$t_{su(1)}$	Setup time, data and control signal to falling edge of ODCK(7)	1 pixel/clock, PIXS = low, OCK_INV = low	ST = Low, C_L = 10 pF	1.2			ns
			ST = High, C_L = 10 pF	1.2			
		2 pixel/clock, PIXS = high, $\overline{STAG}$ = high, OCK_INV = low	ST = Low, C_L = 10 pF	2.7			ns
			ST = High, C_L = 10 pF	2.7			
		2 pixel and $\overline{STAG}$ PIXS = high, $\overline{STAG}$ = low, OCK_INV = low	ST = Low, C_L = 10 pF	1.7			ns
			ST = High, C_L = 10 pF	1.7			
$t_{h(1)}$	Hold time, data and control signal to falling edge of ODCK(7)	1 pixel/clock, PIXS = low, OCK_INV = low	ST = Low, C_L = 10 pF	0.9			ns
			ST = High, C_L = 10 pF	0.9			
		2 pixel and STAG, PIXS = high, $\overline{STAG}$ = low, OCK_INV = low	ST = Low, C_L = 10 pF	2.9			ns
			ST = High, C_L = 10 pF	2.9			
$t_{su(2)}$	Setup time, data and control signal to rising edge of ODCK (7)	1 pixel/clock, PIXS = low, OCK_INV = high	ST = Low, C_L = 10 pF	1.9			ns
			ST = High, C_L = 10 pF	1.9			
		2 pixel/clock, PIXS = high, $\overline{STAG}$ = high, OCK_INV = high	ST = Low, C_L = 10 pF	2.9			ns
			ST = High, C_L = 10 pF	2.9			
		2 pixel and STAG, PIXS = high, $\overline{STAG}$ = low, OCK_INV = high	ST = Low, C_L = 10 pF	2.0			ns
			ST = High, C_L = 10 pF	2.0			
$t_{h(2)}$	Hold time, data and control signal to rising edge of ODCK (7)	1 pixel/clock, PIXS = low, OCK_INV = high	ST = Low, C_L = 10 pF	0.5			ns
			ST = High, C_L = 10 pF	0.5			
		2 pixel and STAG, PIXS = high, $\overline{STAG}$ = Low, OCK_INV = high	ST = Low, C_L = 10 pF	1.4			ns
			ST = High, C_L = 10 pF	1.4			
$f_{(ODCK)}$	ODCK frequency	PIX = Low		25		165	MHz
		PIX = High		12.5		82.5	
	ODCK duty-cycle			45%	50%	60%	
$t_{pd(PDL)}$	Propagation delay time from $\overline{PD}$ low to Hi-Z outputs					18	ns
$t_{pd(PDOL)}$	Propagation delay time from $\overline{PDO}$ low to Hi-Z outputs					18	ns
$t_{(HSC)}$	Time between DE transition to SCDT low(8)	165 MHz			25		ms
$t_{t(FSC)}$	Time between DE low to SCDT high(8)				8		$trans_{(DE)}$(9)
$t_{d(st)}$	ODCK latching edge to QE[23:0] data output	$\overline{STAG}$ = Low, PIXS = High			0.2-5$t_{(pixel)}$		ns

(1) Specified as ac parameter to include sensitivity to overshoot, undershoot and reflection.
(2) By characterization
(3) $t_{(bit)}$ is 1/10 the pixel time, t_{pix}
(4) $t_{(pixel)}$ is the pixel time defined as the period of the RxC input clock. The period of ODCK is equal to t_{pix} in 1-pixel/clock mode or $2t_{pix}$ when in 2-pixel/clock mode.
(5) Measured differentially at 50% crossing using ODCK output clock as trigger.
(6) Rise and fall times measured as time between 20% and 80% of signal amplitude.
(7) Data and control signals are : QE[23:0], QO[23:0], DE, HSYNC, VSYNC and CTL[2:1]
(8) Link active or inactive is determined by amount of time detected between DE transitions. SCDT indicates link activity.
(9) $trans_{(DE)}$ is one transition (low-to-high or high-to-low) of the DE signal.

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PARAMETER MEASUREMENT INFORMATION

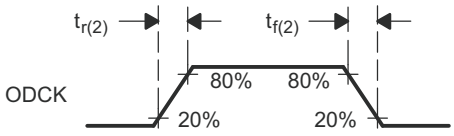


Figure 1. Rise and Fall Time of ODCK

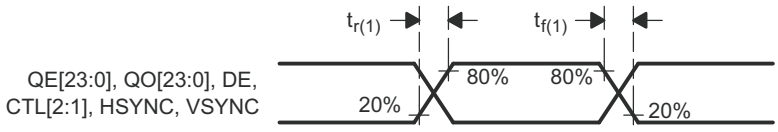


Figure 2. Rise and Fall Time of Data and Control Signals

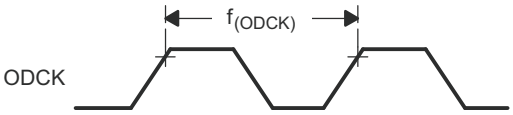


Figure 3. ODCK Frequency

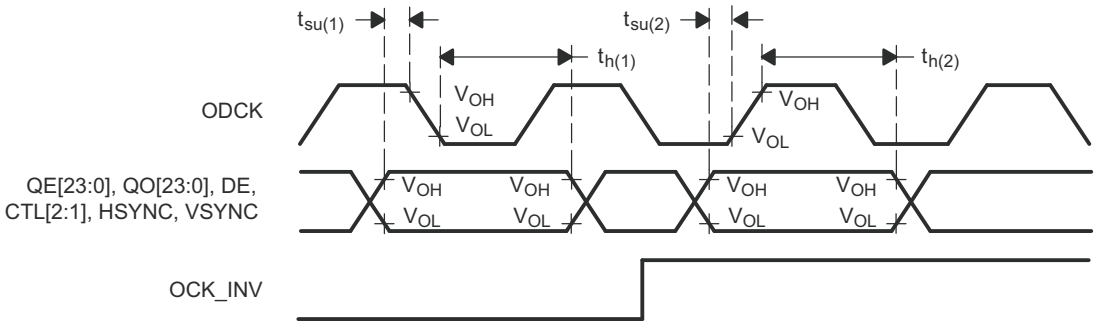


Figure 4. Data Setup and Hold Time to Rising and Falling Edge of ODCK

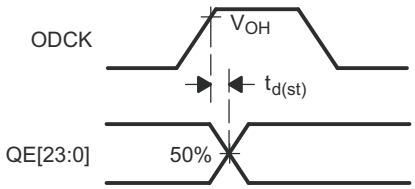


Figure 5. ODCK High to QE[23:0] Staggered Data Output

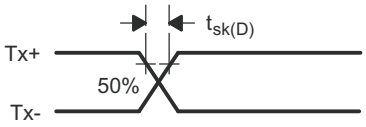


Figure 6. Analog Input Intra-Pair Differential Skew

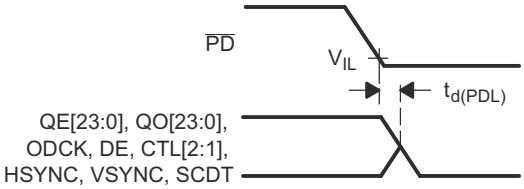


Figure 7. Delay from $\overline{PD}$ Low to Hi-Z Outputs

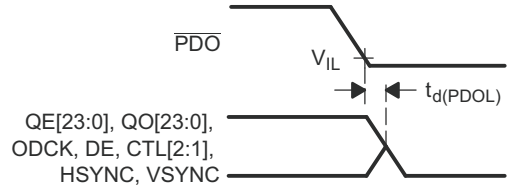


Figure 8. Delay from $\overline{PDO}$ Low to Hi-Z Outputs

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PARAMETER MEASUREMENT INFORMATION (continued)

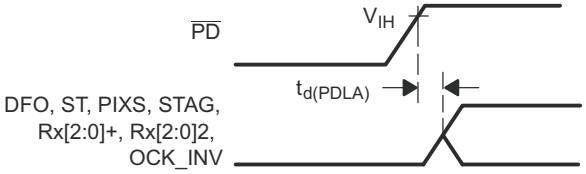


Figure 9. Delay from $\overline{PD}$ Low to High Before Inputs are Active

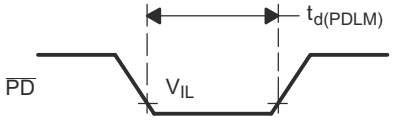


Figure 10. Minimum Time $\overline{PD}$ Low

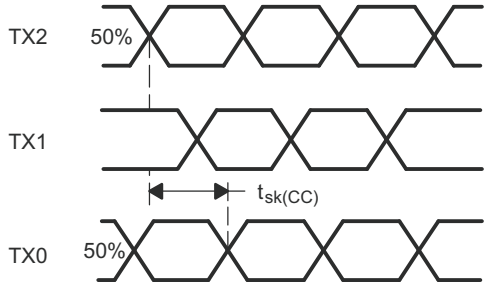


Figure 11. Analog Input Channel-to-Channel Skew

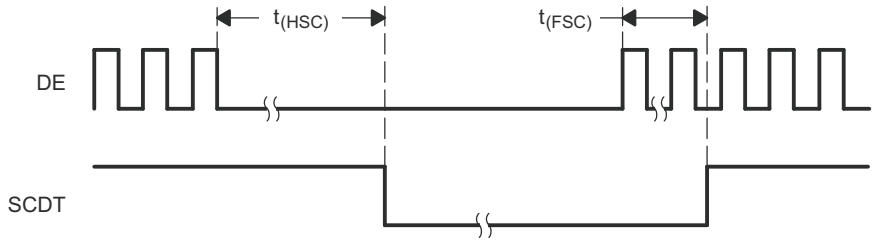


Figure 12. Time Between DE Transitions to SCDT Low and SCDT High

DETAILED DESCRIPTION

FUNDAMENTAL OPERATION

The TFP501 is a DVI digital receiver that is used in digital display systems to receive and decode TMDS encoded RGB pixel data streams. High-bandwidth digital content protection (HDCP) receiver functionality provides decryption of the DVI input data streams encrypted at the transmitter, such as TI's TFP510 HDCP transmitter, to prevent unauthorized viewing or coping of digital content. In a digital display system a host, usually a PC or consumer electronics device, contains a DVI compatible transmitter that receives 24-bit pixel data along with appropriate control signals. The HDCP TFP510 transmitter encrypts and encodes the signals into a high-speed, low-voltage, differential serial bit stream optimized for transmission over a twisted-pair cable to a display device. The display device, usually a flat-panel monitor, requires a DVI and HDCP compatible receiver like the TI TFP501 to decode and decrypt the serial bit stream back to the same 24-bit pixel data and control signals that originated at the host. This decoded data can then be applied directly to the flat panel drive circuitry to produce an image on the display. Since the host and display can be separated by distances up to five meters or more, serial transmission of the pixel data is preferred. To support modern display resolutions up to UXGA, a high-bandwidth receiver with good jitter and skew tolerance is required.

TMDS PIXEL DATA AND CONTROL SIGNAL ENCODING

TMDS stands for transition minimized differential signaling. Only one of two possible TMDS characters for a given pixel is transmitted at a given time. The transmitter keeps a running count of the number of ones and zeros previously sent, transmits the character that minimizes the number of transitions, and approximates a dc balance of the transmission line.

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Three TMDS channels are used to receive RGB pixel data during active display time, DE = High. These same three channels are also used to receive HSYNC, VSYNC, CTL3, and two user definable control signals, CTL[2:1], during inactive display or blanking interval (DE = Low). The following table maps the received input data to the appropriate TMDS input channel in a DVI-compliant system.

RECEIVED PIXEL DATA ACTIVE DISPLAY DE = HIGH	**INPUT CHANNEL**	**OUTPUT PINS (VALID FOR DE = HIGH)**
Red[7:0]	Channel – 2 (Rx2 ±)	QE[23:16] QO[23:16]
Green[7:0]	Channel – 1 (Rx1 ±)	QE[15:8] QO[15:8]
Blue[7:0]	Channel – 0 (Rx0 ±)	QE[7:0] QO[7:0]
RECEIVED CONTROL DATA BLANKING DE = LOW	**TMDS INPUT CHANNEL**	**OUTPUT PINS (VALID FOR DE = LOW)**
CTL[3:2] (1)	Channel – 2 (Rx2 ±)	CTL2
CTL[1:](1)	Channel – 1 (Rx1 ±)	CTL1
HSYNC, VSYNC	Channel – 0 (Rx0 ±)	HSYNC, VSYNC

(1) Some TMDS transmitters transmit a CTL0 signal. The TFP501 decodes and transfers CTL[32:1] and ignores CTL0 characters. CTL3 is used internally to enabl HDCP decryption. CTL3 and CTL0 are not available as a TFP4501 outputs.

The TFP501 discriminates between valid pixel TMDS characters and control TMDS characters to determine the state of active display versus blanking, i.e., state of DE.

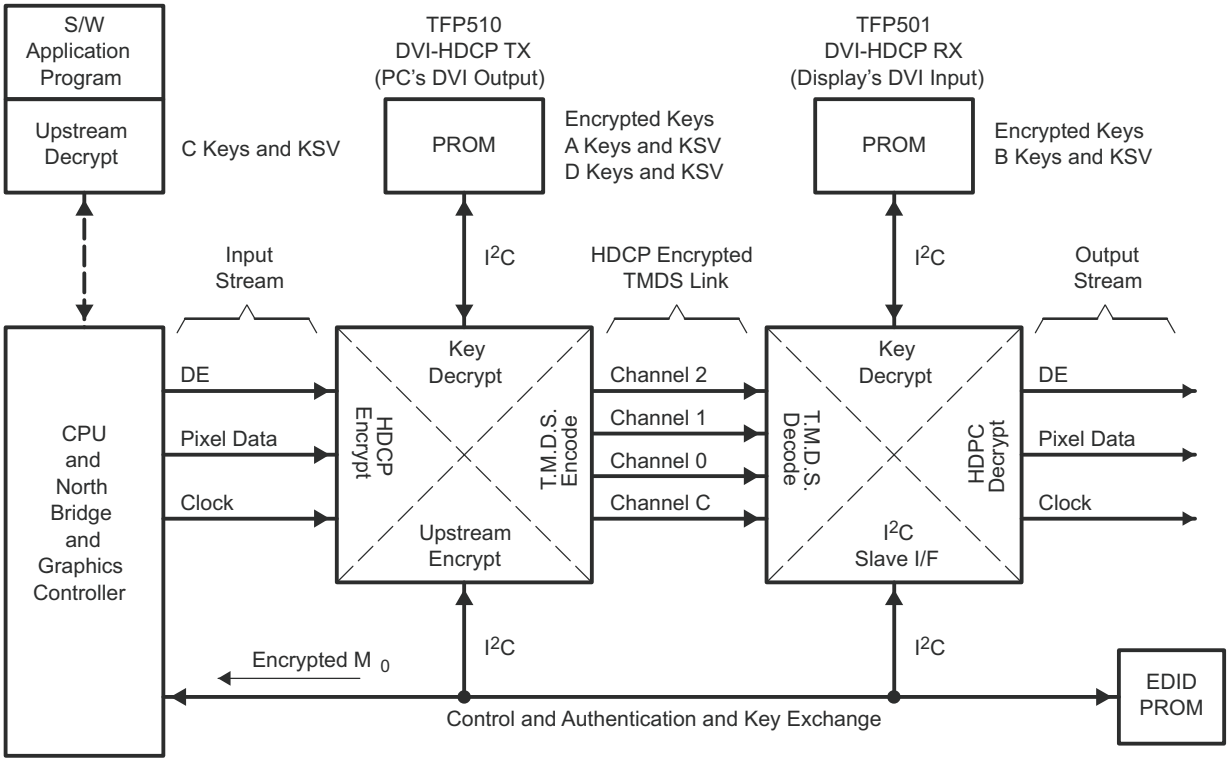
HIG-BANDWIDTH DIGITAL CONTENT PROTECTION (HDCP) OVERVIEW

TI's HDCP transmitters and receivers use up to three cipher engines to protect information that may be externally accessible to the user.

The downstream encryption described in the specification *high-bandwidth digital content protection system* Revision 1.0 is used to protect video data passing from the HDCP transmitter to the HDCP receiver via a DVI link. The HDCP transmitter encrypts video data and the receiver decrypts the data as shown inFigure 13.

The HDCP keys must also be protected from access. TI has chosen to avoid the inconvenience and possible circuit board damage from using epoxy or other barriers between the EEPROM and DVI receiver. An encryption scheme is used to protect the HDCP device key values passing from an off-chip EEPROM to the HDCP receiver via a dedicated I^2C interface. When the HDCP device keys are needed, the encrypted values are read from the EEPROM, decrypted, and used to enable HDCP functionality. TI's HDCP solution provides real advantages with respect to lower systems level cost, ease of implementation, high performance, and exceptional security.

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KSV = Key Selection Vector
M_0 = 64-Bit Secret Value

Figure 13. TI's HDCP Implementation for PC and Display System

TFP501 CLOCKING AND DATA SYNCHRONIZATION

The TFP501 receives a clock reference from the DVI transmitter, such as the TFP510, that has a period equal to the pixel time, $t_{(pixel)}$. The frequency of this clock is also referred to as the pixel rate. Since the TMDS encoded data on Rx[2:0] contains 10 bits per 8-bit pixel, it follows that the Rx[2:0] serial bit rate is 10 times the pixel rate. For example, the required pixel rate to support an UXGA resolution with 60 Hz refresh rate is 165 MHz. The TMDS serial bit rate is 10x the pixel rate or 1.65 Gb/s. Due to the transmission of this high speed digital bit stream on three separate channels (or twisted-pair wires) of long distances (3–5 meters), phase synchronization between the data steams and the input reference clock is not assured. In addition, skew between the three data channels is common. The TFP501 uses a 4x oversampling scheme of the input data streams to achieve reliable synchronization with up to 1-$T_{(pixel)}$ channel-to-channel skew tolerance. Accumulated jitter on the clock and data lines due to reflections and external noise sources is also typical of high-speed serial data transmission. The TFP501 is designed for high jitter tolerance.

The input clock to the TFP501 is conditioned by a PLL (phase-locked-loop) to remove high frequency jitter from the clock. The PLL provides four 10x clock outputs of different phases to locate and sync the TMDS data streams (4x oversampling). During the active display interval, the pixel data is encoded to be transition minimized; whereas, during the blanking interval, the control data is encoded to be transition maximized. A DVI-compliant transmitter is required to transmit during the blanking interval for a minimum period of time, 128-$t_{(pixel)}$, to ensure sufficient time for data synchronization when the receiver sees a transition maximized code. Performing synchronization during the blanking interval, when the data is transition maximized, assures reliable data bit boundary detection. Phase synchronization to the data streams is unique for each of the three input channels and is maintained as long as the link remains active.

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TFP501 TMDS INPUT LEVELS AND INPUT IMPEDANCE MATCHING

The TMDS inputs to the TFP501 receiver have a fixed single-ended input termination impedance to AV_{DD}. The TFP501 is internally optimized using a laser trim process to precisely fix the single-ended termination impedance at 50 Ω. This fixed impedance eliminates the need for external termination resistors while providing optimum impedance matching to standard DVI cables having a characteristic impedance of 100 Ω.

Figure 14 shows a conceptual schematic of a TFP510 transmitter and TFP501 receiver connection. The TFP510 transmitter drives the twisted-pair cable via a current source, usually achieved with an open-drain type output driver. The internal single-ended termination resistors, which are matched to the characteristic impedance of the DVI cable, provide a pullup to A_{VDD}. Naturally, when the transmitter is disconnected and the TFP501 DVI inputs are left unconnected, the TFP501 receiver inputs are pulled up to AV_{DD}. The single-ended differential signal and full differential signal is shown in Figure 15. The TFP501 is designed to respond to differential signal swings ranging from 150 mV to 1.56 V with common mode voltages ranging from (AV_{DD}–300 mV) to (AV_{DD}–37 mV).

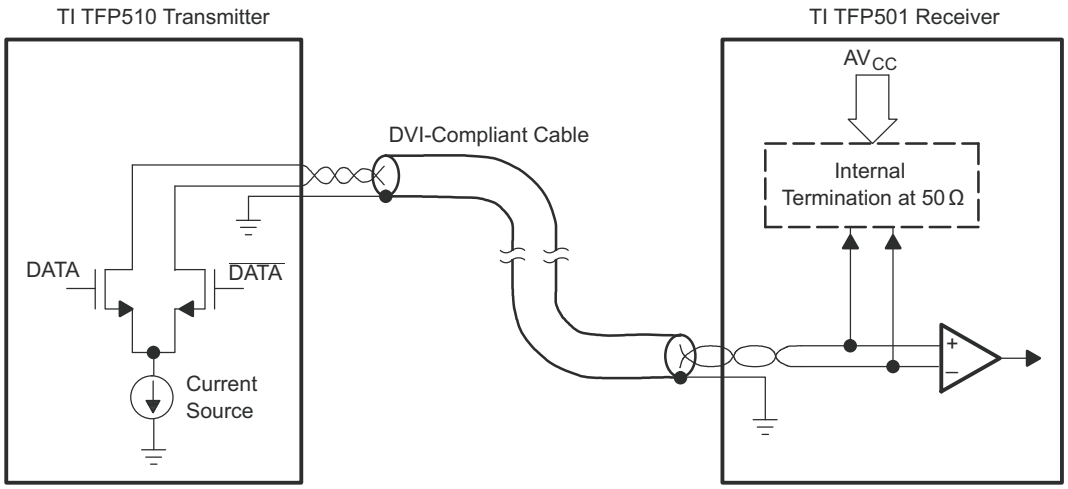


Figure 14. TMDS Differential Input and Transmitter Connection

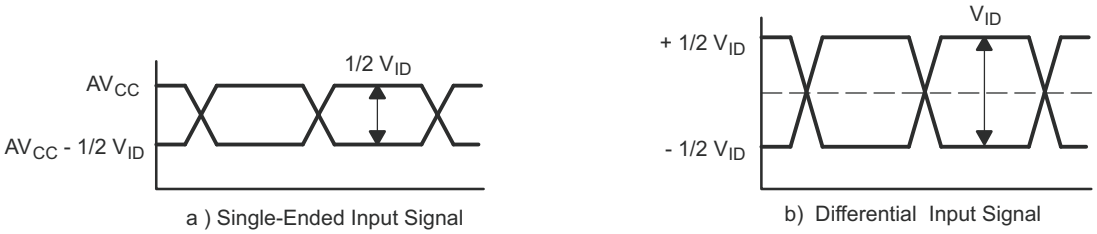


Figure 15. TMDS Inputs

TFP501 MODES OF OPERATION

The TFP501 provides system design flexibility and value by providing the system designer with configurable options or modes of operation to support varying system architectures. The following table outlines the various panel modes that can be supported along with appropriate external control pin settings.

PANEL	PIXEL RATE	ODCK LATCH EDGE	ODCK	DFO	PIXS	OCK_INV
TFT or 16-bit DSTN	1 pixel/clock	Falling	Free run	0	0	0
TFT or 16-bit DSTN	1 pixel/clock	Rising	Free run	0	0	1
TFT	2 pixel/clock	Falling	Free run	0	1	0
TFT	2 pixel/clock	Rising	Free run	0	1	1
24-bit DSTN	1 pixel/clock	Falling	Gated low	1	0	0
NONE	1 pixel/clock	Rising	Gated low	1	0	1

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PANEL	PIXEL RATE	ODCK LATCH EDGE	ODCK	DFO	PIXS	OCK_INV
24-bit DSTN	2 pixel/clock	Falling	Gated low	1	1	0
24-bit DSTN	2 pixel/clock	Rising	Gated low	1	1	1

TFP501 OUTPUT DRIVER CONFIGURATIONS

The TFP501 provides flexibility by offering various output driver features that can be used to optimize power consumption, ground-bounce and power-supply noise. The following sections outline the output driver features and their effects.

Output driver power down ($\overline{PDO}$ = low.) Pulling $\overline{PDO}$ low places all the output drivers, except CTL1 and SCDT, into a high-impedance state. A weak pulldown (approximately 10 µA) gradually pulls these high-impedance outputs to a low level to prevent the outputs from floating. The SCDT output, which indicates link-disabled or link-inactive, can be tied directly to the $\overline{PDO}$ input to disable the output drivers when the link is inactive or when the cable is disconnected. An internal pullup on the $\overline{PDO}$ pin defaults the TFP501 to the normal nonpower-down output drive mode if left unconnected.

Drive Strength (ST = high for high drive strength, ST = low for low drive strength.) The TFP501 allows for selectable output drive strength on the data, control, and ODCK outputs. See the dc specifications table for the values of I_{OH} and I_{OL} current drives for a given ST state. The high output strength offers approximately two times the drive as the low output drive strength.

Time Staggered Pixel Output. This option works only in conjunction with the 2-pixel/clock mode (PIXS = high.) Setting $\overline{STAG}$ = low will time stagger the even and odd pixel output so as to reduce the amount of instantaneous current surge from the power supply. Depending on the PCB layout and design this can help reduce the amount of system ground bounce and power supply noise. The time stagger is such that in 2-pixel/clock mode the even pixel is delayed from the latching edge of ODCK by 0.25 $T_{(ODCK)}$. ($T_{(ODCK)}$ is the period of ODCK. The ODCK period is 2 $t_{(pixel)}$ when in 2-pixel/clock mode.)

Depending on system constraints of output load, pixel rate, panel input architecture, and board cost, the TFP501 drive strength and staggered pixel options allow flexibility to reduce system power supply noise, ground bounce and EMI.

Power Management.

The TFP501 offers several system power management features. The output driver power down ($\overline{PDO}$ = low) is an intermediate mode which offers several uses. During this mode, all output drivers except SCDT and CTL1 are driven to a high-impedance state while the rest of the device circuitry remains active.

The TFP501 power down ($\overline{PD}$ = low) is a complete power down in that it powers down the digital core, the analog circuitry and output drivers. All output drivers are placed into a high-impedance state. All inputs are disabled except for the $\overline{PD}$ input. The TFP501 does not respond to any digital or analog inputs until $\overline{PD}$ is pulled high.

Both $\overline{PDO}$ and $\overline{PD}$ have internal pullups so if left unconnected they default the TFP501 to normal operating modes.

Sync Detect. The TFP501 offers an output, SCDT, to indicate link activity. The TFP501 monitors activity on DE to determine if the link is active. When 1 million pixel clock periods pass without a transition on DE, the TFP501 considers the link inactive and SCDT is driven low. SCDT goes high immediately after the first eight transitions on DE. SCDT again goes low when no more transitions are seen after 2^{18} oscillator clocks.

SCDT can be used to signal a system power management circuit to initiate a system power down when the link is considered inactive. The SCDT can also be tied directly to the TFP501 $\overline{PDO}$ input to power down the output drivers when the link is inactive. It is not recommended to use the SCDT to drive the $\overline{PD}$ input since, once in complete power down, the analog inputs are ignored and the SCDT state does not change. An external, system power management circuit to drive $\overline{PD}$ is preferred.

HDCP REGISTER MAP

TFP501 is a standard I^2C slave device. All the registers can be written and read through the I^2C interface. The I^2C base address of TFP501 is dependent on pin 10 (A0) as shown below.

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Pin 10	Write Address (Hex)	Read Address (Hex)
0	74	75
1	76	77

I²C Register Map

BKSV **Subaddress = 00** **Read Only**

7	6	5	4	3	2	1	0
BKSV[7:0]							

Subaddress = 01 **Read Only**

7	6	5	4	3	2	1	0
BKSV[15:8]							

Subaddress = 02 **Read Only**

7	6	5	4	3	2	1	0
BKSV[23:16]							

Subaddress = 03 **Read Only**

7	6	5	4	3	2	1	0
BKSV[31:24]							

Subaddress = 04 **Read Only**

7	6	5	4	3	2	1	0
BKSV[39:32]							

Video receiver KSV. This value may be used to determine that the video receiver is HDCP capable. Valid KSVs contain 20 ones and 20 zeros, a characteristic that is verified by video transmitter hardware before encryption is enabled.

Ri' **Subaddress = 08** **Read Only**

7	6	5	4	3	2	1	0
Ri'[7:0]							

Subaddress = 09 **Read Only**

7	6	5	4	3	2	1	0
Ri'[15:8]							

Link verification response. Updated every 128th frame. It is recommended that graphics systems protect against errors in the I²C transmission by re-reading this value when unexpected values are received. This value is available at all times between updates.

AKSV **Subaddress = 10** **Read/Write** **Default = 00**

7	6	5	4	3	2	1	0
AKSV[7:0]							

Subaddress =11 **Read/Write** **Default = 00**

7	6	5	4	3	2	1	0
AKSV[15:8]							

Subaddress = 12 **Read/Write** **Default = 00**

7	6	5	4	3	2	1	0
AKSV[23:16]							

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	Subaddress =13		Read/Write		Default = 00		
7	6	5	4	3	2	1	0
AKSV[31:24]							

	Subaddress = 14		Read/Write		Default = 00		
7	6	5	4	3	2	1	0
AKSV[39:32]							

Video transmitter KSV. Writing to 0x14 triggers the authentication sequence in the device.

An	Subaddress = 18		Read/Write		Default = 00		
7	6	5	4	3	2	1	0
An[7:0]							

	Subaddress =19		Read/Write		Default = 00		
7	6	5	4	3	2	1	0
An[15:8]							

	Subaddress = 1A		Read/Write		Default = 00		
7	6	5	4	3	2	1	0
An[23:16]							

	Subaddress =1B		Read/Write		Default = 00		
7	6	5	4	3	2	1	0
An[31:24]							

	Subaddress = 1C		Read/Write		Default = 00		
7	6	5	4	3	2	1	0
An[39:32]							

	Subaddress = 1D		Read/Write		Default = 00		
7	6	5	4	3	2	1	0
An[47:40]							

	Subaddress =1E		Read/Write		Default = 00		
7	6	5	4	3	2	1	0
An[55:48]							

	Subaddress = 1F		Read/Write		Default = 00		
7	6	5	4	3	2	1	0
An[63:56]							

Session random number. This multibyte value must be written by the graphics system before the KSV is written.

Bcaps	Subaddress = 40		Read Only		Default = 10		
7	6	5	4	3	2	1	0
Rsvd	Repeater	KSV-FIFO	Fast	Rsvd	Rsvd	Rsvd	Rsvd

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Bit 6: REPEATER, Video repeater capability. This device is not a repeater. Read as ZERO.

Bit 5: READY, KSV FIFO ready. This device does not support repeater capability. Read as ZERO.

Bit 4: FAST. This device supports 400 kHz transfers. Read as ONE.

Bstatus	**Subaddress = 41**		**Read Only**			**Default = 00**	
7	6	5	4	3	2	1	0
Bstatus[7:0]							

	Subaddress = 42		**Read Only**			**Default = 00**	
7	6	5	4	3	2	1	0
Bstatus[15:8]							

Bstatus. This device does not support repeater capability. All bytes read as 0x00.

KSV_FIFO	**Subaddress = 43**		**Read Only**			**Default = 00**	
7	6	5	4	3	2	1	0
KSV_FIFO							

Key selection vector FIFO. This device is not a repeater. All bytes read as 0x00.

VEN_ID	**Subaddress = C0**		**Read Only**			**Default = 4C**	
7	6	5	4	3	2	1	0
VEN_ID[7:0]							

	Subaddress = C1		**Read Only**			**Default = 01**	
7	6	5	4	3	2	1	0
VEN_ID[15:8]							

This read-only register contains the 16-bit Texas Instruments vendor ID for the TFP501. VEN_ID[15:0] is hardwired to 0x014C

DEV_ID	**Subaddress = C2**		**Read Only**			**Default = 01**	
7	6	5	4	3	2	1	0
DEV_ID[7:0]							

	Subaddress = C3		**Read Only**			**Default = 05**	
7	6	5	4	3	2	1	0
DEV_ID[15:8]							

This read-only register contains the 16-bit device ID for the TFP501. DEV_ID[15:0] is hardwired to 0x0501.

REV_ID	**Subaddress = C4**		**Read Only**			**Default = 01**	
7	6	5	4	3	2	1	0
REV_ID[7:0]							

This read-only register contains the 8-bit revision ID for the TFP501. REV_ID[7:0] is hardwired to 0x01.

I²C INTERFACE

The I²C interface is used to access the internal TFP501 registers. This two-pin interface consists of one clock line, DDC_SCL, and one serial data line, DDC_SDA. The basic I2C access cycles are shown in Figure 16 and Figure 17.

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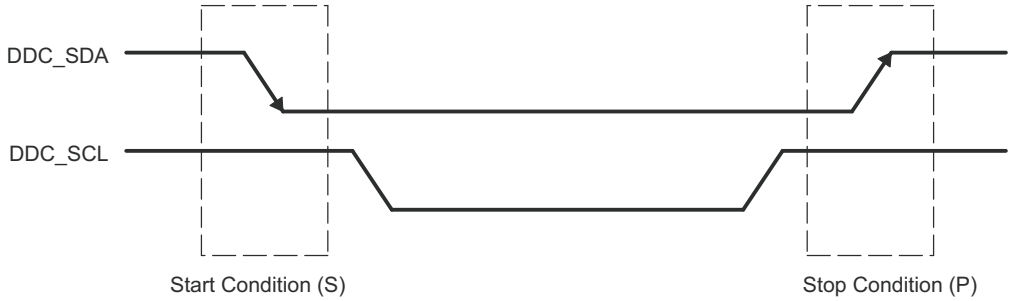


Figure 16. I²C Start and Stop Conditions

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- A subaddress cycle
- Any number of data cycles
- A stop condition

The start and stop conditions are shown in Figure 16. The high to low transition of DDC_SDA while DDC_SCL is high defines the start condition. The low to high transition of DDC_SDA while DDC_SCL is high defines the stop condition. Each cycle, (data or address) consists of 8 bits of serial data followed by one acknowledge bit generated by the receiving device. Thus, each data/address cycle contains 9 bits as shown in Figure 17.

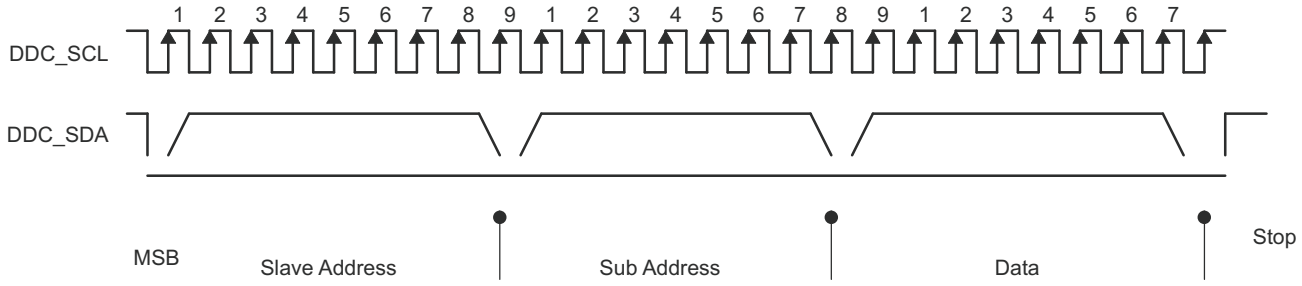


Figure 17. I²C Access Cycles

Following a start condition, each I²C device decodes the slave address. The TFP501 responds with an acknowledge by pulling the DDC_SDA line low during the ninth clock cycle if it decodes the address as its address. During subsequent subaddress and data cycles the TFP501 responds with acknowledge as shown in Figure 18. The subaddress is autoincremented after each data cycle.

The transmitting device must not drive the DDC_SDA signal during the acknowledge cycle so that the receiving device may drive the DDC_SDA signal low. The not acknowledge, A, condition is indicated by the master by keeping the DDC_SDA signal high just before it asserts the stop, P, condition. This sequence terminates a read cycle as shown in Figure 19.

The slave address consists of 7 bits of address along with 1 bit of read/write information as shown below in Figure 18, Figure 19, and Figure 20. For the TFP501, the possible slave addresses (including the r/w bit) are 0x74, 0x76 for write cycles and 0x75 and 0x77 for read cycles. Refer to the register description section for additional base address information.

In order to minimize the number of bits that must be transferred for the link integrity check, a second read format is supported. This format, shown in Figure 20, has an implicit subaddress equal to 0x08, the starting location of R_i'.

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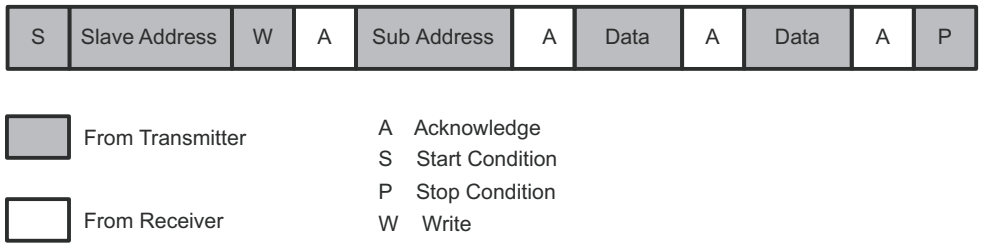


Figure 18. I²C Write Cycle

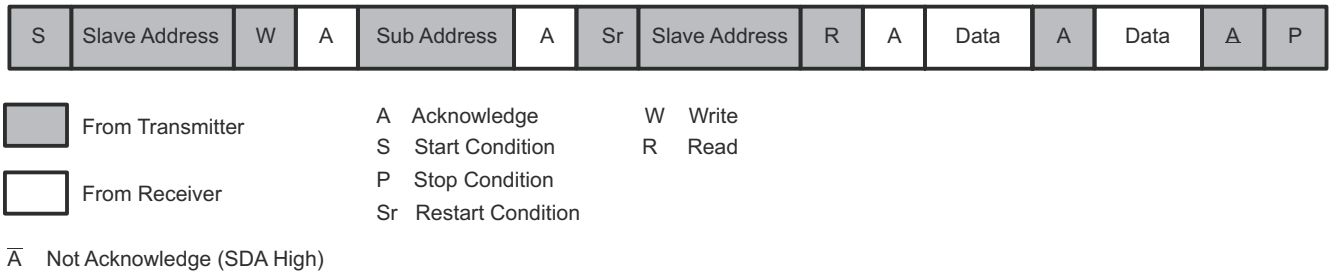


Figure 19. I²C Read Cycle

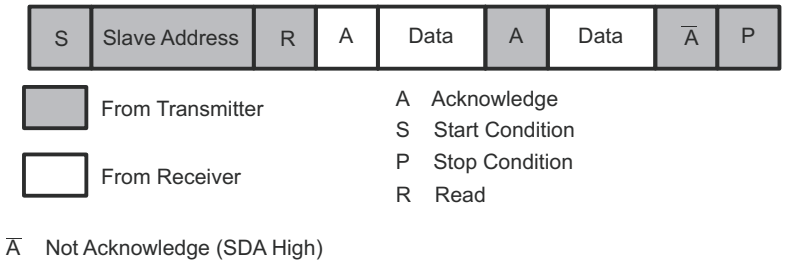


Figure 20. HDCP Port Link Integrity Message Read

PowerPAD™ 100-Pin TQFP PACKAGE

The TFP501 is packaged in TI's thermally enhanced PowerPAD 100-pin TQFP packaging. The PowerPAD package is a 14 mm y 14 mm y 1 mm TQFP outline with 0.5mm lead-pitch. The PowerPAD package has a specially designed die mount pad that offers improved thermal capability over typical TQFP packages of the same outline. The TI 100-pin TQFP PowerPAD package offers a backside solder plane that connects directly to the die mount pad for enhanced thermal conduction. Soldering the backside of the TFP501 to the application board is not required thermally, as the device power dissipation is well within the package capability when not soldered.

Soldering the backside of the device to the PCB ground plane is recommended for electrical considerations. Since the die pad is electrically connected to the chip substrate and hence chip ground, connection of the PowerPAD back side to a PCB ground plane helps to improve EMI, ground bounce, and power supply noise performance.

Table 1 outlines the thermal properties of the TI 100-pin TQFP PowerPAD package. The 100-pin TQFP non-PowerPAD package is included only for reference.

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Table 1. TI 100-TQFP (14 × 14 × 1 mm)/0.5 mm Lead Pitch

PARAMETER		WITHOUT PowerPAD™	PowerPAD™ NOT CONNECTED TO PCB THERMAL PLANE	PowerPAD™ CONNECTED TO PCB THERMAL PLANE(1)
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)(2)	49.17°C/W	27.32°C/W	17.28°C/W
$R_{\theta Jc}$	Junction-to-case thermal resistance (1)(2)	3.11°C/W	0.12°C/W	0.12°C/W
P_D	Package power dissipation (1)(2)(3)	1.6 W	2.9 W	4.6 W

(1) Specified with the PowerPAD bond pad on the backside of the package soldered to a 2 oz Cu plate PCB thermal plane.
(2) Airflow is at 0 LFM (no airflow)
(3) Specified at 150°C junction temperature and 70°C ambient temperature.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TFP501PZP	ACTIVE	HTQFP	PZP	100		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TFP501PZP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

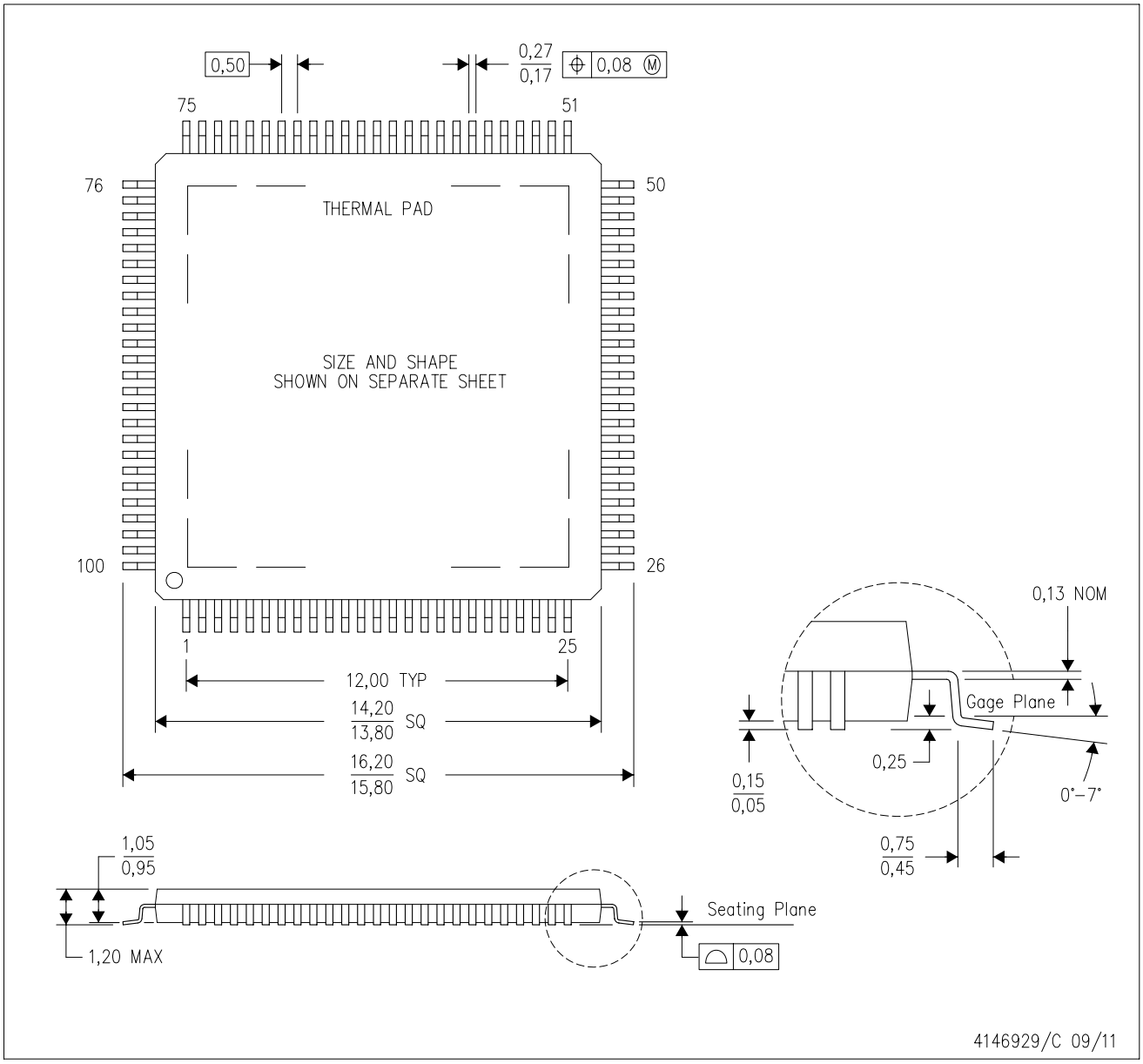
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

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