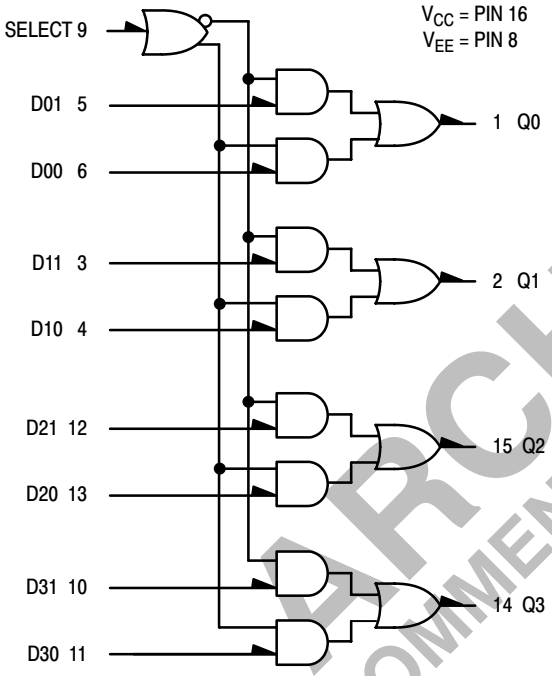
MC10158

Quad 2-Input Multiplexer
(Non–Inverting)

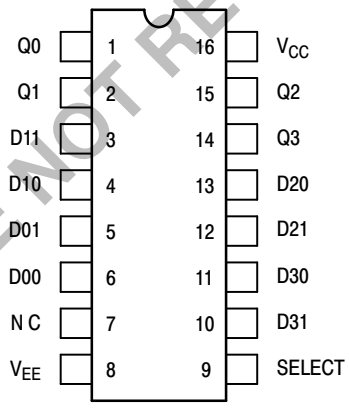
The MC10158 is a quad two channel multiplexer. A common select input determines which data inputs are enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, and D31.

- P_D=197 mW typ/pkg (No Load)
- t_{pd}=2.5 ns typ (Data to Q)
- 3.2 ns typ (Select to Q)
- t_r, t_f=2.5 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT

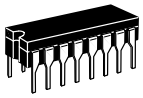


Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

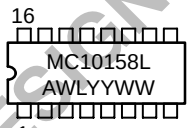
ON Semiconductor

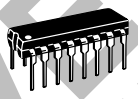
http://onsemi.com

MARKING DIAGRAMS

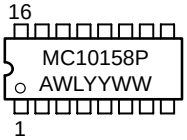


CDIP–16
L SUFFIX
CASE 620



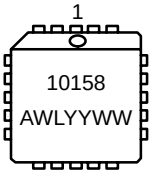


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

TRUTH TABLE

Select	D0	D1	Q
L	X	L	L
L	X	H	H
H	L	X	L
H	H	X	H

ORDERING INFORMATION

Device	Package	Shipping
MC10158L	CDIP–16	25 Units / Rail
MC10158P	PDIP–16	25 Units / Rail
MC10158FN	PLCC–20	46 Units / Rail

ARCHIVE
DEVICE NOT RECOMMENDED FOR NEW DESIGN

© Semiconductor Components Industries, LLC, 2002

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Pin Under Test	Test Limits							Unit
				–30°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current		I_E	8		53		38	48		53	mAdc
Input Current		I_{inH}	9 5		360 400			225 250		225 250	μAdc
		I_{inL}	5	0.5		0.5			0.3		μAdc
Output Voltage	Logic 1	V_{OH}	1	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage	Logic 0	V_{OL}	1	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage	Logic 1	V_{OHA}	1	–1.080		–0.980			–0.910		Vdc
Threshold Voltage	Logic 0	V_{OLA}	1		–1.655			–1.630		–1.595	Vdc
Switching Times (50Ω Load)											ns
Propagation Delay	Data Input	t_{5-1-}	1	1.3	3.1	1.2	2.5	3.0	1.3	3.2	
	Select Input	t_{9+1+}	1	2.5	4.8	2.4	3.2	4.5	2.5	4.8	
Rise Time	(20 to 80%)	t_{1+}	1	1.6	3.4	1.5	2.5	3.3	1.6	3.4	
Fall Time	(20 to 80%)	t_{1-}	1	1.6	3.4	1.5	2.5	3.3	1.6	3.4	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts)					
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

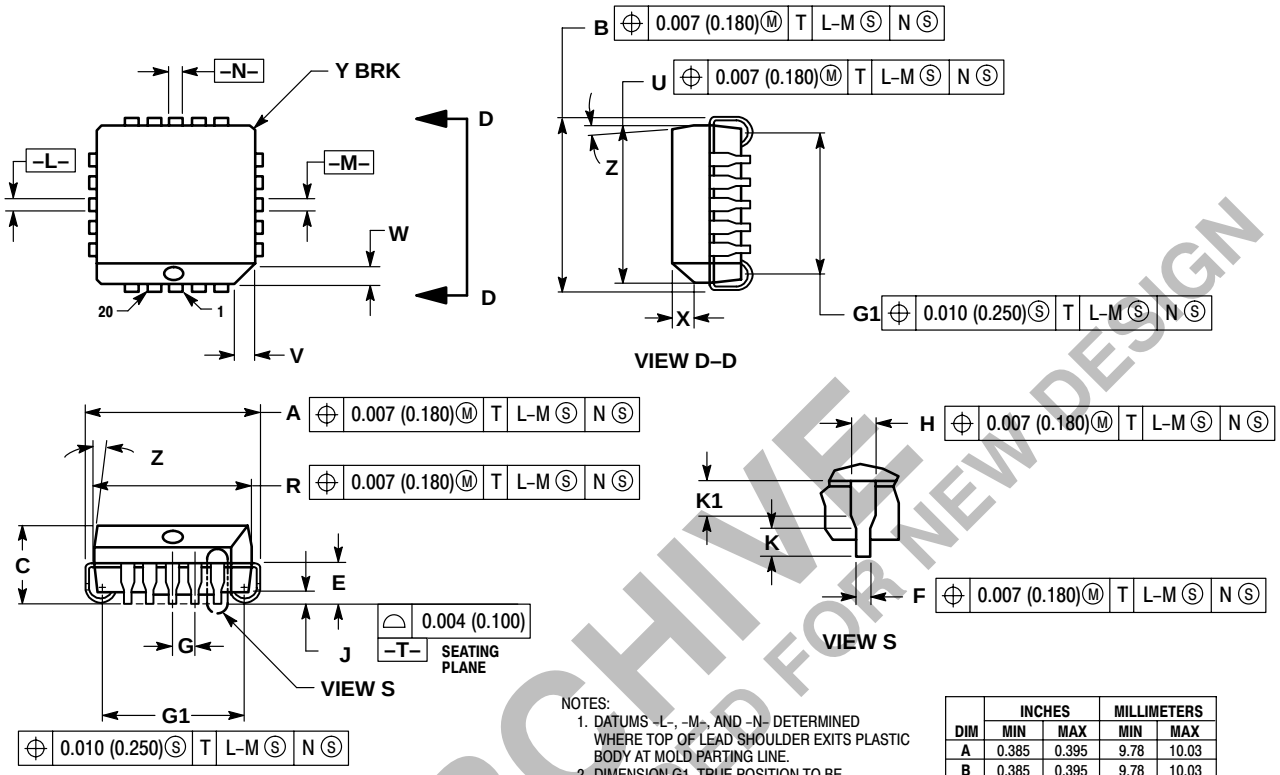
Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	16
Input Current		I_{inH}	9 5	9 5				8 8	16 16
		I_{inL}	5		5			8	16
Output Voltage	Logic 1	V_{OH}	1	5				8	16
Output Voltage	Logic 0	V_{OL}	1					8	16
Threshold Voltage	Logic 1	V_{OHA}	1			5		8	16
Threshold Voltage	Logic 0	V_{OLA}	1				5	8	16
Switching Times	(50Ω Load)			**+1.11V**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	Data Input	t_{5-1-}	1			5	1	8	16
	Select Input	t_{9+1+}	1	6		9	1	8	16
Rise Time	(20 to 80%)	t_{1+}	1			5	1	8	16
Fall Time	(20 to 80%)	t_{1-}	1			5	1	8	16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

ARCHIVE
DEVICE NOT RECOMMENDED FOR NEW DESIGN

PACKAGE DIMENSIONS

PLCC–20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C

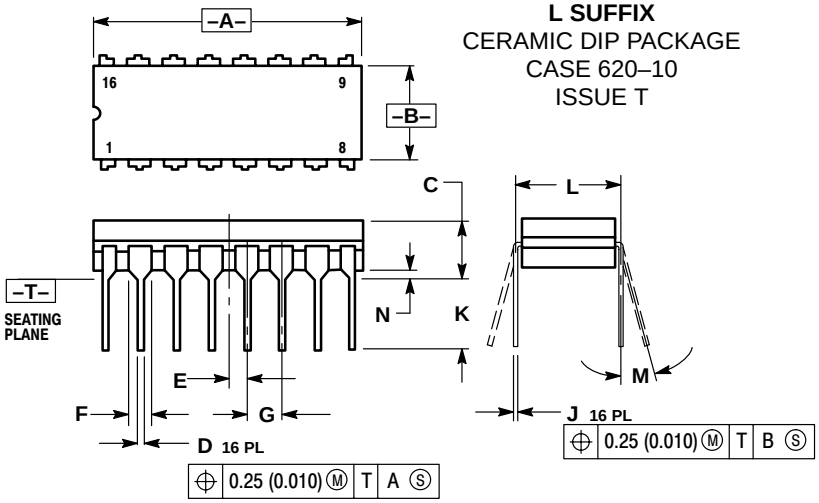


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

ARCHIVE
DEVICE NOT RECOMMENDED FOR NEW DESIGN

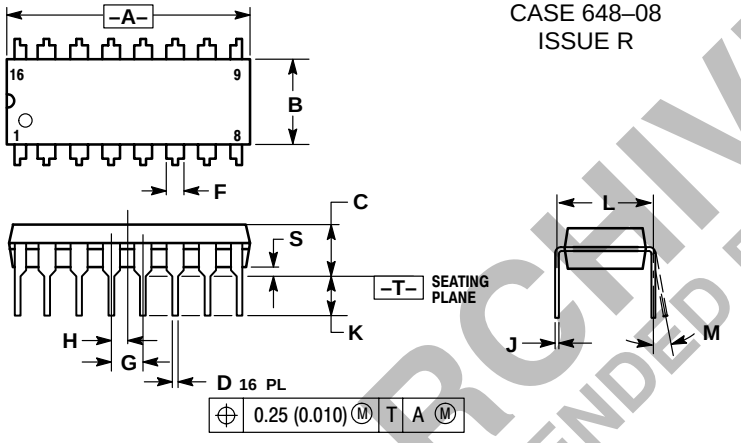
CDIP–16
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

ARCHIVE
NOT RECOMMENDED FOR NEW DESIGN

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.