16-bit, 100kHz Sampling A/D Converter

FEATURES

- 16-Bit No-Missing Codes
- 100kHz Sampling Rate
- Self Calibration
- Inherent T/H Function
- Serial Output Port
- Small 24-Pin DIP
- Low Power
- Sleep Mode
- Four User-Selectable Input Ranges
- Serial Data Clock Output
- ±12 to 15V, +5V Supplies
- Optional Environmental Stress Screening

DESCRIPTION

The MN6500 is a 16-bit, 100kHz Sampling A/D converter complete with internal reference, inherent sampling function and analog input amplifier. Self-calibration ensures ±0.0015%FSR integral linearity error and 16-bits no-missing-codes over the specified temperature range. Output data is provided in a serial format during the conversion or can be clocked from the device upon completing the conversion. Each device is fully tested using contemporary FFT (Fast Fourier Transform) technology guaranteeing frequency-domain performance.

The MN6500 offers four analog input ranges (0 to +5V, 0 to +10V, ±5V and ±10V) whose bipolar and unipolar operation is digitally controlled. Serial output data is provided via the serial output port and can be user configured to allow maximum system flexibility. Serial output clock is also provided to facilitate reading output data.

Packaged in a small 24-pin hermetically-sealed DIP package, the MN6500 only consumes 720mW when operating. While in the sleep mode, power consumption is reduced to 200mW. The MN6500 offers designers four electrical grades (J, K and S) and two operating temperature ranges (0°C to +70°C and −55°C to +125°C). In addition, S models are available with Environmental Stress Screening.

APPLICATIONS

Test and Measurement
Weights and Measures
P.C. Based Data Acquisition
Robotics and Motion Control
Geophysical and Seismic
Fire and Control Systems
System ATE
Analyzers

MN6500 100kHz 16-Bit, A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	−55°C to +125°C
Specified Temperature Range:	
MN6500J, K	0°C to +70°C
MN6500S	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 23)	−0 to +16.5 Volts
−15V Supply (−V_{CC}, Pin 24)	−0 to −16.5 Volts
Digital Inputs (Pins 5, 6, 8, 9, 12, 13, 15, 16, 17)	−0.3 to +V_{DD} +0.3 Volts
Analog Input (Pins 18, 19)	±V_{CC}

ORDERING INFORMATION

PART NUMBER **MN6500 S/B**

Select J, K, or S for desired performance and temperature range.
Add "/B" to "S" and "T" models for Environmental Stress Screening

DESIGN SPECIFICATIONS ALL UNITS (Typical at T_A = +25°C, ±V_{CC} = ±15V, +V_{DD} = +5V, f_{CLK} = 8 MHz unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: 5V (Pin 19 in) 10V (Pin 18 in)		0 to +5, ±5 0 to +10, ±10		Volts Volts
Input Impedance: 5V Input (Pin 19 in) 10V Input (Pin 18 in)		5 10		kOhm kOhm
DIGITAL INPUTS				
Logic Levels: Logic "1" Logic "0"	+2.0		 +0.8	Volts Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V) Logic "0" (V_{IL} = +0.4V)			±10 ±10	μA μA
DIGITAL OUTPUTS				
Logic Levels: Logic "1" (I_{OH} = −40μA) Logic "0" (I_{OL} = +1.6μA)	+2.4		 +0.4	Volts Volts
INTERNAL REFERENCE				
Reference Output: Voltage (Note 2) Drift (Note 2)	+4.45	+4.5 ±10	+4.55	Volts ppm/°C
POWER SUPPLY REQUIREMENTS				
Power Supply Range: (±V_{CC} Supply) (+V_{DD} Supply)	±14.5 +4.5	±15 +5	±15.5 +5.5	Volts Volts
Power Supply Rejection: (±V_{CC} Supply) (+V_{DD} Supply)		+0.001 ±0.001	±0.01 ±0.01	%FSR/%VS %FSR/%VS
Current Drains: +V_{CC} Supply −V_{CC} Supply +V_{DD} Supply		+6 −33 +27	+10 −50 +35	mA mA mA
Power Consumption		720	1075	mW

SPECIFICATION NOTES:

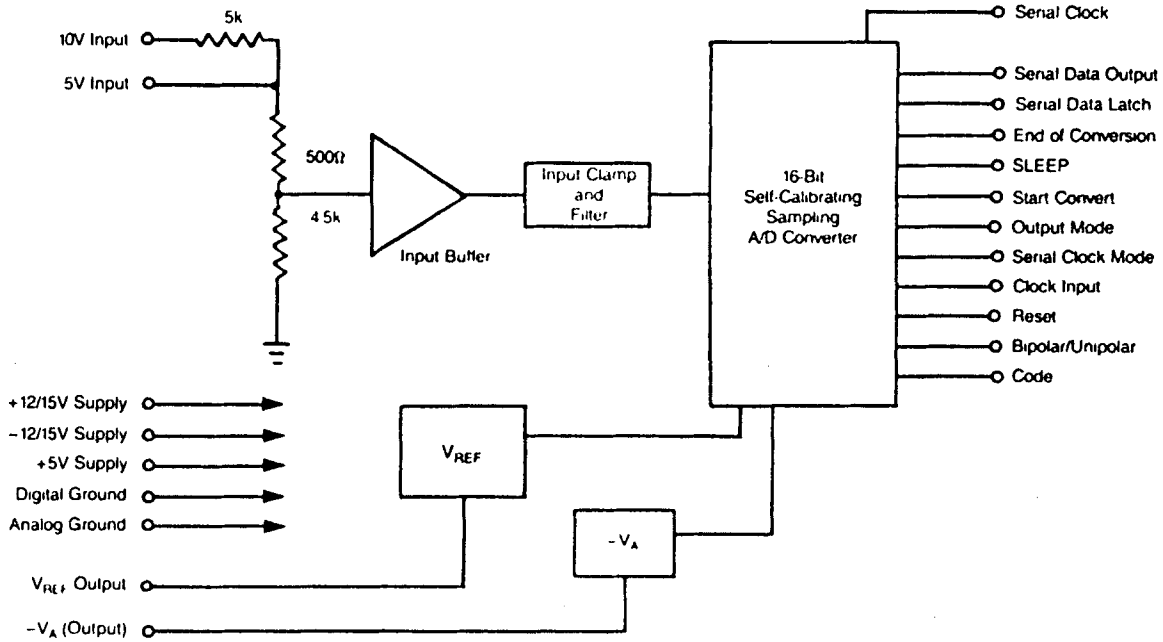
1. Specifications apply after calibration following power-up at +25°C
2. Reference output is to be bypassed to Analog Ground with a 10μF capacitor in parallel with a 0.1μF capacitor. Reference must not be used for applications circuitry without buffering
3. Specification listed applies after calibration at any temperature within specified temperature range.
4. Specification listed applies over the specified temperature range after initial calibration at 25°C.
5. The MN6500J,K is fully specified for 0°C to +70°C operation
   The MN6500S,T is fully specified for −55°C to +125°C operation.

PERFORMANCE CHARACTERISTICS (Typical at T_A = +25°C, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, f_{CLK} = 8 MHz unless otherwise indicated. (Note 1)

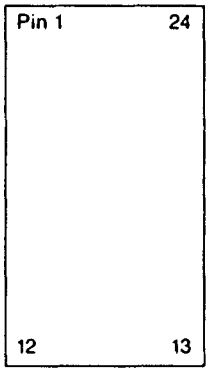
STATIC CHARACTERISTICS	MN6500J	MN6500K	MN6500S	UNITS
Integral Linearity Error (Max) (Note 1)	±0.0022	±0.0015	±0.0022	%FSR
No Missing Codes @ 25°C Over Temperature	15 14	16 15	15 14	Bits Bits
Zero Error @ 25°C (Max) @Temp (Max) Drift	±0.03 ±0.05 ±1	±0.02 ±0.03 ±0.05	±0.03 ±0.07 ±1	%FSR %FSR ppm of FSR/°C
Full Scale Absolute Accuracy: @ 25°C (Max) @ Temp (Max) Drift	±0.1 ±0.17 10	±0.05 ±0.1 5	±0.1 ±0.25 10	%FSR %FSR ppm of FSR/°C
DYNAMIC CHARACTERISTICS				
Minimum Sampling Rate Max A/D Conversion Time	100 8.12	100 8.12	100 8.12	kHz µsec
Signal-to-(Noise+Distortion) f_{AIN} = 1kHz (Min) f_{AIN} = 24kHz (Min)	84 76	86 78	84 76	dB dB
Harmonics and Spurious Noise: f_{AIN} = 1kHz (Min) f_{AIN} = 24kHz (Min)	−92 −84	−94 −86	−92 −84	dB dB

Note 1. After calibration at operating temperature.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Analog Ground	24	$-V_{CC}$ Supply (−15V)
2	Analog Ground	23	$+V_{CC}$ Supply (+15V)
3	$+V_A$ Supply (+5V Analog)	22	$-V_A$ Supply (−5V Output)
4	Reference Output	21	$-V_A$ Supply (−5V Ouput)
5	Serial Clock Mode Input	20	Analog Ground
6	Sleep Mode	19	5V Analog Input
7	End of Conversion (E.O.C)	18	10V Analog Input
8	Reset	17	Bipolar/Unipolar
9	Clock Input	16	Data Output Mode Input
10	Digital Ground	15	Code Input
11	Serial Data Latch	14	Serial Data Output
12	Start Convert	13	Serial Clock

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION — The MN6500 is a 16-bit Sampling A/D converter containing an inherent, user transparent, T/H function and features self calibration, a user configurable serial data output port, four user selectable analog input ranges, and a serial data clock output. The MN6500's low power consumption of only 685mW along with its ability to be able to be switched to "sleep mode" make it an excellent choice for battery powered applications. Self-calibration and the inherent T/H function enable the MN6500 to accurately sample and digitize dynamically changing analog input signals at a 100kHz throughput rate

The MN6500 is designed to operate from ±12V or ±15V and +5V power supplies and an externally generated Master Clock. The MN6500 must be reset on power-up by bringing Reset (pin 8) from high to low and then high again. When Reset is brought low (for a minimum of 150nSec) all internal logic in the device is cleared. Upon Reset's return high a calibration cycle begins which takes 11,528,160 master clock cycles to complete (1.4 seconds with an 8MHz master clock). While in calibration, the MN6500 will ignore any changes to the Start Convert Input (pin 12). When the MN6500 is placed in the Sleep Mode (pin 6 low) it retains its calibration in memory and does not require recalibration once normal operation is resumed.

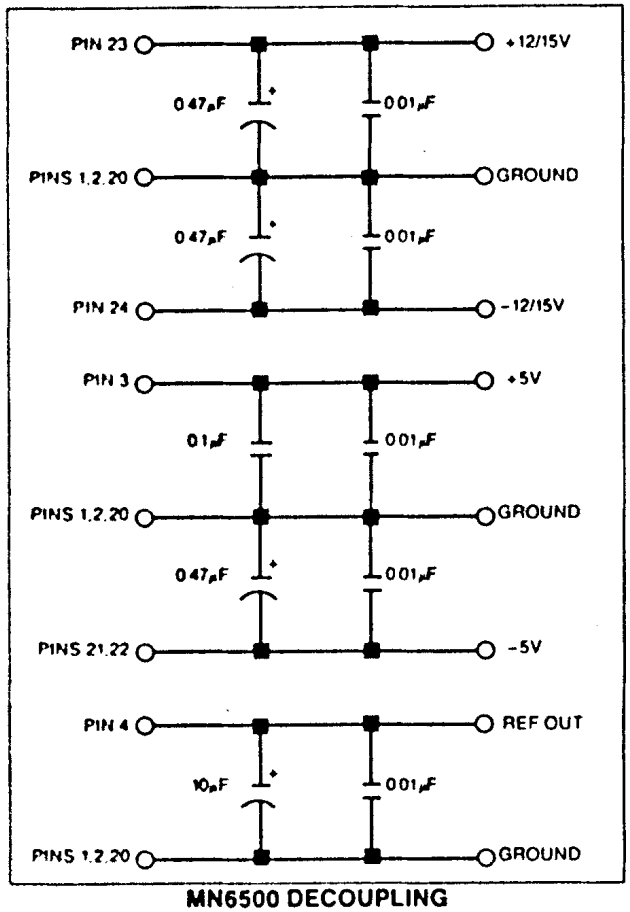
After calibration, conversions can be initiated by the falling edge of Start Convert. The signal applied to Start Convert (pin 12) must remain low for a minimum of one Master Clock cycle plus 20nSec but no longer than the minimum conversion time minus two master clock cycles or an additional conversion cycle will be initiated with an inadequate acquisition time. The MN6500 will complete conversion of the sample within 66 master clock cycles and then return to the track mode. When operating in Free Run Mode, Start convert is disabled and should be tied to DGND or +5V.

With the conversion complete the serial data output (pin 14), the serial clock (pin 13), and the serial data latch (pin 11) can be configured in three different output modes (PDT, RBT, SSC), as well as an internal, synchronous loopback mode (FRN).

POWER SUPPLIES AND LAYOUT — The MN6500 is powered from standard supply voltages of +12/15V (pin 23), −12/15V (pin 24), and +5V (pin 3). The analog ground (pins 1,2,20) and digital ground (pin 10) are separated to minimize analog and digital circuit interaction. These grounds should be tied together as close to the unit as possible, and connected to system analog ground, preferably through a large low-impedance ground plane beneath the package. The analog ground is internally used as a reference point, therefore it should be used as the system analog ground reference point. Care must be taken to reduce the system noise to a level below the MN6500's high-resolution conversion capability.

It is recommended that the power supplies be decoupled in the following manner. The +12/15V and −12/15V supplies should be bypassed with a 0.01μF capacitor in parallel with a 0.47μF capacitor to analog ground. The +5V supply, which powers both analog and digital internal circuitry, should be bypassed with a 0.1μF capacitor in parallel with a 0.01μF capacitor to analog ground. The optimum value decoupling capacitors to use may vary depending on the users system noise characteristics.

A −5V analog supply is created internal to the MN6500 and brought out to pins 21 and 22 for bypassing. It is recommended that these pins be bypassed with a 0.01μF capacitor in parallel with a 0.47μF capacitor.



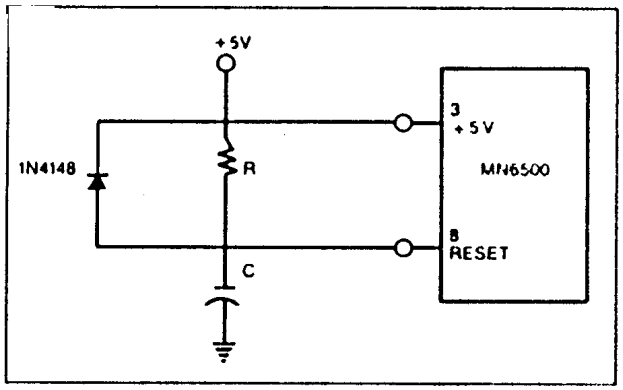
MN6500 DECOUPLING

REFERENCE OUTPUT — The MN6500 contains an internal +4.5V low-drift, precision reference. This reference voltage appears at Reference Output (pin 4) to allow for external attachment of a 0.01μF capacitor in parallel with a 10μF tantalum capacitor. These capacitors allow the reference to exhibit low output impedance throughout the frequency range of the devices operation. The optimum value of these capacitors will vary with the frequency of the Master Clock. It is recommended that the Reference Output not be used for any additional system requirements without the use of an external buffer and only if absolutely necessary.

CALIBRATION — The MN6500 must be reset upon power up in order to guarantee a consistent starting condition and initially calibrate the device. To perform the reset function, a simple power-on reset circuit can be built using a resistor and capacitor as shown below. The resistor should be less than or equal to 10k. The system power supplies and clock should be established prior to Reset rising.

The MN6500 must be reset by bringing Reset (pin 8) from high to low and then high again. When Reset is brought low (for a minimum of 150nSec) all internal logic in the device is cleared. Upon Reset's return high a calibration cycle begins which takes 11,528,160 master clock cycles to complete (1.4 seconds with an 8MHz master clock). While in

calibration, the MN6500 will ignore any changes to the Start Convert Input (pin 12). When the MN6500 is placed in the Sleep Mode (pin 6 low) it retains its calibration in memory and does not require recalibration once normal operation is resumed.



MN6500 RESET

MASTER CLOCK — Calibration and conversion times are directly related to the frequency of the Master Clock. The MN6500 can operate with a clock frequency of up to 9 216 MHz (8 MHz in FRN mode) allowing a maximum conversion rate of 100kHz. A CMOS compatible clock is recommended.

INITIATING CONVERSIONS — A falling transition on the Start Convert pin (pin 12) places the input in the Hold mode and begins the conversion cycle. The analog input is frozen on the internal capacitor array the instant Start Convert goes low. The MN6500 will complete its conversion of this frozen input within 66 master clock cycles and then return to the track mode. After allowing sufficient time for acquisition the device can begin another conversion. The MN6500 requires 6 master clock cycles for signal acquisition.

Unlike systems with separate track-and-holds and A/D converters, a sampling clock can be easily connected to the Start Convert Input. The duty cycle of this clock is not significant. The Start Convert input is latched internally by the master clock, so a minimum pulse low time of only 1/clk + 20nSec is required. If Start Convert remains low longer than the minimum conversion time minus two master clock cycles, an additional conversion cycle will be initiated without allowing adequate time for signal acquisition. In Free Run mode (see section on Digital Output Mode selection) the MN6500 will convert at a rate of Clk/80 and the Start Convert input is ignored.

Although the MN6500 can be operated asynchronous to the master clock if necessary, it is considered good practice to synchronize sampling to the master clock in order to minimize the effects of clock feedthrough.

ANALOG INPUT RANGE SELECTION — The MN6500 can be digitally configured to accept the following analog input ranges:

0V to +5V
0V to +10V
−5V to +5V
−10V to +10V

When pin 17 is low the MN6500 will accept unipolar inputs. When pin 17 is high the MN6500 will accept bipolar inputs.

Pin 19 is the 5V input.

Pin 18 is the 10V input.

PIN CONNECTIONS	ANALOG INPUT VOLTAGE RANGE			
	0 to +5V	0 to +10V	±5V	±10V
Connect pin 19 to	Analog Input	Open	Analog Input	Open
Connct pin 18 to	Open	Analog Input	Open	Analog Input
Connect pin 17 to Logic	"0"	"0"	"1"	"1"

INPUT RANGE SELECTION

CODE INPUT is pin 15 Binary or 2's complement output.

OUTPUT MODE SELECTION — The MN6500 can be configured in three different output modes, as well as an internal, synchronous loop-back mode. The operating mode is selected by setting the states of the Serial Clock Mode Input (pin 5) and the Data Output Mode Input (pin 16). In all modes, serial data is output on the Serial Data Output (pin 14) starting with the MSB. The subsequent data bits are updated on the falling edge of the master clock.

When the Serial Clock Mode Input (pin 5) is high, the Serial Clock pin (pin 13) is an input, allowing data to be clocked out with an external serial clock at rates up to 5 MHz. Any additional clock edges after #16 will clock out logic 1's. A low level on pin 5 makes the Serial Clock pin (pin 13) an output and the converter clocks out each bit as it is determined at a rate of 1/4 the master clock speed. Table # shows the different states of the mode pins and the corresponding output modes.

MODE	SERIAL CLK MODE INPUT PIN 5	DATA OUT MODE INPUT PIN 16	SERIAL CLK PIN 13	START CONVT
PDT	1	1	INPUT	INPUT
RBT	1	0	INPUT	INPUT
SSC	0	1	OUTPUT	INPUT
FRN	0	0	OUTPUT	X

PDT = Pipelined Data Transmission
RBT = Registered Burst Transmission
SSC = Synchronous Self Clocking
FRN = Free-Run

PIPELINED DATA TRANSMISSION (PDT) — PDT mode is selected by tying both Serial Clock Mode (pin 5) and Output Mode (pin 13) high. In PDT mode, the Serial Clock mode pin is an input. Data is registered during conversion and output in the following conversion cycle. Start Convert (pin 12) must be brought low, initiating conversion, before data from the previous conversion is available on pin 14. If all data bits have not been clocked out before the next falling edge of Start Convert, data from the conversion will be lost A clock must be applied to pin 13, as previously mentioned, to extract the data.

REGISTERED BURST TRANSMISSION (RBT) — The RBT mode is selected by tying Serial Clock Mode (pin 5) high and Output Mode (pin 13) low. The Serial Clock Mode pin is an input, as in PDT mode, however data is available immediately following the conversion, and may be clocked out immediately after EOC (pin 7) goes low. The falling edge of the Start Convert signal clears the output buffer, losing any unread data. A new conversion may be initiated before all the data has been read if the unread data bits are unnecessary.

SYNCHRONOUS SELF CLOCKING (SSC) — The SSC mode is selected by tying Serial Clock Mode (pin 5) low and Output Mode (pin 13) high. In the SSC mode the Serial Clock pin is an output that clocks out each data bit as it is being converted. The Serial Clock output remains high between conversions and runs at a rate of 1/4 the master clock speed for 16 low pulses during a conversion. The Serial Data Latch output (pin 11) goes low with the first falling edge of the Serial Clock output (pin 13), and returns high after 2 master clock cycles after the last rising edge of Serial Clock. This signal frames the 16 output data bits and is useful for shift register or DSP serial port interfacing.

FREE RUN (FRN) — Free Run is the internal, synchronous loopback mode of operation. The FRN mode is selected by tying both Serial Clock Mode (pin 5) and Output Mode (pin 13) low. In the SSC mode the Serial Clock pin is an output and operates the same as in the SSC mode. In the Free Run mode the MN6500 initiates a new conversion every 80

MN6500 PIN DESCRIPTIONS

Pin Designation	Function
POWER SUPPLY CONNECTIONS	
PIN 1,2,20	ANALOG GROUND REFERENCE
PIN 10	DIGITAL GROUND
PIN 3	+VA SUPPLY (+5V) Positive analog and digital power supply. Device operates from nominal +5V. Decouple with 0.1μf capacitor in parallel with 0.01μf capacitor to analog ground.
PIN 21,22	–VA SUPPLY (–5V OUTPUT BROUGHT OUT FOR DECOUPLING ONLY) Decouple with 0.47μf capacitor in parallel with 0.01μf capacitor to analog ground.
PIN 23	+VCC (+12/15V) Positive analog power supply. Devices will operate from nominal +12V or +15V supplies. Decouple with 0.47μf capacitor in parallel with 0.01μf capacitor to analog ground.
PIN 24	–VCC (–12/15V) Negative analog power supply. Devices will operate from nominal –12V or –15V supplies. Decouple with 0.47μf capacitor in parallel with 0.01μf capacitor to analog ground.
ANALOG INPUTS	
PIN 18	10V ANALOG INPUT Analog input for 0 to +10V and ±10V ranges.
PIN 19	5V ANALOG INPUT Analog input for 0 To +5V and ±5V ranges.
ANALOG OUTPUTS	
PIN 4	REFERENCE OUTPUT Internal reference voltage is brought out to this pin for decoupling. Recommended decoupling is a 10μF tantalum capacitor in parallel with a 0.01μF capacitor.
DIGITAL OUTPUTS	
PIN 7	TEST POINT TP1
PIN 11	SERIAL DATA LATCH This output signal provides a convenient latch signal for the 16 output data bits. This signal can be used to control external serial to parallel latch circuitry.
PIN 13	SERIAL CLOCK Pin 13 is an output in SSC and FRN modes (pin 5 low). A serial clock is internally generated at a rate of 1/4 the master clock frequency and output on pin 13. When pin 5 is high pin 13 is an input (see digital input section).

Pin Designation	Function
PIN 14	SERIAL DATA OUTPUT Data bits are presented in an MSB first format on a falling edge of pin 13 (SERIAL CLOCK). Data is valid to be latched on the rising edge of SERIAL CLOCK.
DIGITAL INPUTS	
PIN 5	SERIAL CLOCK MODE INPUT Pin 13 (SERIAL CLOCK) is an input when pin 5 is high. Pin 13 (SERIAL CLOCK) is an output when pin 5 is low. Pin 5 is used in conjunction with pin 16 to select one of four output modes (PDT, RBT, SSC, FRN).
PIN 6	NOT SLEEP A logic 0 on pin 6 causes the MN6500 to enter a low power state of operation. Calibration is retained in memory. Pin6 should be at logic 1 for normal operation.
PIN 8	RESET Resets all internal digital logic when taken low. A full calibration sequence is initiated when pin 8 returns high. During calibration pin 12 (START CONVERT) will be ignored. The MN6500 must be reset upon power-up. The device may be reset (recalibrated) at any time.
PIN 9	CLOCK INPUT All conversions and calibrations are timed from a master clock which must be externally applied by driving pin 9 with a CMOS compatible clock.
PIN 12	START CONVERT A falling transition on pin 12 initiates a conversion. The Start Convert signal must return high before the conversion is complete.
PIN 13	SERIAL CLOCK Pin 13 is an input in PDT and RBT modes (pin 5 high). Serial data changes status on a falling edge of this input and is valid on a rising edge. When pin 5 is low, pin 13 is an output (see digital output section).
PIN 15	CODE INPUT Determines whether output data appears in 2's complement or binary format. High is 2's complement and low is binary.
PIN 16	DATA OUTPUT MODE INPUT Pin 16 is used with pin 5 to determine which of four output modes is desired (pipeline, burst, sync self-clk, free run).
PIN 17	BIPOLAR/NOT UNIPOLAR At logic 0 the MN6500 accepts a unipolar analog input At logic 1 the MN6500 accepts a bipolar analog input.

master clock cycles. The Start Convert input (pin 12) is disabled and should be tied to either +5V or DGND. The Serial Data Latch goes low synchronously with the first falling edge of the Serial Clock output (pin 13) and returns high 2 master clock cycles after the last rising edge of Serial Clock. This signal frames the 16 output data bits and is useful for shift register or DSP serial port interfacing.

SLEEP MODE — The MN6500 features a Sleep mode of operation which causes the device to dissipate very little power while maintaining its calibration factors in memory at times when the device is not sampling or converting. The device does not require a new calibration after a return from the sleep mode. The Sleep mode is activated by tying pin 6 low and inactivated by a high level at pin 6. The Sleep mode pin (pin 6) should be tied high for normal operation. In order to achieve minimum start up time after a return from sleep mode all power supplies should remain present on the device. If startup time is not a factor, as long as +5V (pin 3) remains at greater than +2.0V the MN6500 will retain its calibration factors in memory.

DIGITAL OUTPUT CODING

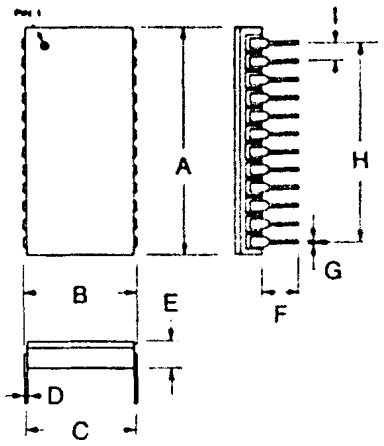
BINARY	0 to +5V	0 to +10V	±5V	±10V
MSB LSB				
1111 1111 1111 1111	+5.000000	+10.0000000	+5.0000000	+10.0000000
1111 1111 1111 111*	+4.9998900	+9.9997711	+4.9997711	+9.9995422
1000 0000 0000 000*	+2.5000382	+0.0000763	+0.0000763	+0.0001526
**** **** **** ****	+2.4999619	−0.0000763	−0.0000763	−0.0001526
0111 1111 1111 111*	+2.4998856	−0.0002289	−0.0002289	−0.0004578
0000 0000 0000 000*	+0.0000380	−9.9999237	−4.9999237	−9.9998474
0000 0000 0000 0000	0.0000000	−10.0000000	−5.0000000	−10.0000000

2's COMPLEMENT	0 to +5V	0 to +10V	±5V	±10V
MSB LSB				
0111 1111 1111 1111	+5.000000	+10.0000000	+5.0000000	+10.0000000
0111 1111 1111 111*	+4.9998900	+9.9997711	+4.9997711	+9.9995422
0000 0000 0000 000*	+2.5000382	+0.0000763	+0.0000763	+0.0001526
**** **** **** ****	+2.4999619	−0.0000763	−0.0000763	−0.0001526
1111 1111 1111 111*	+2.4998856	−0.0002289	−0.0002289	−0.0004578
1000 0000 0000 000*	+0.0000380	−9.9999237	−4.9999237	−9.9998474
1000 0000 0000 0000	0.0000000	−10.0000000	−5.0000000	−10.0000000

CODING NOTES:

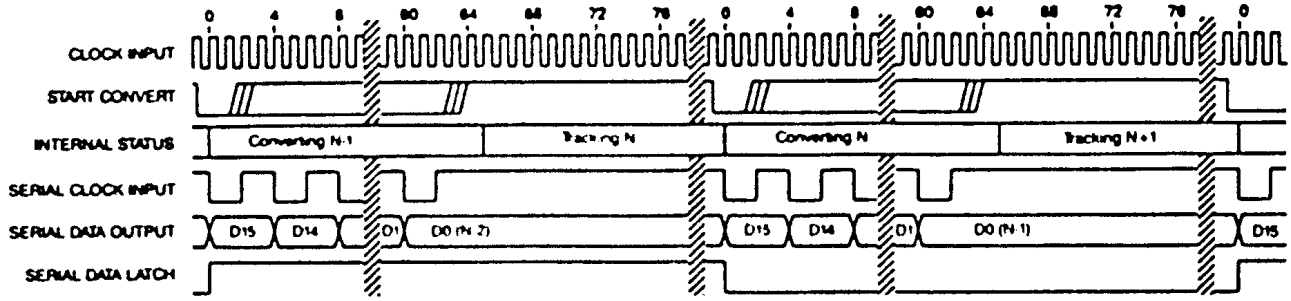
1. For 5 Volts FSR, 1 LSB for 16 Bits = 76.3μV.
2. For 10 Volt FSR, 1 LSB for 16 Bits = 152.6μV.
3. For 20 Volt FSR, 1 LSB for 16 Bits = 305.2μV.
4. For unipolar ranges, the coding is straight binary.
5. For bipolar ranges, the coding is offset binary.

24-PIN SIDE-BRAZED DIP

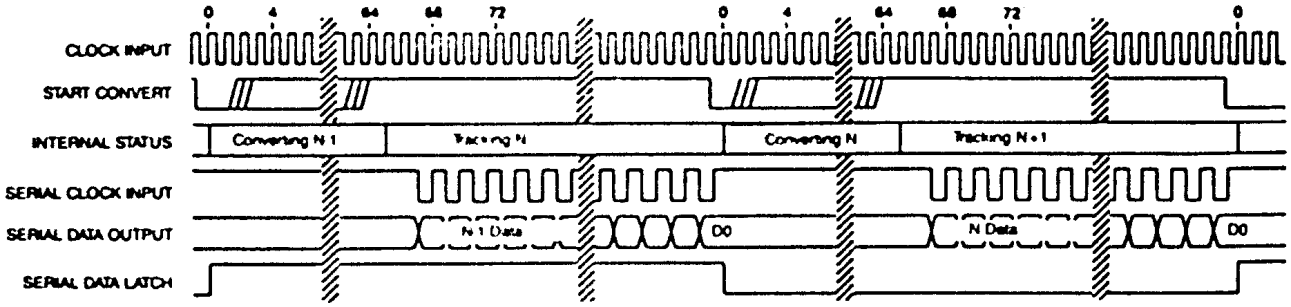


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.23	1.270	31.24	32.26
B	0.600	0.620	15.24	15.75
C	0.600 BASIC		15.24 BASIC	
D	0.008	0.012	0.20	0.30
E		0.183		4.65
F	0.175	0.205	4.45	5.21
G	0.015	0.019	0.38	0.48
H	1.100 BASIC		27.94 BASIC	
I	0.098	0.102	2.49	2.59

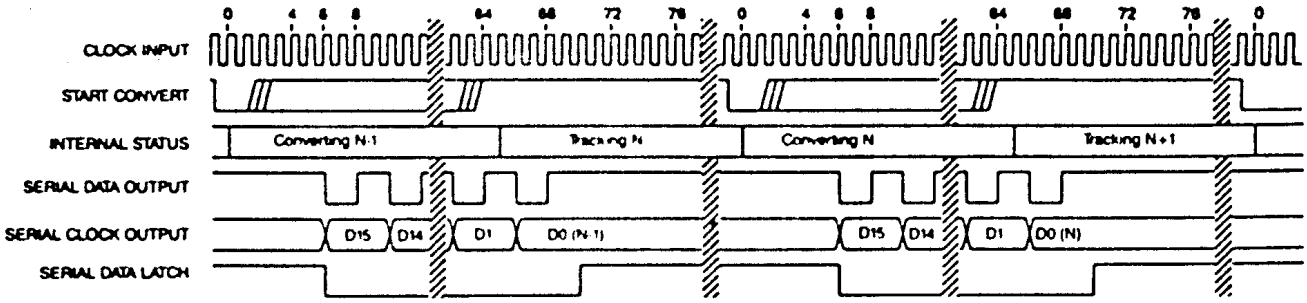
MODE A: PIPELINED DATA TRANSMISSION



MODE B: REGISTERED BURST TRANSMISSION



MODE C: SYNCHRONOUS SELF-CLOCKING



MODE D: FREE RUN

