LH168M

384-output TFT-LCD Source Driver IC

DESCRIPTION

The LH168M is a 384-output TFT-LCD source driver IC which can simultaneously display 262 144 colors in 64 gray scales.

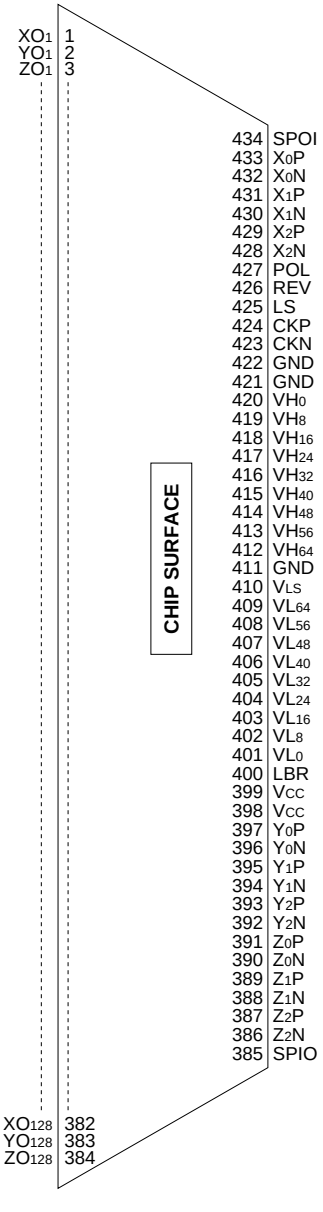
FEATURES

- Number of LCD drive outputs : 384
- Built-in 6-bit digital input DAC
- Dot-inversion drive : Outputs the inverted gray scale voltages between LCD drive pins next to each other
- RSDS™*(Reduced Swing Differential Signaling) input interface (Data and CK) : Possible to reduce Electro-Magnetic Interference (EMI)
- Possible to display 262 144 colors in 64 gray scales with reference voltage input of 18 gray scales : This reference voltage input corresponds to γ correction and intermediate reference voltage input can be abbreviated
- Cascade connection
- Sampling sequence :
  Output shift direction can be selected
  XO_1, YO_1, $ZO_1 \rightarrow XO_{128}$, YO_{128}, ZO_{128} or
  ZO_{128}, YO_{128}, $XO_{128} \rightarrow ZO_1$, YO_1, XO_1
- Shift clock frequency : 68 MHz (MAX.)
- Supply voltages
  – V_{CC} (for logic system) : +3.0 to +3.6 V
  – V_{LS} (for LCD drive system) : +12 V (MAX.)
- Package : 434-pin TCP (Tape Carrier Package)

* RSDS is a trademark of National Semiconductor Corporation. SHARP recommends FPD87310 of National Semiconductor Corporation as a timing controller for RSDS™.

PIN CONNECTIONS

434-PIN TCP TOP VIEW



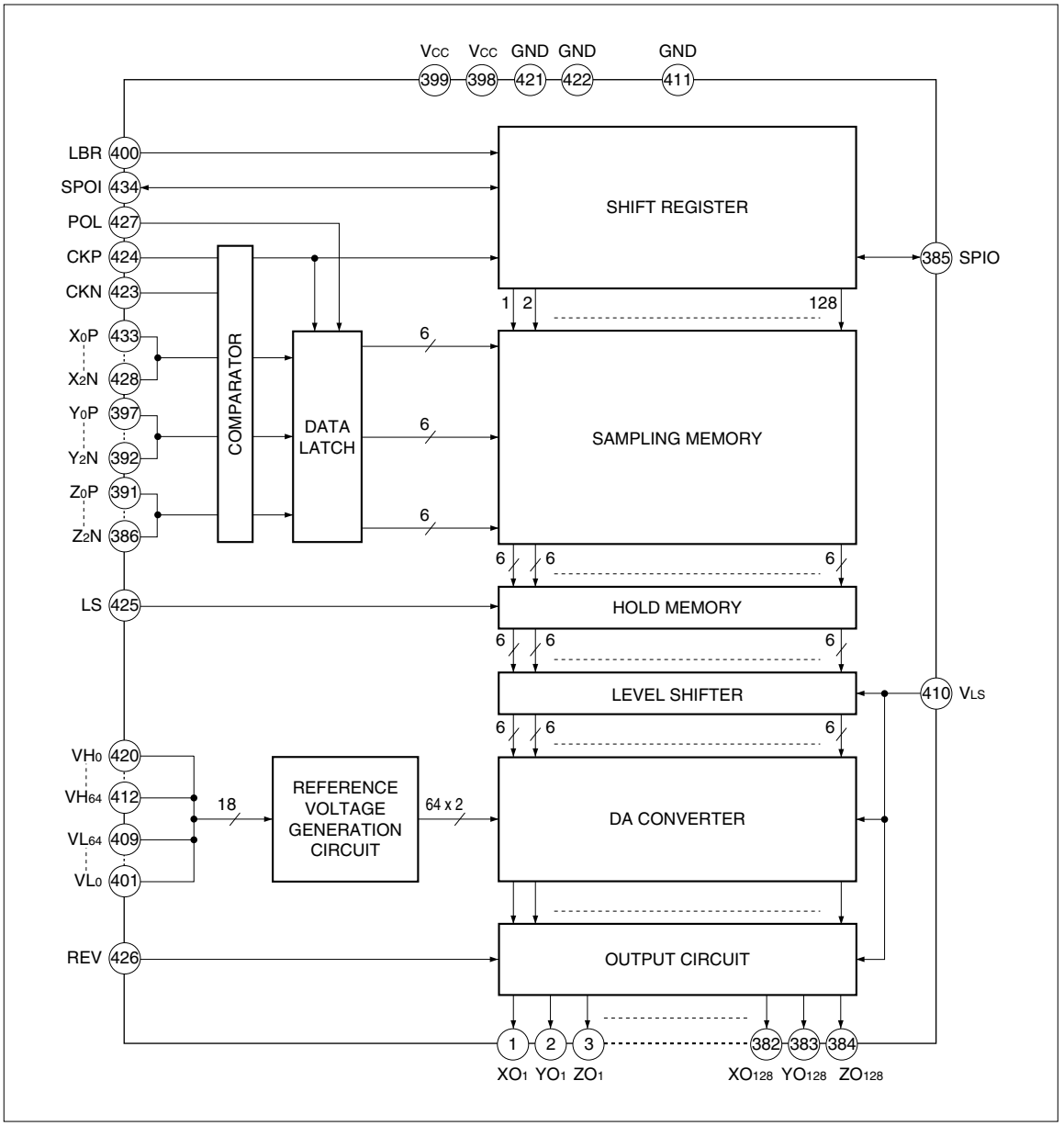
NOTE :
Doesn't prescribe TCP outline.

In the absence of confirmation by device specification sheets, SHARP takes no responsibility for any defects that may occur in equipment using any SHARP devices shown in catalogs, data books, etc. Contact SHARP in order to obtain the latest device specification sheets before using any SHARP device.

PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 to 384	XO_1-ZO_{128}	O	LCD drive output pins
385	SPIO	I/O	Start pulse input/cascade output pin
386 to 391	Z_2N-Z_0P	I	Data input pins
392 to 397	Y_2N-Y_0P	I	Data input pins
398, 399	V_{CC}	–	Power supply pins for digital circuit
400	LBR	I	Shift direction selection input pin
401 to 409	VL_0-VL_{64}	I	Reference voltage input pins
410	V_{LS}	–	Power supply pin for analog circuit
411, 421, 422	GND	–	Ground pins
412 to 420	VH_{64}-VH_0	I	Reference voltage input pins
423, 424	CKN, CKP	I	Shift clock input pins
425	LS	I	Latch input pin
426	REV	I	LCD drive output polarity exchange input pin
427	POL	I	Input data polarity exchange input pin
428 to 433	X_2N-X_0P	I	Data input pins
434	SPOI	I/O	Start pulse input/cascade output pin

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Shift Register	Used as a bi-directional shift register which performs the shifting operation by CK and selects bits for data sampling.
Data Latch	Used to temporary latch the input data which is sent to the sampling memory.
Comparator	Convert low voltage input signal into internal [CMOS level] voltage input signal.
Sampling Memory	Used to sample the data to be entered by time sharing.
Hold Memory	Used for latch processing of data in the sampling memory by LS input.
Level Shifter	Used to shift the data in the hold memory to the power supply level of the analog circuit unit and sends the shifted data to DA converter.
Reference Voltage Generation Circuit	Used to generate a gamma-connected 64 x 2-level voltage by the resistor dividing circuit.
DA Converter	Used to generate an analog signal according to the display data and sends the signal to the output circuit.
Output Circuit	Used as a voltage follower, configured with an operational amplifier and an output buffer, which outputs analog signals of 64 x 2 gray scales to LCD drive output pin.

INPUT/OUTPUT CIRCUITS

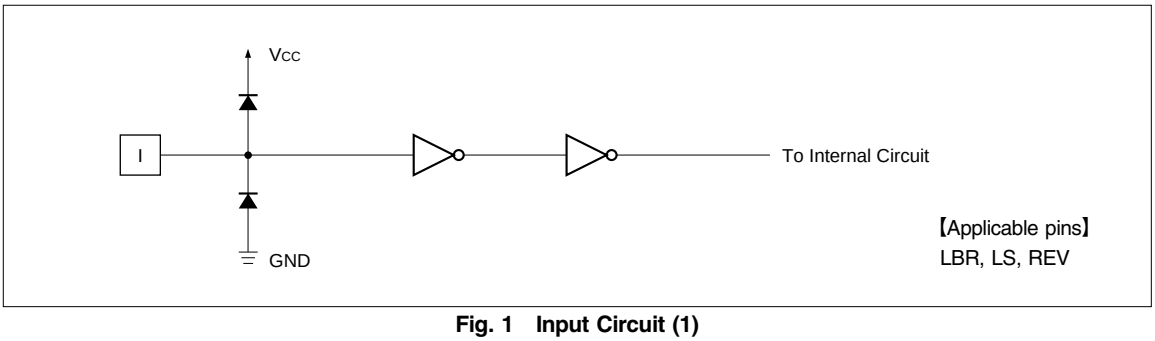


Fig. 1 Input Circuit (1)

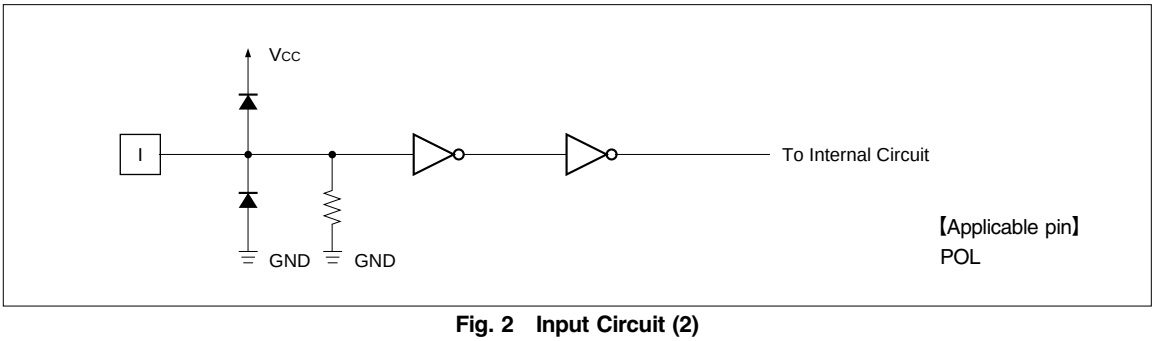


Fig. 2 Input Circuit (2)

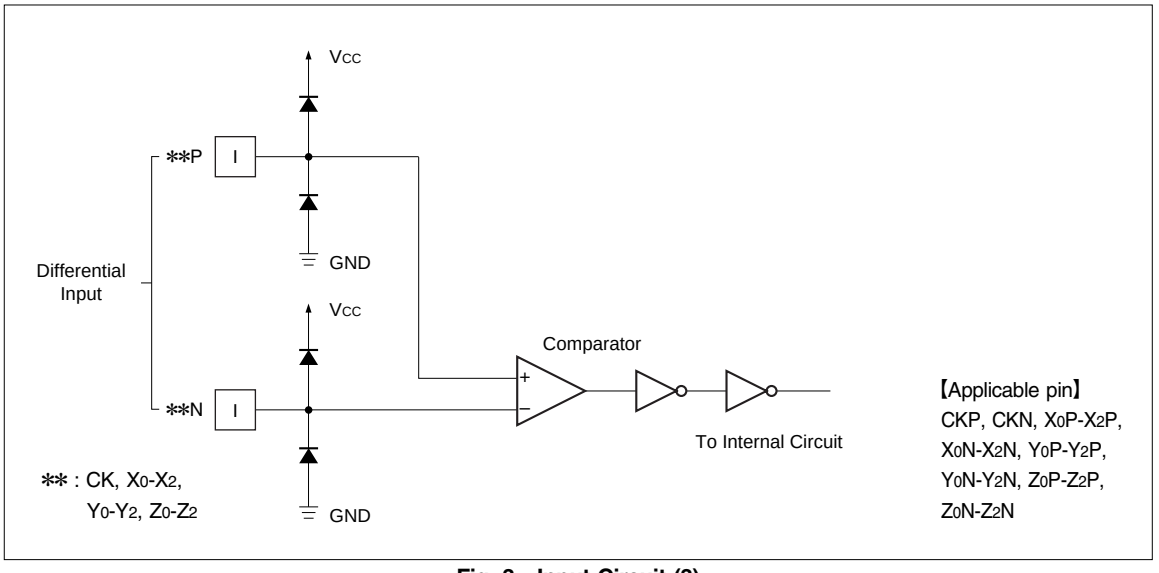


Fig. 3 Input Circuit (3)

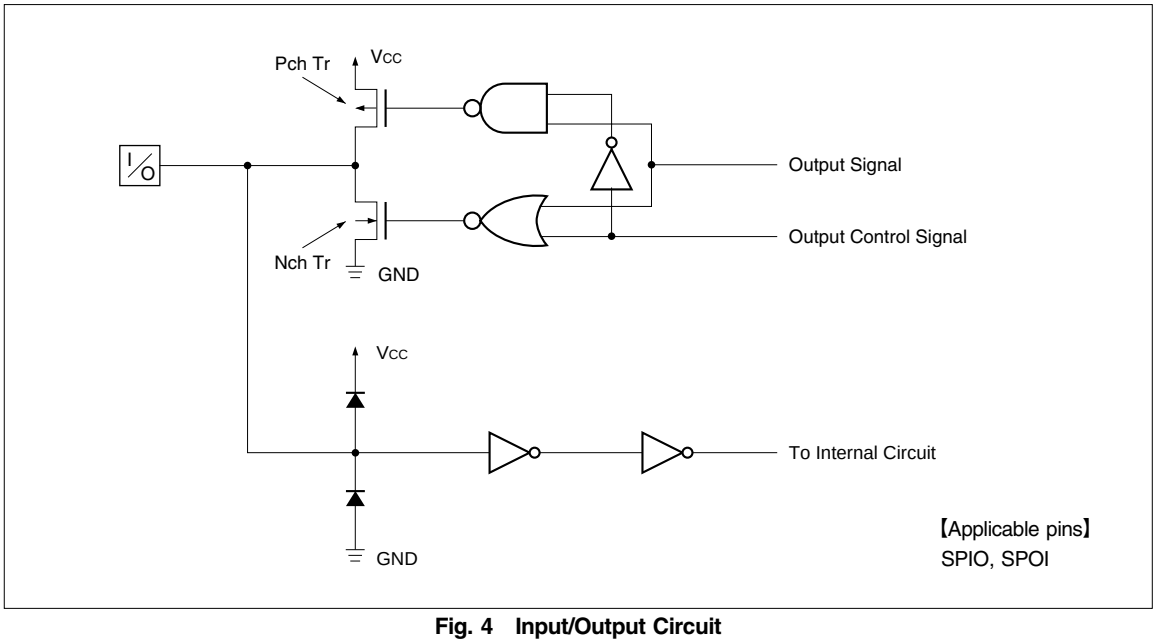


Fig. 4 Input/Output Circuit

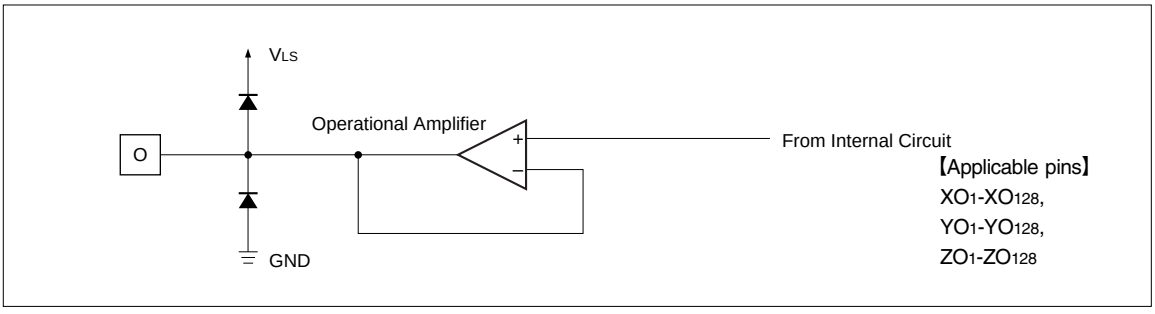


Fig. 5 Output Circuit

FUNCTIONAL DESCRIPTION

Pin Functions

SYMBOL	FUNCTIONS
V_{CC}	Used as power supply pin for digital circuit, connected to +3.0 to +3.6 V.
V_{LS}	Used as power supply pin for analog circuit, connected to +8.0 to +12.0 V.
GND	Used as ground pin, connected to 0 V.
SPIO SPOI	Used as input pins of start pulse and also used as output pins for cascade connection. When "H" is input into start pulse input pin, data sampling is started. On completion of sampling, "H" pulse is output to output pin for cascade connection. Pin functions are selected by LBR. For selecting, refer to **"Functional Operations"**.
LBR	Used as input pin for selecting the shift register direction. For selecting, refer to **"Functional Operations"**.
LS	Used as input pin for parallel transfer from sampling memory to hold memory. Data is transferred at the rising edge and output from LCD drive output pin.
CKP CKN	Used as shift clock input pin. Data is latched into sampling memory from data input pin at the falling edge and the rising edge. (Use RSDS input voltage : 0 V to V_{CC} – 1.0 V)
VH_0-VH_{64} VL_0-VL_{64}	Used as reference voltage input pins. Hold the reference voltage fixed during the period of LCD drive output. For relation between input data and output voltage values, refer to **"Output Voltage Value"**. For internal gamma correction, refer to **"Gamma Correction Value"**. Observe the following relation for input voltage. $V_{LS} > VH_0 \geq VH_8 \geq \cdots \geq VH_{64} \geq VL_{64} \geq VL_{56} \geq \cdots \geq VL_0 >$ GND.
X_0P-X_2N Y_0P-Y_2N Z_0P-Z_2N	Used as data input pins of R, G, and B colors. 3-bit data are input from data pins at the falling edge and the rising edge of CKP (CKN). For relation between input data and output voltage values, refer to **"Functional Operations"** and **"Output Voltage Value"**. Select the data to be entered into X, Y, and Z according to picture element arrays of the panel.
XO_1-XO_{128}, YO_1-YO_{128}, ZO_1-ZO_{128}	Used as LCD drive output pins which output the voltage c/orresponding to the input of data input pins (X_0P to X_2N, Y_0P to Y_2N, Z_0P to Z_2N). Data of XO_1 to XO_{128} correspond to X_0P to X_2N. Data of YO_1 to YO_{128} correspond to Y_0P to Y_2N, and data of ZO_1 to ZO_{128} correspond to Z_0P to Z_2N. For relation between input data and output voltage values, refer to **"Functional Operations"** and **"Output Voltage Value"**.

SYMBOL	FUNCTIONS
POL	Used as input pin for input data polarity exchange. When "L" is entered, display data becomes normal mode. When "H" is entered, input data becomes polarity exchange mode. For relation between input data and output voltage value, refer to **"Output Voltage Value"**. These pins are pulled down at the inside.
REV	Used as polarity exchange pin of LCD drive output. Data is taken at the term when LS is "H" and the output polarity of LCD drive output pin is determined. For exchanging, refer to **"Output Characteristics"**.

Functional Operations

The following describes the relation between data input pin and output direction.

Data input pin	X_0P-X_2N	Y_0P-Y_2N	Z_0P-Z_2N	.....	X_0P-X_2N	Y_0P-Y_2N	Z_0P-Z_2N
Output direction	XO_1	YO_1	ZO_1	.....	XO_{128}	YO_{128}	ZO_{128}

The following describes the relation between LBR pin, SPOI pin, SPIO pin and output direction

PIN	OUTPUT DIRECTION	
	RIGHT SHIFT (XO_1, YO_1, ZO_1→XO_{128}, YO_{128}, ZO_{128})	LEFT SHIFT (ZO_{128}, YO_{128}, XO_{128}→ZO_1, YO_1, XO_1)
LBR	H	L
SPOI	Input	Output
SPIO	Output	Input

NOTE :

Color data corresponding to X, Y, and Z vary depending on the output direction.

Output Characteristics

The following describes the relation between REV pin and output polarity of LCD drive pin.

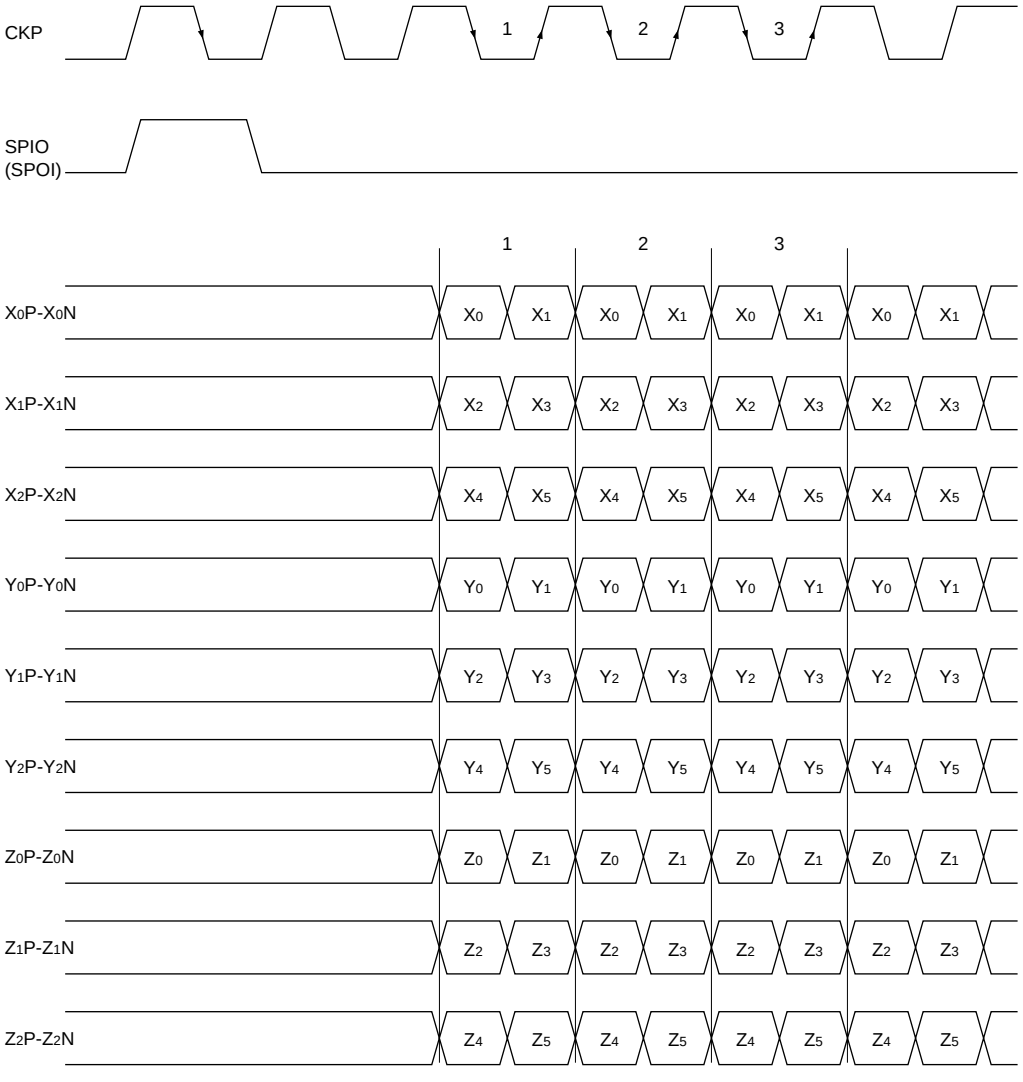
REV	"H"	"L"
XO_1	+	–
YO_1	–	+
ZO_1	+	–
XO_2	–	+
YO_2	+	–
ZO_2	–	+
XO_3	+	–
YO_3	–	+
ZO_3	+	–
XO_4	–	+
YO_4	+	–
ZO_4	–	+
:	:	:
XO_{125}	+	–
YO_{125}	–	+
ZO_{125}	+	–
XO_{126}	–	+
YO_{126}	+	–
ZO_{126}	–	+
XO_{127}	+	–
YO_{127}	–	+
ZO_{127}	+	–
XO_{128}	–	+
YO_{128}	+	–
ZO_{128}	–	+

NOTES :

+ : The gray scale voltages corresponding to reference voltage VH_0 to VH_{64} are outputs.

– : The gray scale voltages corresponding to reference voltage VL_0 to VL_{64} are outputs.

Timing Diagram



Output Voltage Value

Two voltages are selected from all of the reference voltages (V_0-V_{64}) by the upper 3-bit data (D_5, D_4 and D_3) of the 6-bit input data (D_5, D_4, D_3, D_2, D_1 and D_0) taken by time sharing, and intermediate value is determined by the lower 3-bit data (D_2, D_1 and D_0). The V_i is a reference voltage (VH_i or VL_i) that is determined by the polarity exchange input (REV). Relation between input data and output voltage values is shown below.

(i = 0, 8, 16, 24, 32, 40, 48, 56, 64)

(1) Output voltage when reference voltage is VH_0 to VH_{64}.

INPUT DATA	OUTPUT VOLTAGE		INPUT DATA	OUTPUT VOLTAGE	
	POL = "L"	POL = "H"		POL = "L"	POL = "H"
0	VH_0	$VH_{64} + (VH_{56} - VH_{64}) \times 1/8$	20	VH_{32}	$VH_{32} + (VH_{24} - VH_{32}) \times 1/8$
1	$VH_8 + (VH_0 - VH_8) \times 7/8$	$VH_{64} + (VH_{56} - VH_{64}) \times 2/8$	21	$VH_{40} + (VH_{32} - VH_{40}) \times 7/8$	$VH_{32} + (VH_{24} - VH_{32}) \times 2/8$
2	$VH_8 + (VH_0 - VH_8) \times 6/8$	$VH_{64} + (VH_{56} - VH_{64}) \times 3/8$	22	$VH_{40} + (VH_{32} - VH_{40}) \times 6/8$	$VH_{32} + (VH_{24} - VH_{32}) \times 3/8$
3	$VH_8 + (VH_0 - VH_8) \times 5/8$	$VH_{64} + (VH_{56} - VH_{64}) \times 4/8$	23	$VH_{40} + (VH_{32} - VH_{40}) \times 5/8$	$VH_{32} + (VH_{24} - VH_{32}) \times 4/8$
4	$VH_8 + (VH_0 - VH_8) \times 4/8$	$VH_{64} + (VH_{56} - VH_{64}) \times 5/8$	24	$VH_{40} + (VH_{32} - VH_{40}) \times 4/8$	$VH_{32} + (VH_{24} - VH_{32}) \times 5/8$
5	$VH_8 + (VH_0 - VH_8) \times 3/8$	$VH_{64} + (VH_{56} - VH_{64}) \times 6/8$	25	$VH_{40} + (VH_{32} - VH_{40}) \times 3/8$	$VH_{32} + (VH_{24} - VH_{32}) \times 6/8$
6	$VH_8 + (VH_0 - VH_8) \times 2/8$	$VH_{64} + (VH_{56} - VH_{64}) \times 7/8$	26	$VH_{40} + (VH_{32} - VH_{40}) \times 2/8$	$VH_{32} + (VH_{24} - VH_{32}) \times 7/8$
7	$VH_8 + (VH_0 - VH_8) \times 1/8$	VH_{56}	27	$VH_{40} + (VH_{32} - VH_{40}) \times 1/8$	VH_{24}
8	VH_8	$VH_{56} + (VH_{48} - VH_{56}) \times 1/8$	28	VH_{40}	$VH_{24} + (VH_{16} - VH_{24}) \times 1/8$
9	$VH_{16} + (VH_8 - VH_{16}) \times 7/8$	$VH_{56} + (VH_{48} - VH_{56}) \times 2/8$	29	$VH_{48} + (VH_{40} - VH_{48}) \times 7/8$	$VH_{24} + (VH_{16} - VH_{24}) \times 2/8$
A	$VH_{16} + (VH_8 - VH_{16}) \times 6/8$	$VH_{56} + (VH_{48} - VH_{56}) \times 3/8$	2A	$VH_{48} + (VH_{40} - VH_{48}) \times 6/8$	$VH_{24} + (VH_{16} - VH_{24}) \times 3/8$
B	$VH_{16} + (VH_8 - VH_{16}) \times 5/8$	$VH_{56} + (VH_{48} - VH_{56}) \times 4/8$	2B	$VH_{48} + (VH_{40} - VH_{48}) \times 5/8$	$VH_{24} + (VH_{16} - VH_{24}) \times 4/8$
C	$VH_{16} + (VH_8 - VH_{16}) \times 4/8$	$VH_{56} + (VH_{48} - VH_{56}) \times 5/8$	2C	$VH_{48} + (VH_{40} - VH_{48}) \times 4/8$	$VH_{24} + (VH_{16} - VH_{24}) \times 5/8$
D	$VH_{16} + (VH_8 - VH_{16}) \times 3/8$	$VH_{56} + (VH_{48} - VH_{56}) \times 6/8$	2D	$VH_{48} + (VH_{40} - VH_{48}) \times 3/8$	$VH_{24} + (VH_{16} - VH_{24}) \times 6/8$
E	$VH_{16} + (VH_8 - VH_{16}) \times 2/8$	$VH_{56} + (VH_{48} - VH_{56}) \times 7/8$	2E	$VH_{48} + (VH_{40} - VH_{48}) \times 2/8$	$VH_{24} + (VH_{16} - VH_{24}) \times 7/8$
F	$VH_{16} + (VH_8 - VH_{16}) \times 1/8$	VH_{48}	2F	$VH_{48} + (VH_{40} - VH_{48}) \times 1/8$	VH_{16}
10	VH_{16}	$VH_{48} + (VH_{40} - VH_{48}) \times 1/8$	30	VH_{48}	$VH_{16} + (VH_8 - VH_{16}) \times 1/8$
11	$VH_{24} + (VH_{16} - VH_{24}) \times 7/8$	$VH_{48} + (VH_{40} - VH_{48}) \times 2/8$	31	$VH_{56} + (VH_{48} - VH_{56}) \times 7/8$	$VH_{16} + (VH_8 - VH_{16}) \times 2/8$
12	$VH_{24} + (VH_{16} - VH_{24}) \times 6/8$	$VH_{48} + (VH_{40} - VH_{48}) \times 3/8$	32	$VH_{56} + (VH_{48} - VH_{56}) \times 6/8$	$VH_{16} + (VH_8 - VH_{16}) \times 3/8$
13	$VH_{24} + (VH_{16} - VH_{24}) \times 5/8$	$VH_{48} + (VH_{40} - VH_{48}) \times 4/8$	33	$VH_{56} + (VH_{48} - VH_{56}) \times 5/8$	$VH_{16} + (VH_8 - VH_{16}) \times 4/8$
14	$VH_{24} + (VH_{16} - VH_{24}) \times 4/8$	$VH_{48} + (VH_{40} - VH_{48}) \times 5/8$	34	$VH_{56} + (VH_{48} - VH_{56}) \times 4/8$	$VH_{16} + (VH_8 - VH_{16}) \times 5/8$
15	$VH_{24} + (VH_{16} - VH_{24}) \times 3/8$	$VH_{48} + (VH_{40} - VH_{48}) \times 6/8$	35	$VH_{56} + (VH_{48} - VH_{56}) \times 3/8$	$VH_{16} + (VH_8 - VH_{16}) \times 6/8$
16	$VH_{24} + (VH_{16} - VH_{24}) \times 2/8$	$VH_{48} + (VH_{40} - VH_{48}) \times 7/8$	36	$VH_{56} + (VH_{48} - VH_{56}) \times 2/8$	$VH_{16} + (VH_8 - VH_{16}) \times 7/8$
17	$VH_{24} + (VH_{16} - VH_{24}) \times 1/8$	VH_{40}	37	$VH_{56} + (VH_{48} - VH_{56}) \times 1/8$	VH_8
18	VH_{24}	$VH_{40} + (VH_{32} - VH_{40}) \times 1/8$	38	VH_{56}	$VH_8 + (VH_0 - VH_8) \times 1/8$
19	$VH_{32} + (VH_{24} - VH_{32}) \times 7/8$	$VH_{40} + (VH_{32} - VH_{40}) \times 2/8$	39	$VH_{64} + (VH_{56} - VH_{64}) \times 7/8$	$VH_8 + (VH_0 - VH_8) \times 2/8$
1A	$VH_{32} + (VH_{24} - VH_{32}) \times 6/8$	$VH_{40} + (VH_{32} - VH_{40}) \times 3/8$	3A	$VH_{64} + (VH_{56} - VH_{64}) \times 6/8$	$VH_8 + (VH_0 - VH_8) \times 3/8$
1B	$VH_{32} + (VH_{24} - VH_{32}) \times 5/8$	$VH_{40} + (VH_{32} - VH_{40}) \times 4/8$	3B	$VH_{64} + (VH_{56} - VH_{64}) \times 5/8$	$VH_8 + (VH_0 - VH_8) \times 4/8$
1C	$VH_{32} + (VH_{24} - VH_{32}) \times 4/8$	$VH_{40} + (VH_{32} - VH_{40}) \times 5/8$	3C	$VH_{64} + (VH_{56} - VH_{64}) \times 4/8$	$VH_8 + (VH_0 - VH_8) \times 5/8$
1D	$VH_{32} + (VH_{24} - VH_{32}) \times 3/8$	$VH_{40} + (VH_{32} - VH_{40}) \times 6/8$	3D	$VH_{64} + (VH_{56} - VH_{64}) \times 3/8$	$VH_8 + (VH_0 - VH_8) \times 6/8$
1E	$VH_{32} + (VH_{24} - VH_{32}) \times 2/8$	$VH_{40} + (VH_{32} - VH_{40}) \times 7/8$	3E	$VH_{64} + (VH_{56} - VH_{64}) \times 2/8$	$VH_8 + (VH_0 - VH_8) \times 7/8$
1F	$VH_{32} + (VH_{24} - VH_{32}) \times 1/8$	VH_{32}	3F	$VH_{64} + (VH_{56} - VH_{64}) \times 1/8$	VH_0

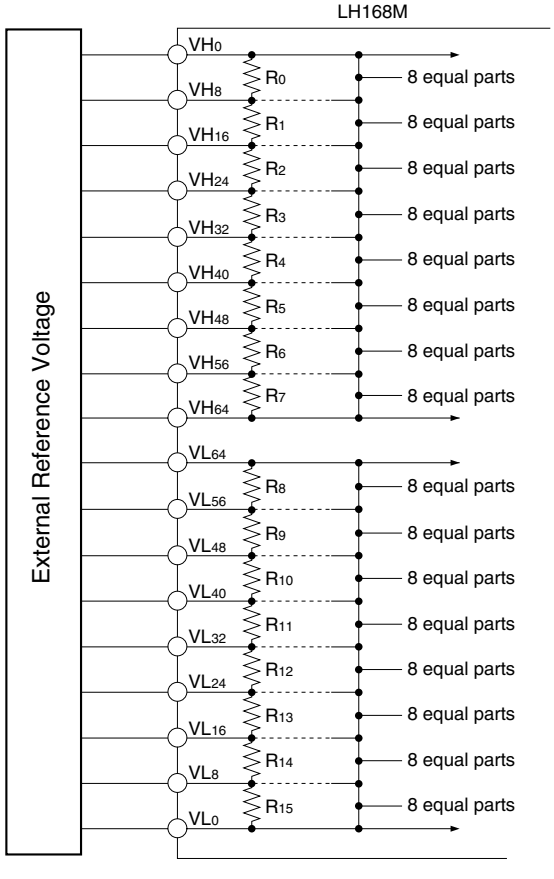
(2) Output voltage when reference voltage is V_{L0} to V_{L64}.

INPUT DATA	OUTPUT VOLTAGE		INPUT DATA	OUTPUT VOLTAGE	
	POL = "L"	POL = "H"		POL = "L"	POL = "H"
0	V_{L0}	$V_{L64} + (V_{L56} - V_{L64}) \times 1/8$	20	V_{L32}	$V_{L32} + (V_{L24} - V_{L32}) \times 1/8$
1	$V_{L8} + (V_{L0} - V_{L8}) \times 7/8$	$V_{L64} + (V_{L56} - V_{L64}) \times 2/8$	21	$V_{L40} + (V_{L32} - V_{L40}) \times 7/8$	$V_{L32} + (V_{L24} - V_{L32}) \times 2/8$
2	$V_{L8} + (V_{L0} - V_{L8}) \times 6/8$	$V_{L64} + (V_{L56} - V_{L64}) \times 3/8$	22	$V_{L40} + (V_{L32} - V_{L40}) \times 6/8$	$V_{L32} + (V_{L24} - V_{L32}) \times 3/8$
3	$V_{L8} + (V_{L0} - V_{L8}) \times 5/8$	$V_{L64} + (V_{L56} - V_{L64}) \times 4/8$	23	$V_{L40} + (V_{L32} - V_{L40}) \times 5/8$	$V_{L32} + (V_{L24} - V_{L32}) \times 4/8$
4	$V_{L8} + (V_{L0} - V_{L8}) \times 4/8$	$V_{L64} + (V_{L56} - V_{L64}) \times 5/8$	24	$V_{L40} + (V_{L32} - V_{L40}) \times 4/8$	$V_{L32} + (V_{L24} - V_{L32}) \times 5/8$
5	$V_{L8} + (V_{L0} - V_{L8}) \times 3/8$	$V_{L64} + (V_{L56} - V_{L64}) \times 6/8$	25	$V_{L40} + (V_{L32} - V_{L40}) \times 3/8$	$V_{L32} + (V_{L24} - V_{L32}) \times 6/8$
6	$V_{L8} + (V_{L0} - V_{L8}) \times 2/8$	$V_{L64} + (V_{L56} - V_{L64}) \times 7/8$	26	$V_{L40} + (V_{L32} - V_{L40}) \times 2/8$	$V_{L32} + (V_{L24} - V_{L32}) \times 7/8$
7	$V_{L8} + (V_{L0} - V_{L8}) \times 1/8$	V_{L56}	27	$V_{L40} + (V_{L32} - V_{L40}) \times 1/8$	V_{L24}
8	V_{L8}	$V_{L56} + (V_{L48} - V_{L56}) \times 1/8$	28	V_{L40}	$V_{L24} + (V_{L16} - V_{L24}) \times 1/8$
9	$V_{L16} + (V_{L8} - V_{L16}) \times 7/8$	$V_{L56} + (V_{L48} - V_{L56}) \times 2/8$	29	$V_{L48} + (V_{L40} - V_{L48}) \times 7/8$	$V_{L24} + (V_{L16} - V_{L24}) \times 2/8$
A	$V_{L16} + (V_{L8} - V_{L16}) \times 6/8$	$V_{L56} + (V_{L48} - V_{L56}) \times 3/8$	2A	$V_{L48} + (V_{L40} - V_{L48}) \times 6/8$	$V_{L24} + (V_{L16} - V_{L24}) \times 3/8$
B	$V_{L16} + (V_{L8} - V_{L16}) \times 5/8$	$V_{L56} + (V_{L48} - V_{L56}) \times 4/8$	2B	$V_{L48} + (V_{L40} - V_{L48}) \times 5/8$	$V_{L24} + (V_{L16} - V_{L24}) \times 4/8$
C	$V_{L16} + (V_{L8} - V_{L16}) \times 4/8$	$V_{L56} + (V_{L48} - V_{L56}) \times 5/8$	2C	$V_{L48} + (V_{L40} - V_{L48}) \times 4/8$	$V_{L24} + (V_{L16} - V_{L24}) \times 5/8$
D	$V_{L16} + (V_{L8} - V_{L16}) \times 3/8$	$V_{L56} + (V_{L48} - V_{L56}) \times 6/8$	2D	$V_{L48} + (V_{L40} - V_{L48}) \times 3/8$	$V_{L24} + (V_{L16} - V_{L24}) \times 6/8$
E	$V_{L16} + (V_{L8} - V_{L16}) \times 2/8$	$V_{L56} + (V_{L48} - V_{L56}) \times 7/8$	2E	$V_{L48} + (V_{L40} - V_{L48}) \times 2/8$	$V_{L24} + (V_{L16} - V_{L24}) \times 7/8$
F	$V_{L16} + (V_{L8} - V_{L16}) \times 1/8$	V_{L48}	2F	$V_{L48} + (V_{L40} - V_{L48}) \times 1/8$	V_{L16}
10	V_{L16}	$V_{L48} + (V_{L40} - V_{L48}) \times 1/8$	30	V_{L48}	$V_{L16} + (V_{L8} - V_{L16}) \times 1/8$
11	$V_{L24} + (V_{L16} - V_{L24}) \times 7/8$	$V_{L48} + (V_{L40} - V_{L48}) \times 2/8$	31	$V_{L56} + (V_{L48} - V_{L56}) \times 7/8$	$V_{L16} + (V_{L8} - V_{L16}) \times 2/8$
12	$V_{L24} + (V_{L16} - V_{L24}) \times 6/8$	$V_{L48} + (V_{L40} - V_{L48}) \times 3/8$	32	$V_{L56} + (V_{L48} - V_{L56}) \times 6/8$	$V_{L16} + (V_{L8} - V_{L16}) \times 3/8$
13	$V_{L24} + (V_{L16} - V_{L24}) \times 5/8$	$V_{L48} + (V_{L40} - V_{L48}) \times 4/8$	33	$V_{L56} + (V_{L48} - V_{L56}) \times 5/8$	$V_{L16} + (V_{L8} - V_{L16}) \times 4/8$
14	$V_{L24} + (V_{L16} - V_{L24}) \times 4/8$	$V_{L48} + (V_{L40} - V_{L48}) \times 5/8$	34	$V_{L56} + (V_{L48} - V_{L56}) \times 4/8$	$V_{L16} + (V_{L8} - V_{L16}) \times 5/8$
15	$V_{L24} + (V_{L16} - V_{L24}) \times 3/8$	$V_{L48} + (V_{L40} - V_{L48}) \times 6/8$	35	$V_{L56} + (V_{L48} - V_{L56}) \times 3/8$	$V_{L16} + (V_{L8} - V_{L16}) \times 6/8$
16	$V_{L24} + (V_{L16} - V_{L24}) \times 2/8$	$V_{L48} + (V_{L40} - V_{L48}) \times 7/8$	36	$V_{L56} + (V_{L48} - V_{L56}) \times 2/8$	$V_{L16} + (V_{L8} - V_{L16}) \times 7/8$
17	$V_{L24} + (V_{L16} - V_{L24}) \times 1/8$	V_{L40}	37	$V_{L56} + (V_{L48} - V_{L56}) \times 1/8$	V_{L8}
18	V_{L24}	$V_{L40} + (V_{L32} - V_{L40}) \times 1/8$	38	V_{L56}	$V_{L8} + (V_{L0} - V_{L8}) \times 1/8$
19	$V_{L32} + (V_{L24} - V_{L32}) \times 7/8$	$V_{L40} + (V_{L32} - V_{L40}) \times 2/8$	39	$V_{L64} + (V_{L56} - V_{L64}) \times 7/8$	$V_{L8} + (V_{L0} - V_{L8}) \times 2/8$
1A	$V_{L32} + (V_{L24} - V_{L32}) \times 6/8$	$V_{L40} + (V_{L32} - V_{L40}) \times 3/8$	3A	$V_{L64} + (V_{L56} - V_{L64}) \times 6/8$	$V_{L8} + (V_{L0} - V_{L8}) \times 3/8$
1B	$V_{L32} + (V_{L24} - V_{L32}) \times 5/8$	$V_{L40} + (V_{L32} - V_{L40}) \times 4/8$	3B	$V_{L64} + (V_{L56} - V_{L64}) \times 5/8$	$V_{L8} + (V_{L0} - V_{L8}) \times 4/8$
1C	$V_{L32} + (V_{L24} - V_{L32}) \times 4/8$	$V_{L40} + (V_{L32} - V_{L40}) \times 5/8$	3C	$V_{L64} + (V_{L56} - V_{L64}) \times 4/8$	$V_{L8} + (V_{L0} - V_{L8}) \times 5/8$
1D	$V_{L32} + (V_{L24} - V_{L32}) \times 3/8$	$V_{L40} + (V_{L32} - V_{L40}) \times 6/8$	3D	$V_{L64} + (V_{L56} - V_{L64}) \times 3/8$	$V_{L8} + (V_{L0} - V_{L8}) \times 6/8$
1E	$V_{L32} + (V_{L24} - V_{L32}) \times 2/8$	$V_{L40} + (V_{L32} - V_{L40}) \times 7/8$	3E	$V_{L64} + (V_{L56} - V_{L64}) \times 2/8$	$V_{L8} + (V_{L0} - V_{L8}) \times 7/8$
1F	$V_{L32} + (V_{L24} - V_{L32}) \times 1/8$	V_{L32}	3F	$V_{L64} + (V_{L56} - V_{L64}) \times 1/8$	V_{L0}

γ (Gamma) Correction Value

Between reference voltage input pins VH_0 and VH_{64}, 64 resistors are connected in series.
And between reference voltage input pins VL_0 and VL_{64}, 64 resistors are connected in series. No resistor is connected between reference voltage input pins VH_{64} and VL_{64}.

The γ correction curve is a broken line connected between intermediate voltage inputs (VH_8, VH_{16}, VH_{24}, VH_{32}, VH_{40}, VH_{48}, VH_{56}, VL_8, VL_{16}, VL_{24}, VL_{32}, VL_{40}, VL_{48} and VL_{56}). Each γ correction value between the intermediate voltage inputs is divided into 8 parts by the same resistor.



The following shows the ratio of γ correction resistance, when R_0 equals 1.

R_0	1.00
R_1	0.50
R_2	0.50
R_3	0.50
R_4	0.50
R_5	0.50
R_6	0.50
R_7	1.00

R_8	1.00
R_9	0.50
R_{10}	0.50
R_{11}	0.50
R_{12}	0.50
R_{13}	0.50
R_{14}	0.50
R_{15}	1.00

PRECAUTIONS

Precautions when connecting or disconnecting the power supply

This IC has some power supply pins, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. Therefore, when connecting the power supply, observe the following sequence.

V_{CC} → logic input → V_{LS}, VH_0-VH_{64}, VL_0-VL_{64}

When disconnecting the power supply, follow the reverse sequence.

Reference voltage input

The relation of the reference voltage input is shown here.

$V_{LS} > VH_0 \geq VH_8 \geq \cdots \geq VH_{56} \geq VH_{64} \geq 0.5V_{LS} \geq VL_{64} \geq VL_{56} \geq \cdots \geq VL_8 \geq VL_0 >$ GND

Maximum ratings

When connecting or disconnecting the power supply, this IC must be used within the range of the absolute maximum ratings.

Target output load

This IC is designed for a 150 pF output load capacity. When using this IC for other than 150 pF panels, confirm the device is having no problem before using it.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage	V_{CC}	V_{CC}	−0.3 to +6.0	V	1, 2
	V_{LS}	V_{LS}	−0.3 to +13.0	V	
Input voltage	V_I	VH_0-VL_0	−0.3 to V_{LS} + 0.3	V	
	V_I	SPIO, SPOI, CKP, CKN, LS, REV, LBR, POL, X_0P-X_2N, Y_0P-Y_2N, Z_0P-Z_2N	−0.3 to V_{CC} + 0.3	V	
Output voltage	V_O	SPIO, SPOI	−0.3 to V_{CC} + 0.3	V	
	V_O	XO_1-ZO_{128}	−0.3 to V_{LS} + 0.3	V	
Storage temperature	T_{STG}		−45 to +125	˚C	

NOTES :

1. T_A = +25 ˚C
2. The maximum applicable voltage on any pin with respect to GND (0 V).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	+3.0		+3.6	V	1
	V_{LS}	+8.0		+12.0	V	
Reference voltage input	VH_0-VH_{64}	0.5V_{LS}		V_{LS} − 0.1	V	
	VL_0-VL_{64}	+0.1		0.5V_{LS}	V	
Clock frequency	f_{CK}			68	MHz	
LCD drive output load capacity	C_L			150	pF	
Operating temperature	T_{OPR}	−20		+75	˚C	

NOTE :

1. The applicable voltage on any pin with respect to GND (0 V).

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = +3.0 to +3.6 V, V_{LS} = +8.0 to +12.0 V, T_{OPR} = −20 to +75 ˚C)

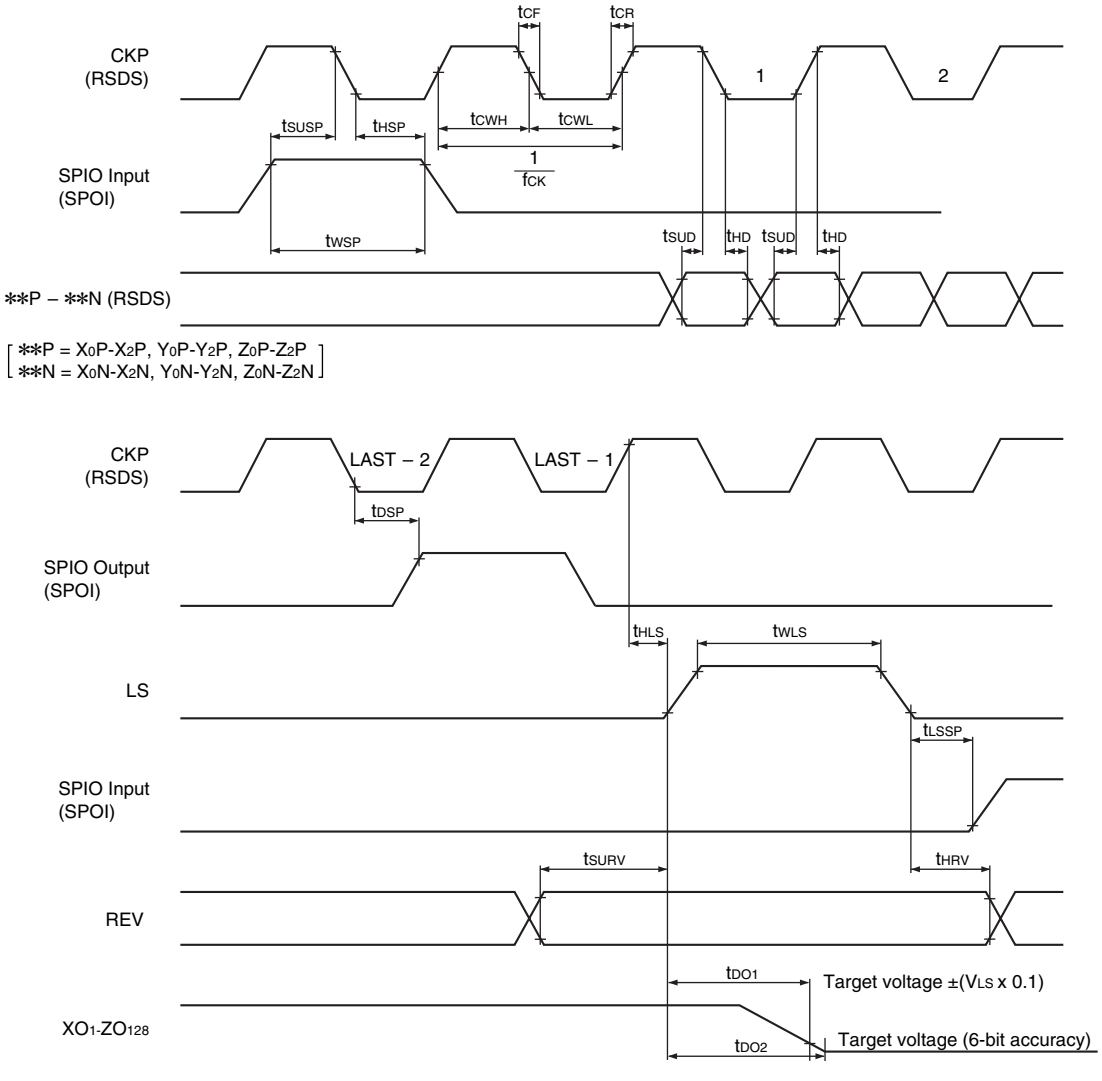
PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		SPIO, SPOI, LS, LBR, REV, POL	GND		0.3V_{CC}	V	
Input "High" voltage	V_{IH}			0.7V_{CC}		V_{CC}	V	
RSDS Input "Low" voltage	V_{ILRSDS}		X_0P-X_2N, Y_0P-Y_2N, Z_0P-Z_2N, CKP, CKN		−200		mV	1
RSDS Input "High" voltage	V_{IHRSDS}				200		mV	
RSDS reference voltage	$V_{COMRSDS}$			GND + 0.1	1.2	V_{CC} − 1.2	V	2
Output "Low" voltage	V_{OL}	I_{OL} = 0.3 mA	SPIO, SPOI	GND		GND + 0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = −0.3 mA		V_{CC} − 0.4		V_{CC}	V	
Input "Low" current	I_{ILL1}		X_0P-X_2N, Y_0P-Y_2N, Z_0P-Z_2N, SPIO, SPOI, CKP, CKN, LS LBR, REV, POL			10	µA	
Input "High" current	I_{ILH1}		X_0P-X_2N, Y_0P-Y_2N, Z_0P-Z_2N, SPIO, SPOI, CKP, CKN, LS, LBR			10	µA	
	I_{ILH2}		POL			400	µA	
Supply current (In operation mode)	I_{CC1}	f_{CK} = 65 MHz f_{LS} = 50 kHz f_{REV} = 50 kHz (Data sampling state)	V_{CC}-GND			14	mA	
Supply current (In standby mode)	I_{CC2}	f_{CK} = 65 MHz f_{LS} = 50 kHz SPI = REV = GND is fixed. (Standby state)				2	mA	
Supply current (In operation mode)	I_{LS1}	f_{CK} = 65 MHz f_{LS} = 50 kHz f_{REV} = 50 kHz (Data sampling state)	V_{LS}-GND			5	mA	
Supply current (In standby mode)	I_{LS2}	f_{CK} = 65 MHz f_{LS} = 50 kHz SPI = REV = GND is fixed. (Standby state)				4	mA	
Output voltage range	V_{OUT}		XO_1-ZO_{128}	GND + 0.2		V_{LS} − 0.2	V	3
Deviations between output voltage pins	V_{OD}			−20		+20	mV	
Output current	I_{O1}-I_{O4}			100	200		µA	4
Resistance between reference voltage input pins	R_{GMAH}		VH_0-VH_{64}	10	20	30	kΩ	
	R_{GMAL}		VL_0-VL_{64}	10	20	30	kΩ	

NOTES :

1. $V_{COMRSDS}$ = (V**P+V**N)/2 = 1.2 V
   **P = X_0P-X_2P, Y_0P-Y_2P, Z_0P-Z_2P
   **N = X_0N-X_2N, Y_0N-Y_2N, Z_0N-Z_2N
2. $V_{DIFFRSDS}$ = V**P − V**N = 0.2 V
3. Criterion of evaluating voltage deviations.
   (a) Between output voltage pins
   Measuring values : Output voltage value at the time after 10 µs at the rising edge of LS. (Average of several times)
   (Conditions) Output load capacity is 150 pF.
   In a state when the reference voltage is fixed.
   Expecting values : Calculated following these specifications.
   (Conditions) In a state when the reference voltage is fixed.
   (b) Between LCD drivers.
   Measuring values : Applicable to (a).
   (Conditions) Applicable to (a).
   Expecting values : Applicable to (a).
   (Conditions) Applicable to (a).
   Each input voltage between the LCD drivers must be made perfectly equal by connecting corresponding reference voltage input pins.
4. I_{O1} : Applied voltage = 8.0 V for output pins XO_1 to ZO_{128}.
   Output voltage = 7.5 V for output pins XO_1 to ZO_{128}.
   V_{LS} = 10.0 V
   I_{O2} : Applied voltage = 7.0 V for output pins XO_1 to ZO_{128}.
   Output voltage = 7.5 V for output pins XO_1 to ZO_{128}.
   V_{LS} = 10.0 V
   I_{O3} : Applied voltage = 3.0 V for output pins XO_1 to ZO_{128}.
   Output voltage = 2.5 V for output pins XO_1 to ZO_{128}.
   V_{LS} = 10.0 V
   I_{O4} : Applied voltage = 2.0 V for output pins XO_1 to ZO_{128}.
   Output voltage = 2.5 V for output pins XO_1 to ZO_{128}.
   V_{LS} = 10.0 V

AC Characteristics

(V_{CC} = +3.0 to +3.6 V, V_{LS} = +8.0 to +12.0 V, T_{OPR} = –20 to +75 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT
Clock frequency	f_{CK}		CKP			68	MHz
"H" level pulse width	t_{CWH}			6			ns
"L" level pulse width	t_{CWL}			6			ns
Input rise time	t_{CR}					5	ns
Input fall time	t_{CF}					5	ns
Data setup time	t_{SUD}		X_0P-X_2N, Y_0P-Y_2N, Z_0P-Z_2N	3			ns
Data hold time	t_{HD}			0			ns
Start pulse setup time	t_{SUSP}		SPIO, SPOI	1			ns
Start pulse hold time	t_{HSP}			2			ns
Start pulse width	t_{WSP}					$\frac{1}{f_{CK}}$	ns
Start pulse output delay time	t_{DSP}	C_L = 15 pF				13	ns
LCD drive output delay time 1	t_{DO1}	C_L = 150 pF	XO_1-ZO_{128}			3	µs
LCD drive output delay time 2	t_{DO2}	C_L = 150 pF				10	µs
LS signal-SPI signal setup time	t_{LSSP}		LS	$\frac{1}{f_{CK}}$			ns
LS signal-CK signal hold time	t_{HLS}			7			ns
LS signal "H" level width	t_{WLS}			$\frac{1}{f_{CK}}$			ns
REV signal-LS signal setup time	t_{SURV}		REV	14			ns
REV signal-LS signal hold time	t_{HRV}			10			ns

Timing Chart