74ALVC16373

Low-Voltage 1.8/2.5/3.3 V 16-Bit Transparent Latch

With 3.6 V−Tolerant Inputs and Outputs (3−State, Non−Inverting)

ON Semiconductor®

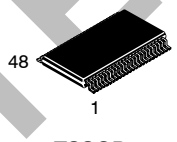
http://onsemi.com

The 74ALVC16373 is an advanced performance, non−inverting 16−bit transparent latch. It is designed for very high−speed, very low−power operation in 1.8 V, 2.5 V or 3.3 V systems. The ALVC16373 is byte controlled, with each byte functioning identically, but independently. Each byte has separate Output Enable and Latch Enable inputs. These control pins can be tied together for full 16−bit operation.

The 74ALVC16373 contains 16 D−type latches with 3−state 3.6 V−tolerant outputs. When the Latch Enable (LEn) inputs are HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, (a latch output will change state each time its D input changes). When LE is LOW, the latch stores the information that was present on the D inputs a setup time preceding the HIGH−to−LOW transition of LE. The 3−state outputs are controlled by the Output Enable ($\overline{\text{OEn}}$) inputs. When $\overline{\text{OE}}$ is LOW, the outputs are enabled. When $\overline{\text{OE}}$ is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches.

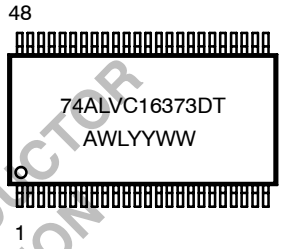
- Designed for Low Voltage Operation: V_{CC} = 1.65−3.6 V
- 3.6V Tolerant Inputs and Outputs
- High Speed Operation: 3.6 ns max for 3.0 to 3.6 V
  4.5 ns max for 2.3 to 2.7 V
  6.8 ns max for 1.65 to 1.95 V
- Static Drive: ±24 mA Drive at 3.0 V
  ±12 mA Drive at 2.3 V
  ±4 mA Drive at 1.65 V
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0 V†
- Near Zero Static Supply Current in All Three Logic States (40 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds ±250 mA @ 125°C
- ESD Performance: Human Body Model >2000 V; Machine Model >200 V
- Second Source to Industry Standard 74ALVC16373

†To ensure the outputs activate in the 3−state condition, the output enable pins should be connected to V_{CC} through a pull−up resistor. The value of the resistor is determined by the current sinking capability of the output connected to the $\overline{\text{OE}}$ pin.



TSSOP−48
DT SUFFIX
CASE 1201

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN NAMES

Pins	Function
$\overline{\text{OEn}}$	Output Enable Inputs
LEn	Latch Enable Inputs
D0−D15	Inputs
O0−O15	Outputs

ORDERING INFORMATION

Device	Package	Shipping
74ALVC16373DTR	TSSOP	2500/Tape & Reel

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

© Semiconductor Components Industries, LLC, 2006

June, 2006 − Rev. 1
Publication Order Number:
74ALVC16373/D

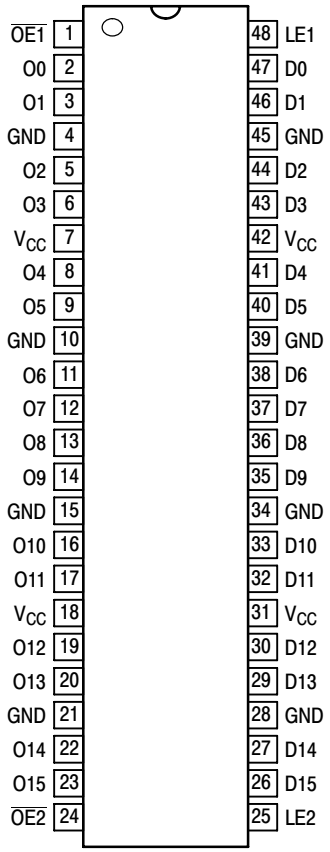


Figure 1. 48−Lead Pinout
(Top View)

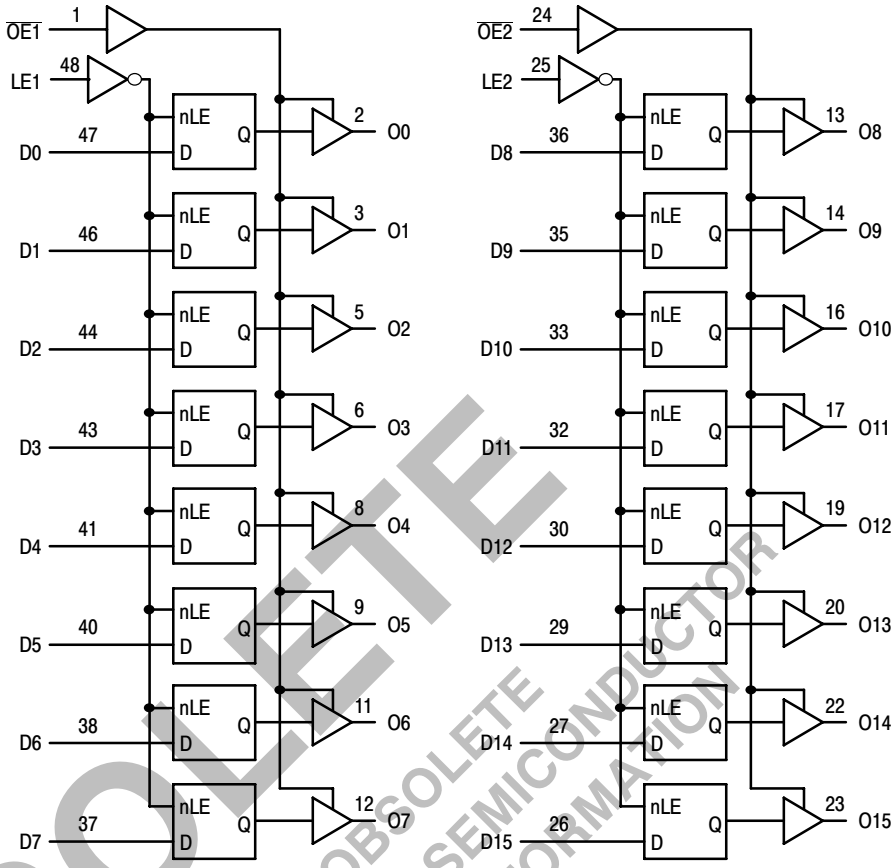


Figure 2. Logic Diagram

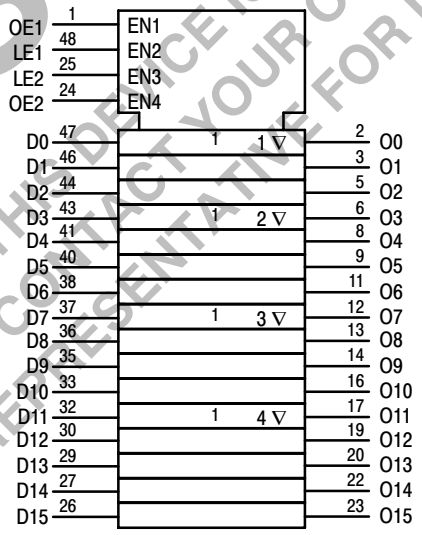


Figure 3. IEC Logic Diagram

Inputs			Outputs	Inputs			Outputs
LE1	**$\overline{OE1}$**	**D0:7**	**O0:7**	**LE2**	**$\overline{OE2}$**	**D8:15**	**O8:15**
X	H	X	Z	X	H	X	Z
H	L	L	L	H	L	L	L
H	L	H	H	H	L	H	H
L.	L	X	O0	L	L	X	O0

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs. O0 = No Change.

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

MAXIMUM RATINGS (Note 1)

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +4.6	V
V_I	DC Input Voltage		−0.5 to +4.6	V
V_O	DC Output Voltage		−0.5 to +4.6	V
I_{IK}	DC Input Diode Current	V_I < GND	−50	mA
I_{OK}	DC Output Diode Current	V_O < GND	−50	mA
I_O	DC Output Sink/Source Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)		90	°C/W
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL−94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	>2000 >200 N/A	V
$I_{LATCH-UP}$	Latch−Up Performance	Above V_{CC} and Below GND at 125°C (Note 6)	±250	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2−ounce copper trace with no air flow.
3. Tested to EIA/JESD22−A114−A.
4. Tested to EIA/JESD22−A115−A.
5. Tested to JESD22−C101−A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.2	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	(Note 7)	−0.5		3.6	V
V_O	Output Voltage	(Active State) (3−State)	0 0		V_{CC} 3.6	V
T_A	Operating Free−Air Temperature		−40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V,	V_{CC} = 2.5 V ±0.2 V V_{CC} = 3.0 V ±0.3 V	0 0		20 10	ns/V

7. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = −40°C to +85°C Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 8)	1.65 V ≤ V_{CC} < 2.3 V	0.65 x V_{CC}		V
		2.3 V ≤ V_{CC} ≤ 2.7 V	1.7		
		2.7 V < V_{CC} ≤ 3.6 V	2.0		
V_{IL}	LOW Level Input Voltage (Note 8)	1.65 V ≤ V_{CC} < 2.3 V		0.35 x V_{CC}	V
		2.3 V ≤ V_{CC} ≤ 2.7 V		0.7	
		2.7 V < V_{CC} ≤ 3.6 V		0.8	
V_{OH}	HIGH Level Output Voltage	1.65 V ≤ V_{CC} ≤ 3.6 V; I_{OH} = −100 μA	V_{CC} − 0.2		V
		V_{CC} = 1.65 V; I_{OH} = −4 mA	1.2		
		V_{CC} = 2.3 V; I_{OH} = −6 mA	2.0		
		V_{CC} = 2.3 V; I_{OH} = −12 mA	1.7		
		V_{CC} = 2.7 V; I_{OH} = −12 mA	2.2		
		V_{CC} = 3.0 V; I_{OH} = −12 mA	2.4		
		V_{CC} = 3.0 V; I_{OH} = −24 mA	2.0		
V_{OL}	LOW Level Output Voltage	1.65 V ≤ V_{CC} ≤ 3.6 V; I_{OL} = 100 μA		0.2	V
		V_{CC} = 1.65 V; I_{OL} = 4 mA		0.45	
		V_{CC} = 2.3 V; I_{OL} = 6 mA		0.4	
		V_{CC} = 2.3 V; I_{OL} = 12 mA		0.7	
		V_{CC} = 2.7 V; I_{OL} = 12 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 24 mA		0.55	
I_I	Input Leakage Current	1.65 V ≤ V_{CC} ≤ 3.6 V; 0 V ≤ V_I ≤ 3.6 V		±5.0	μA
I_{OZ}	3−State Output Current	1.65 V ≤ V_{CC} ≤ 3.6 V; 0 V ≤ V_O ≤ 3.6 V; V_I = V_{IH} or V_{IL}		±10	μA
I_{OFF}	Power−Off Leakage Current	V_{CC} = 0 V; V_I or V_O = 3.6 V		10	μA
I_{CC}	Quiescent Supply Current (Note 9)	1.65 V ≤ V_{CC} ≤ 3.6 V; V_I = GND or V_{CC}		40	μA
		1.65 V ≤ V_{CC} ≤ 3.6 V; 3.6 V ≤ V_I, V_O ≤ 3.6 V		±40	μA
ΔI_{CC}	Increase in I_{CC} per Input	2.7 V < V_{CC} ≤ 3.6 V; V_{IH} = V_{CC} − 0.6 V		750	μA

8. These values of V_I are used to test DC electrical characteristics only.
9. Outputs disabled or 3−state only.

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

AC CHARACTERISTICS (Note 10; $t_R = t_F = 2.0$ ns; $C_L = 30$ pF; $R_L = 500\ \Omega$)

Symbol	Parameter	Waveform	Limits						Unit
			$T_A = -40°C$ to $+85°C$						
			V_{CC} = 3. 0V to 3.6 V		V_{CC} = 2.3 V to 2.7 V		V_{CC} = 1.65 to 1.95 V		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Dn to On	1	1.1 1.1	3.6 3.6	1.0 1.0	4.5 4.5	1.5 1.5	6.8 6.8	ns
t_{PLH} t_{PHL}	Propagation Delay LE to On	1	1.0 1.0	3.9 3.9	1.0 1.0	4.9 4.9	1.5 1.5	7.8 7.8	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.0 1.0	4.7 4.7	1.0 1.0	6.0 6.0	1.5 1.5	9.2 9.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.4 1.4	4.1 4.1	1.2 1.2	5.1 5.1	1.5 1.5	6.8 6.8	ns
t_s	Setup Time, High or Low Dn to LE	3	1.1		1.0		2.5		ns
t_h	Hold Time, High or Low Dn to LE	3	1.4		1.5		1.0		ns
t_w	LE Pulse Width, High	3	3.3		3.3		4.0		ns
t_{OSHL} t_{OSLH}	Output−to−Output Skew (Note 11)			0.5 0.5		0.5 0.5		0.75 0.75	ns

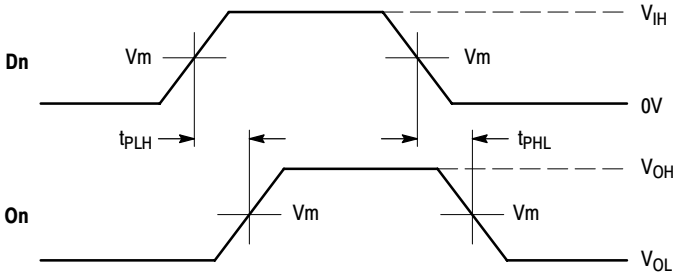
10. For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.
11. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	Note 12	6	pF
C_{OUT}	Output Capacitance	Note 12	7	pF
C_{PD}	Power Dissipation Capacitance	Note 12, 10 MHz	20	pF

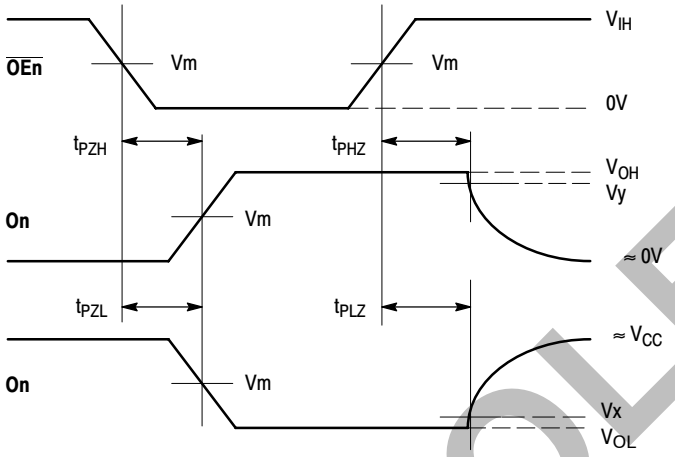
12. V_{CC} = 1.8, 2.5 or 3.3 V; V_I = 0 V or V_{CC}.

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

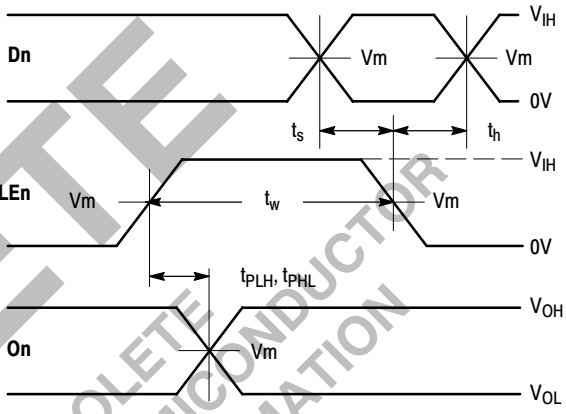


WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F$ = 2.0ns, 10% to 90%; f = 1MHz; t_W = 500ns

Figure 4. AC Waveforms



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.0ns, 10% to 90%; f = 1MHz; t_W = 500ns

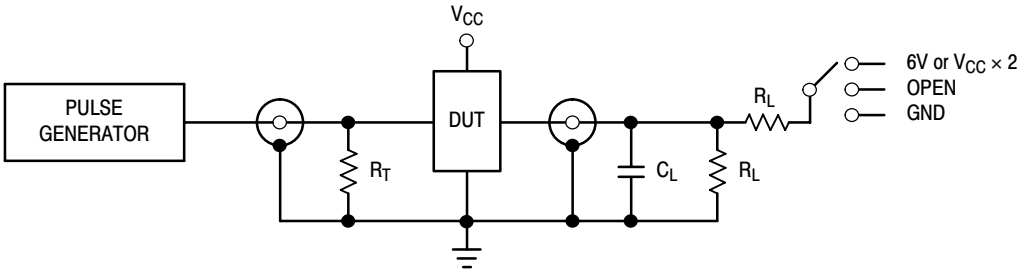


WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES
$t_R = t_F$ = 2.0ns, 10% to 90%; f = 1MHz; t_W = 500ns except when noted

Figure 5. AC Waveforms

Symbol	V_{CC}		
	3.3V ±0.3V	**2.5V ±0.2V**	**1.8V ±0.15V**
V_{IH}	2.7V	V_{CC}	V_{CC}
V_m	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_x	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6 V at V_{CC} = 3.3 ±0.3 V; V_{CC}× 2 at V_{CC} = 2.5 ±0.2 V; 1.8 V ±0.15 V
t_{PZH}, t_{PHZ}	GND

C_L = 30 pF or equivalent (Includes jig and probe capacitance)
R_L = 500 Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 6. Test Circuit

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

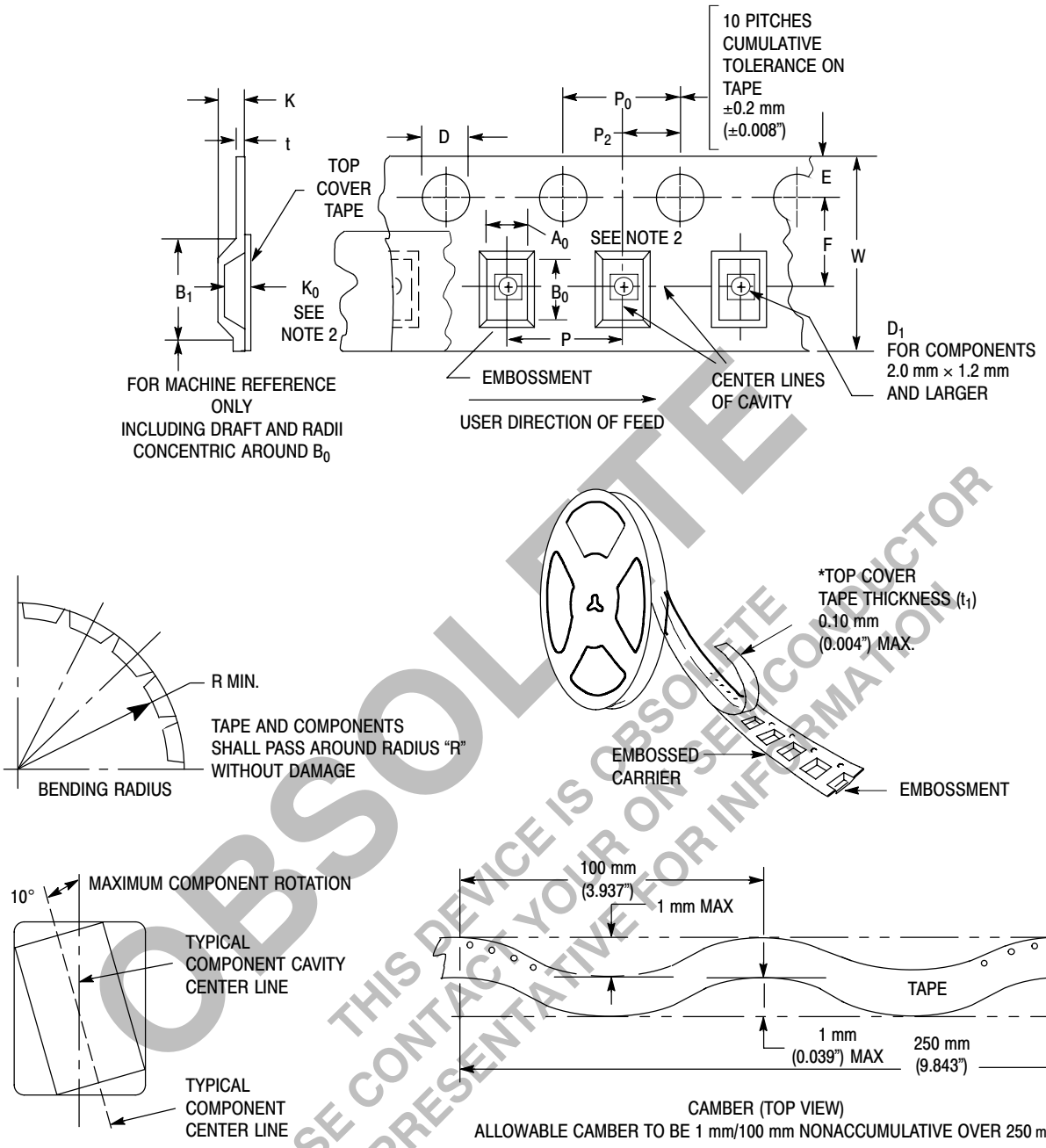


Figure 7. Carrier Tape Specifications

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

EMBOSSED CARRIER DIMENSIONS (See Notes 1 and 2)

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R	T	W
24mm	20.1mm (0.791")	1.5 + 0.1mm −0.0 (0.059 +0.004" −0.0)	1.5mm Min (0.060")	1.75 ±0.1 mm (0.069 ±0.004")	11.5 ±0.10 mm (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 ±0.1 mm (0.63 ±0.004")	4.0 ±0.1 mm (0.157 ±0.004")	2.0 ±0.1 mm (0.079 ±0.004")	30 mm (1.18")	0.6 mm (0.024")	24.3 mm (0.957")

1. Metric Dimensions Govern−English are in parentheses for reference only.
2. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity.

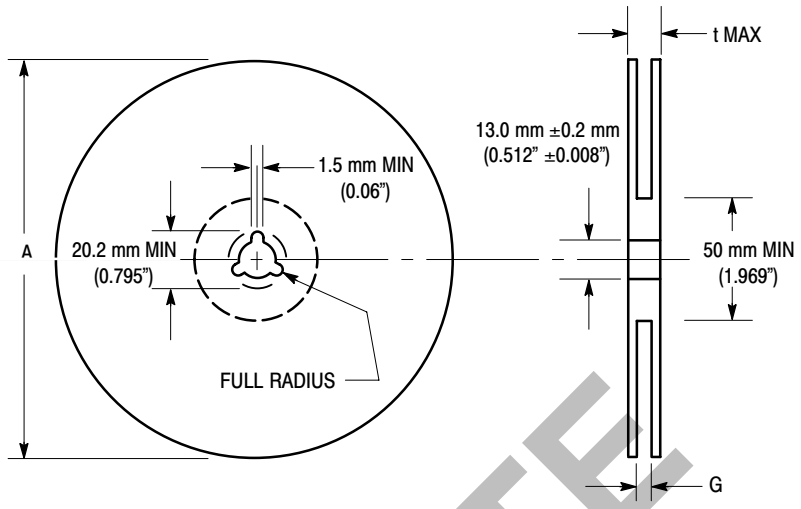


Figure 8. Reel Dimensions

REEL DIMENSIONS

Tape Size	A Max	G	t Max
24 mm	360 mm (14.173")	24.4 mm + 2.0 mm, −0.0 (0.961" + 0.078", −0.00)	30.4 mm (1.197")

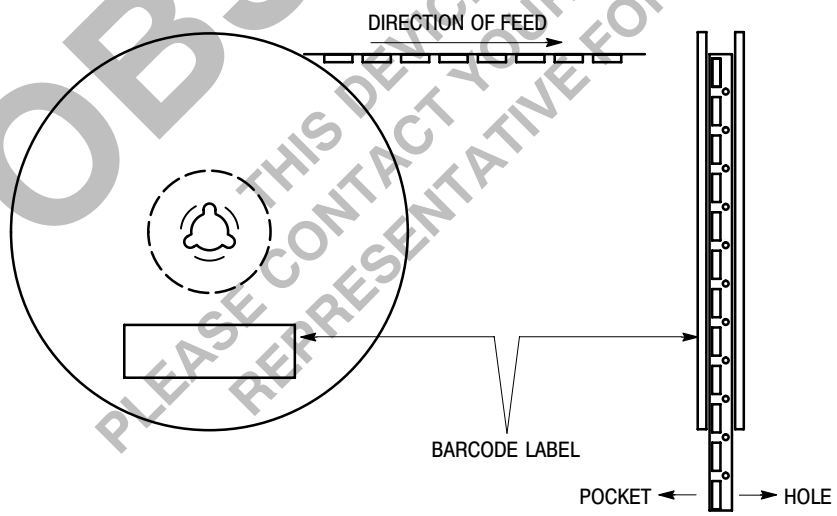


Figure 9. Reel Winding Direction

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

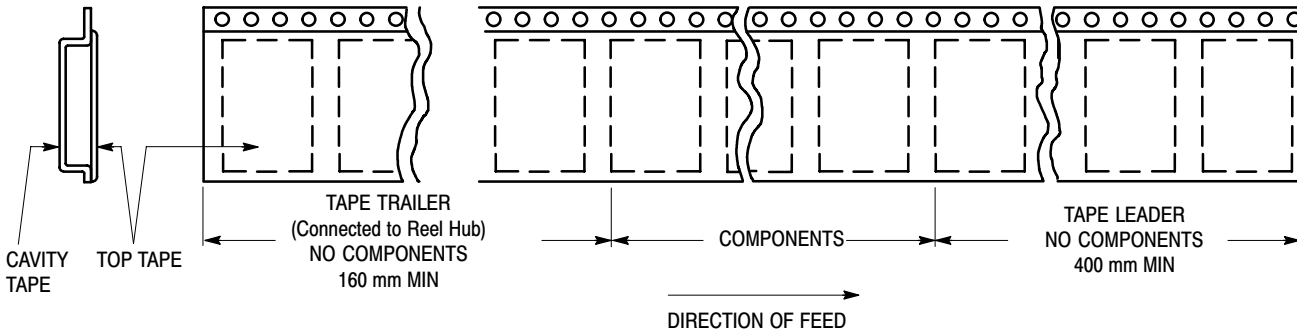


Figure 10. Tape Ends for Finished Goods

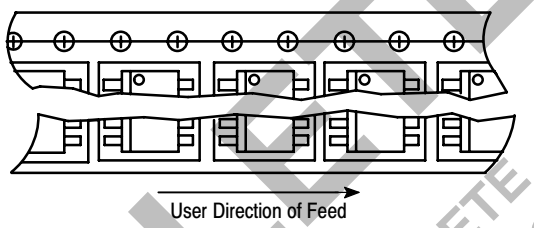


Figure 11. Reel Configuration

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

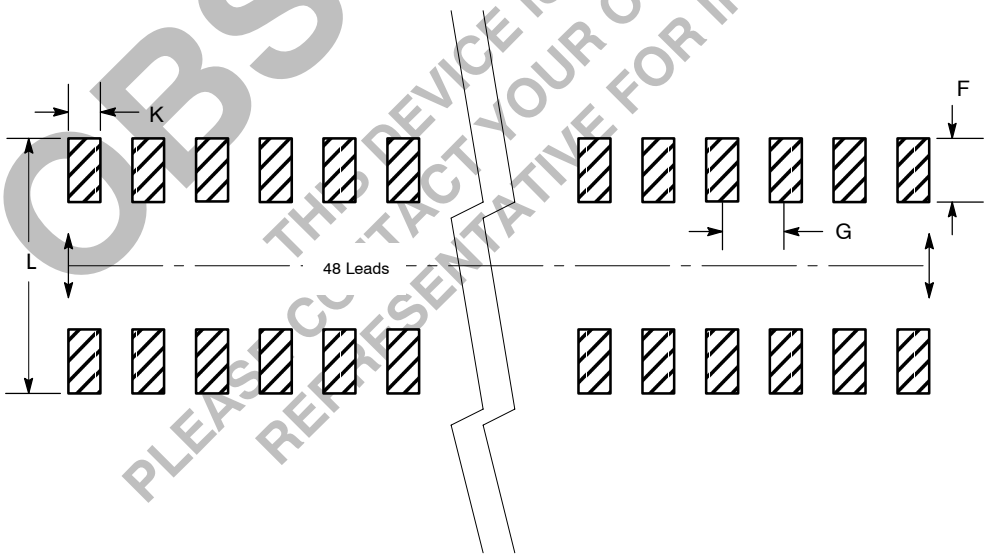
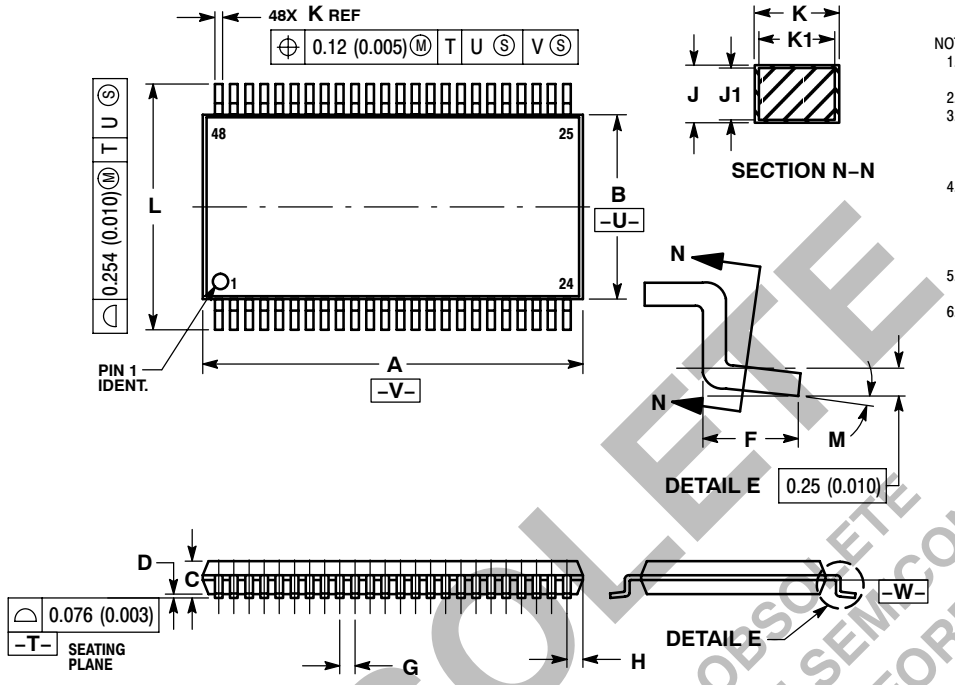


Figure 12. Package Footprint

PACKAGE DIMENSIONS

TSSOP
DT SUFFIX
CASE 1201−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	---	0.015	---
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8 °	0 °	8 °

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative