UCC5304 4-A Source, 6-A Sink Single-Channel Reinforced Isolation Gate Driver With High Noise Immunity

1 Features

- Reinforced isolation
- Single channel in DWV Package with 8.5-mm creepage distance
- CMTI greater than 100-V/ns
- 4-A peak source, 6-A peak sink output
- Switching parameters:
  - 40-ns maximum propagation delay
  - 5-ns maximum delay matching
  - 5.5-ns maximum pulse-width distortion
  - 35-µs maximum VDD power-up delay
- Up to 18-V VDD output drive supply
  - 5-V VDD UVLO
- Operating temp. range (T_A) –40°C to 125°C
- Rejects input pulses shorter than 5-ns
- TTL and CMOS compatible inputs

2 Applications

- AC-DC and DC-DC converters
- Motor drives
- Industrial transportation and robotics

3 Description

The UCC5304 device is an isolated single-channel gate driver with 4-A peak-source and 6-A peak-sink current. It is designed to drive power MOSFETs and GaNFETs in PFC, Isolated AC/DC, DC/DC, and synchronous rectification applications, with fast switching performance and robust ground bounce protection through greater than 100-V/ns common-mode transient immunity (CMTI).

The UCC5304 is available in a 8.5 mm SOIC-8 (DWV) package and can support isolation voltage up to 5-kV_{RMS}. Compared to an optocoupler, the UCC5304 family has lower part-to-part skew, lower propagation delay, higher operating temperature, and higher CMTI.

Protection features include: IN pin rejects input transient shorter than 5-ns; both input and output can withstand –2-V spikes for 200-ns, both supplies have undervoltage lockout (UVLO), and active pull down protection clamps the output below 2.1-V when unpowered or floated.

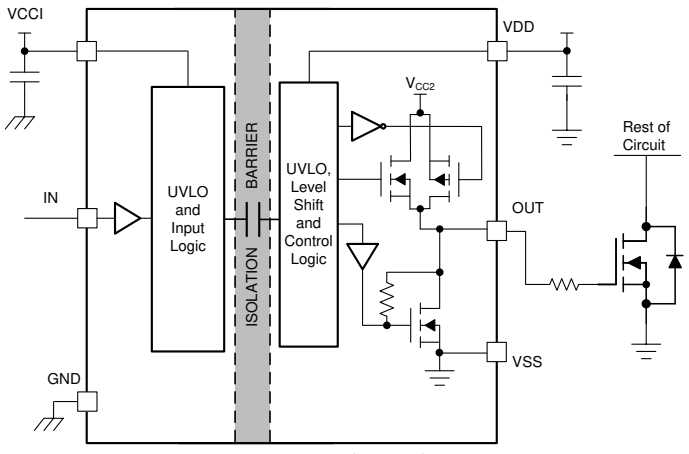
With these features, this device enables high efficiency, high power density, and robustness in a wide variety of power applications.

Device Information[1]

PART NUMBER	PACKAGE	UVLO
UCC5304	DWV-8 (SOIC)	5-V

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

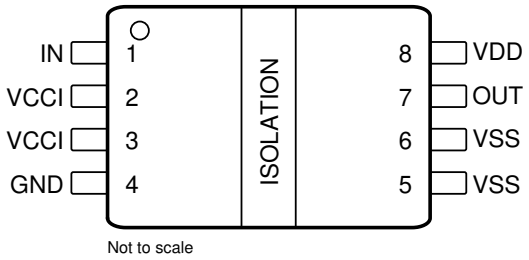
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2020) to Revision B	Page
• Changed marketing status from Advance Information to initial release.	1

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5 Pin Configuration and Functions

DWV Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O(1)	DESCRIPTION
GND	4	P	Primary-side ground reference. All signals in the primary side are referenced to this ground.
IN	1	I	Input signal. IN input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
OUT	7	O	Output of driver. Connect to the gate of the FET or IGBT.
VCCI	2, 3	P	Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible.
VDD	8	P	Secondary-side power for driver. Locally decoupled to VSS using a low ESR/ESL capacitor located as close to the device as possible.
VSS	5, 6	P	Ground for secondary-side driver.

(1) P = power, G = ground, I = input, O = output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input bias pin supply voltage	VCCI to GND	–0.5	6	V
Driver bias supply	VDD-VSS	–0.5	20	V
Output signal voltage	OUT to VSS	–0.5	V_{VDD}+0.5	V
	OUT to VSS, Transient for 200 ns(2)	–2	V_{VDD}+0.5	V
Input signal voltage	IN to GND	–0.5	V_{VCCI}+0.5	V
	IN Transient to GND for 200ns(2)	–2	V_{VCCI}+0.5	V
Junction temperature, T_J (3)		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Values are verified by characterization and are not production tested.
(3) To maintain the recommended operating conditions for T_J, see the Thermal Information .

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VCCI	VCCI Input supply voltage	3	5.5	V
VDD	Driver output bias supply	6.0	18	V
T_J	Junction Temperature	–40	130	°C
T_A	Ambient Temperature	–40	125	°C

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6.4 Thermal Information

THERMAL METRIC(1)		DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	32.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Power Ratings

			VALUE	UNIT
P_D	Power dissipation	VCCI= 5.0 V; VDD = 12 V; IN = 3.3-V, 2.36-MHz 50% duty cycle square wave; 1.0-nF load on OUT	0.700	W
P_{DI}	Power dissipation by transmitter side		0.015	W
P_{DO}	Power dissipation by driver side		0.685	W

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6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance(1)	Shortest pin-to-pin distance through air	> 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	> 8.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test;	1060	V_{RMS}
		DC Voltage	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(4)	Method a, After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 2400\ V_{PK}$, t_m = 10 s	≤ 5	
		Method b1; At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$; t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM} = 2813\ V_{PK}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 sin (2πft), f =1 MHz	0.5	pF
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S =150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5700 V_{RMS}, t = 60 s. (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 6840 V_{RMS}, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

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6.7 Safety-Related Certifications

VDE	UL	CQC
Plan to certify according to DIN V VDE V 0884-11:2017-01	Plan to be recognized under UL 1577 Component Recognition Program	Plan to certify according to GB 4943.1-2011

6.8 Safety-Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	SIDE	MIN	TYP	MAX	UNIT
I_S	Safety output supply current	$R_{\theta JA}$ = 108.5ºC/W, V_{VDD} = 12 V, T_J = 150°C, T_A = 25°C See	DRIVER side			96	mA
P_S	Safety supply power	$R_{\theta JA}$ = 108.5ºC/W, V_{VCCI} = 5.5 V, T_J = 150°C, T_A = 25°C See	INPUT side			0.015	W
			DRIVER side			1.135	
			TOTAL			1.150	
T_S	Safety temperature(1)					150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the ***Thermal Information*** table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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6.9 Electrical Characteristics

V_{VCCI} = 3.3 V or 5.0 V, 0.1-µF capacitor from VCCI to GND and 1uF capacitor from VDD to VSS, V_{VDD} = 12 V, 1-µF capacitor from VDD to VSS, T_A = –40°C to +125°C, unless otherwise noted(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCCI}	VCCI quiescent current	V_{IN} = 0 V		1.5	2.0	mA
I_{VDD}	VDD quiescent current	V_{IN} = 0 V,		1.0	1.8	mA
I_{VCCI}	VCCI operating current	(f = 500 kHz) operating current		2.5		mA
I_{VDD}	VDD operating current	(f = 500 kHz) operating current C_{OUT} = 100 pF, V_{VDD} = 12 V		2.5		mA
VCC SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V_{VCCI_ON}	UVLO Rising threshold		2.55	2.7	2.85	V
V_{VCCI_OFF}	UVLO Falling threshold		2.35	2.5	2.65	V
V_{VCCI_HYS}	UVLO Threshold hysteresis			0.2		V
VDD SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V_{VDD}	UVLO Rising threshold		5.0	5.5	5.9	V
V_{VDD_OFF}	UVLO Falling threshold		4.7	5.2	5.6	V
V_{VDD_HYS}	UVLO Threshold hysteresis			0.3		V
IN						
V_{INH}	Input high threshold voltage		1.6	1.8	2	V
V_{INL}	Input low threshold voltage		0.8	1	1.25	V
V_{IN_HYS}	Input threshold hysteresis			0.8		V
OUTPUT						
I_{O+}	Peak output source current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz, bench measurement		4		A
I_{O-}	Peak output sink current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz, bench measurement		6		A
R_{OH}	Output resistance at high state	I_{OUT} = –10 mA, R_{OHA}, R_{OHB} do not represent drive pull-up performance. See t_{RISE} in Switching Characteristics and Output Stage for more details.		5		Ω
R_{OL}	Output resistance at low state	I_{OUT} = 10 mA		0.55		Ω
V_{OH}	Output voltage at high state	V_{VDD} = 12 V, I_{OUT} = –10 mA		11.95		V
V_{OL}	Output voltage at low state	V_{VDD} = 12 V, I_{OUT} = 10 mA		5.5		mV
V_{OAPD}	Driver output (V_{OUT}) active pull down	V_{VDD}, I_{OUT} = 200 mA		1.75	2.1	V

(1) Current direction in the testing conditions are defined to be positive into the pin and negative out of the specified terminal (unless otherwise noted).
(2) Parameters that has only typical values, are not production tested and guaranteed by design.

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6.10 Switching Characteristics

V_{VCCI} = 3.3 V or 5.5 V, 0.1-µF capacitor from VCCI to GND, V_{VDD} = 12 V, 1-µF capacitor from VDD and VSS, load capacitance C_{OUT} = 0 pF, T_J = –40°C to +125°C, unless otherwise noted(1).

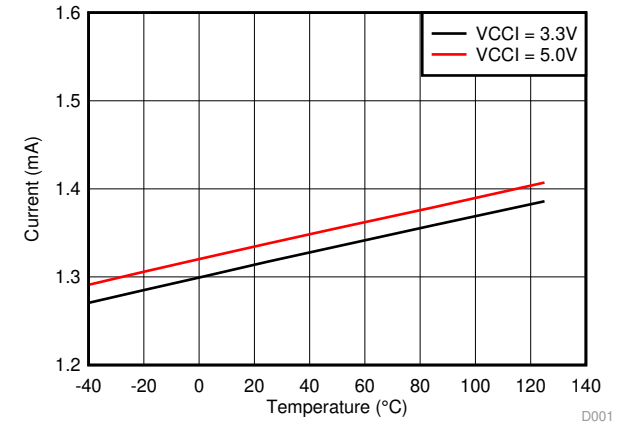
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RISE}	Output rise time, see Figure 17	C_{VDD} = 10 µF, C_{OUT} = 1.8 nF, V_{VDD} = 12 V, f = 1 kHz		5	16	ns
t_{FALL}	Output fall time, see Figure 17	C_{VDD} = 10 µF, C_{OUT} = 1.8 nF , V_{VDD} = 12 V, f = 1 kHz		6	12	ns
t_{PWmin}	Minimum input pulse width that passes to output, see and	Output does not change the state if input signal less than t_{PWmin}		10	20	ns
t_{PDHL}	Propagation delay at falling edge, see	INx high threshold, V_{INH}, to 10% of the output		28	40	ns
t_{PDLH}	Propagation delay at rising edge, see	INx low threshold, V_{INL}, to 90% of the output		28	40	ns
t_{PWD}	Pulse width distortion in each channel, see	$\lvert t_{PDLH} - t_{PDHL} \rvert$			5.5	ns
$t_{VCCI+ to OUT}$	VCCI Power-up Delay Time: UVLO Rise to OUT, See Figure 18	IN tied to VCCI		40	59	µs
$t_{VDD+ to OUT}$	VDD Power-up Delay Time: UVLO Rise to OUT See Figure 19	INtied to VCCI		22	35	µs
$\lvert CM_H \rvert$	High-level common-mode transient immunity (See)	Slew rate of GND vs. VSS, IN is tied to GND or VCCI; V_{CM}=1000 V;	100			V/ns
$\lvert CM_L \rvert$	Low-level common-mode transient immunity (See)	Slew rate of GND vs. VSS, IN is tied to GND or VCCI; V_{CM}=1000 V;	100			V/ns

(1) Parameters that has only typical values, are not production tested and guaranteed by design.

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6.11 Typical Characteristics

VDD = 12 V, VCCI = 3.3 V or 5.0 V, T_A = 25°C, C_L=0pF unless otherwise noted.



No Load IN = GND

Figure 1. VCCI Quiescent Current

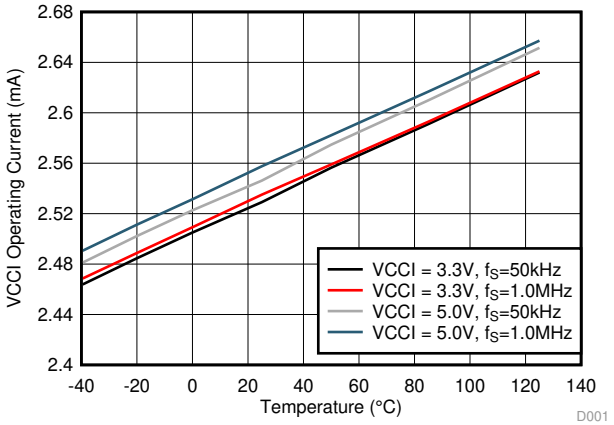


Figure 2. VCCI Operating Current - I_{VCCI}

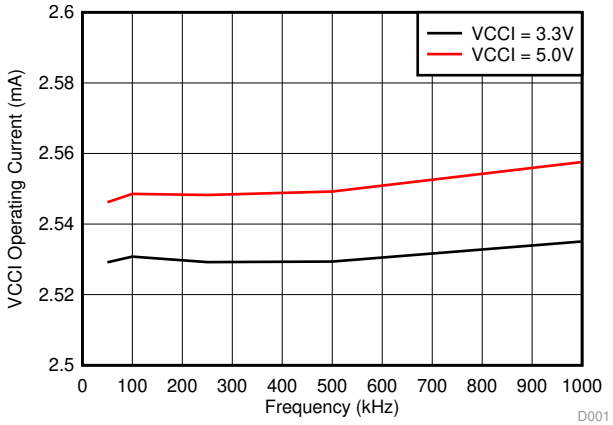
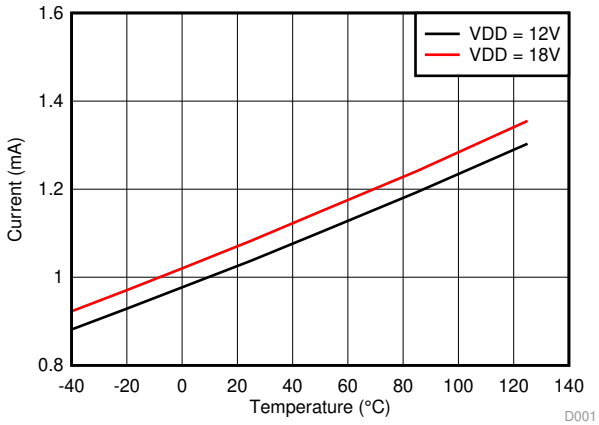
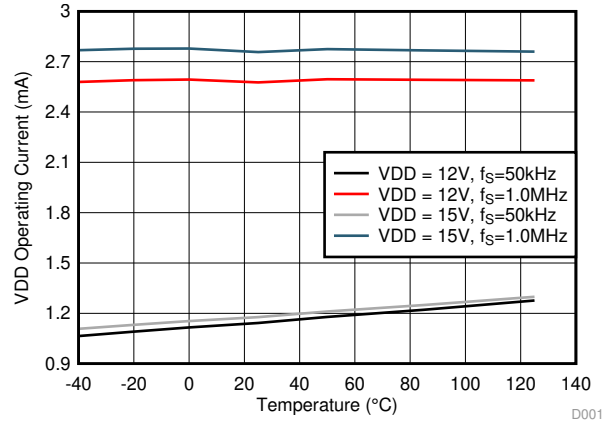


Figure 3. VCCI Operating Current vs. Frequency



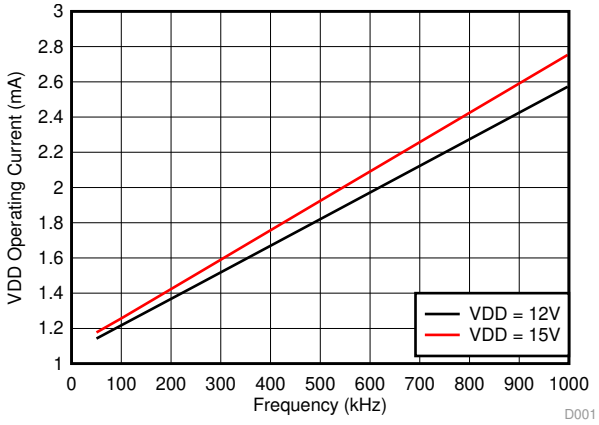
No Load IN = GND

Figure 4. VDD Quiescent Current (I_{VDD})



No Load

Figure 5. VDD Channel Operating Current (I_{VDD})



No Load IN pin switching

Figure 6. Operating Current (I_{VDD}) vs. Frequency

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Typical Characteristics (continued)

VDD = 12 V, VCCI = 3.3 V or 5.0 V, T_A = 25°C, C_L=0pF unless otherwise noted.

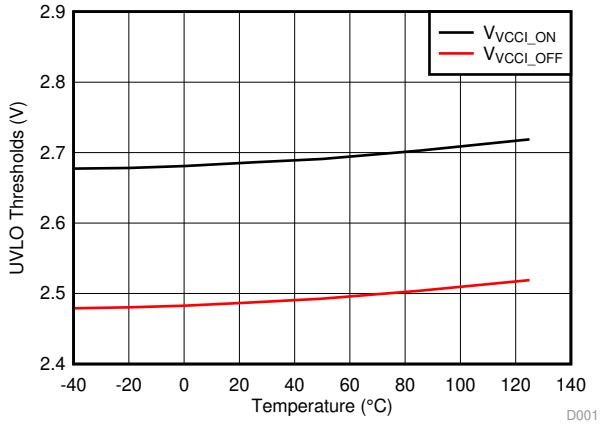


Figure 7. VCCI UVLO Threshold Voltage

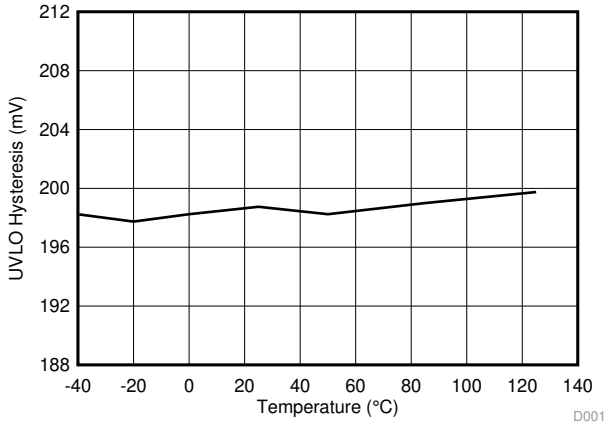


Figure 8. VCCI UVLO Threshold Hysteresis Voltage

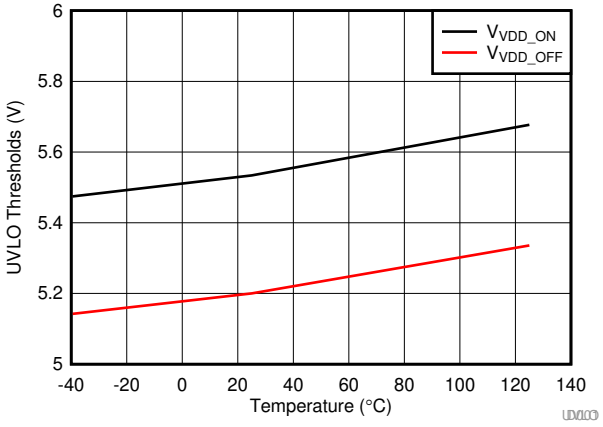


Figure 9. VDD Supply UVLO Threshold Voltage

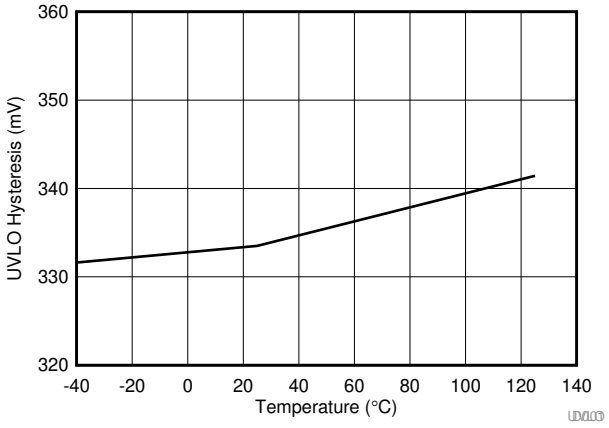


Figure 10. VDD Supply UVLO Threshold Hysteresis

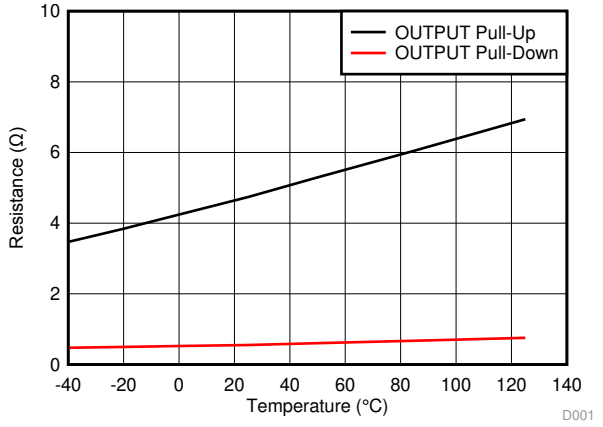


Figure 11. OUT Pullup and Pulldown Resistance

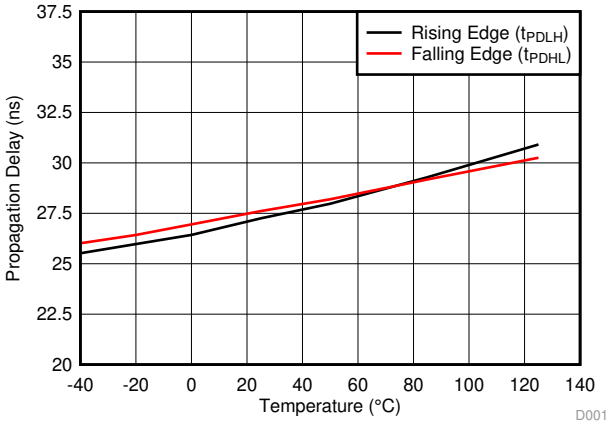
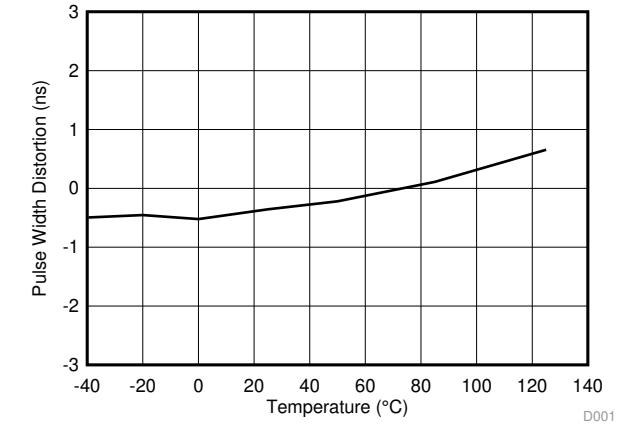


Figure 12. Propagation Delay, Rising and Falling Edge

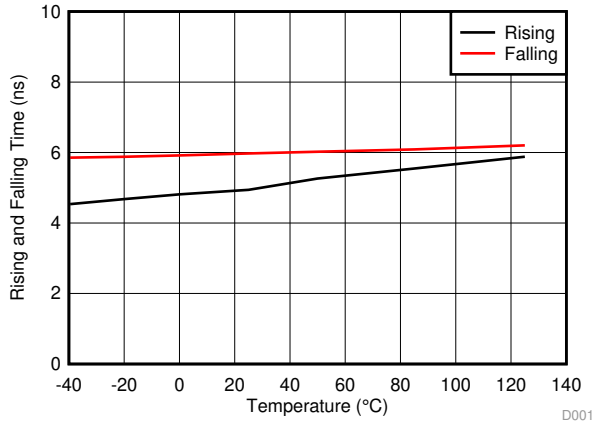
Typical Characteristics (continued)

VDD = 12 V, VCCI = 3.3 V or 5.0 V, T_A = 25°C, C_L=0pF unless otherwise noted.



$t_{PDLH} - t_{PDHL}$

Figure 13. Pulse Width Distortion



C_L = 1.8 nF

Figure 14. Rise Time and Fall Time

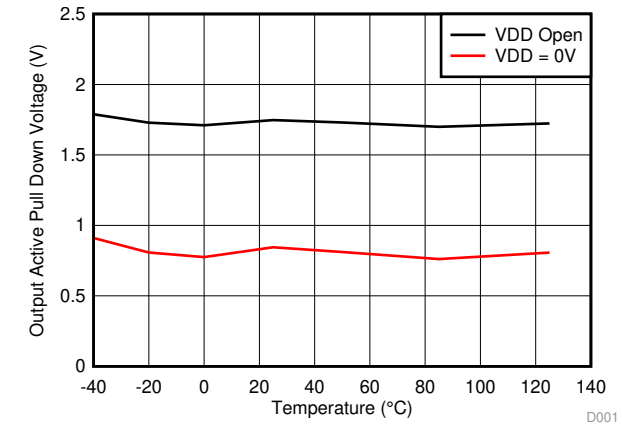


Figure 15. OUTPUT Active Pulldown Voltage

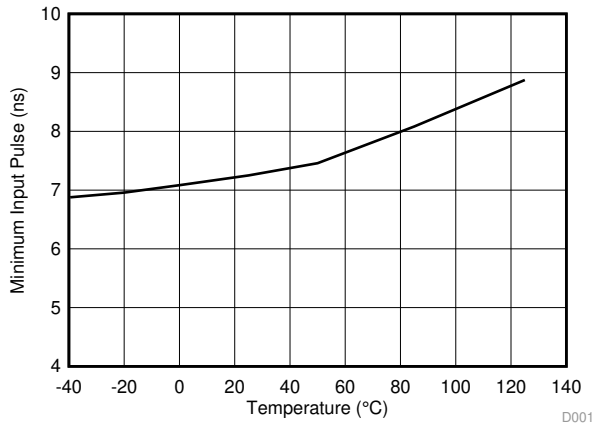


Figure 16. Minimum Pulse that Changes Output

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7 Parameter Measurement Information

7.1 Rising and Falling Time

Figure 17 shows the criteria for measuring rising (t_{RISE}) and falling (t_{FALL}) times. For more information on how short rising and falling times are achieved see Output Stage

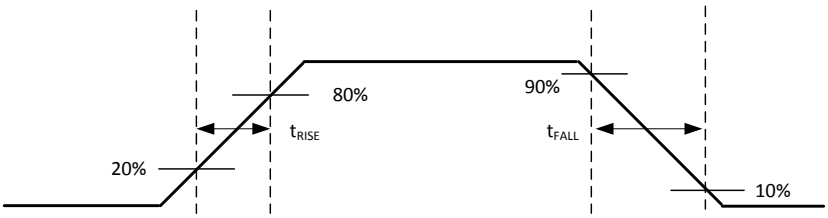


Figure 17. Rising and Falling Time Criteria

7.2 Power-up UVLO Delay to OUTPUT

Before the driver is ready to deliver a proper output state, there is a power-up delay from the UVLO rising edge to output and it is defined as $t_{VCCI+\ to\ OUT}$ for VCCI UVLO, which is 40 µs typically, and $t_{VDD+\ to\ OUT}$ for VDD UVLO, which is 22 µs typically. It is recommended to allow proper delay margin after the driver VCCI and VDD bias supplies are ready before applying the PWM signal at the IN pin. Figure 18 and Figure 19 show the power-up UVLO delay timing diagram for VCCI and VDD.

If the IN pin is active before VCCI or VDD have crossed above their respective on thresholds, the output will not update until $t_{VCCI+\ to\ OUT}$ or $t_{VDD+\ to\ OUT}$ after VCCI or VDD crossing its UVLO rising threshold. However, when either VCCI or VDD receive a voltage less than their respective off thresholds, there is <1µs delay, depending on the voltage slew rate on the supply pins, before the outputs are held low. This asymmetric delay is designed to ensure safe operation during VCCI or VDD brownouts.

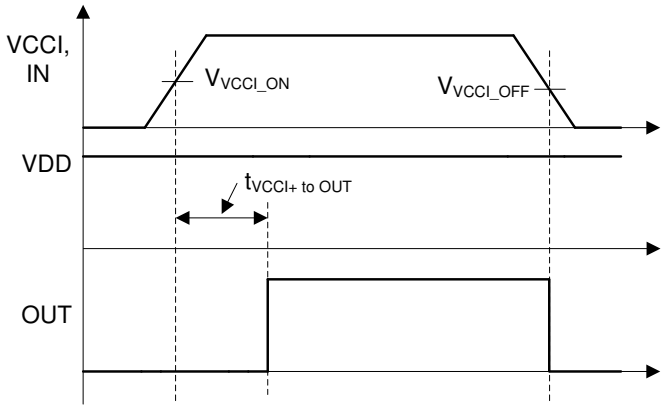


Figure 18. VCCI Power-up UVLO Delay

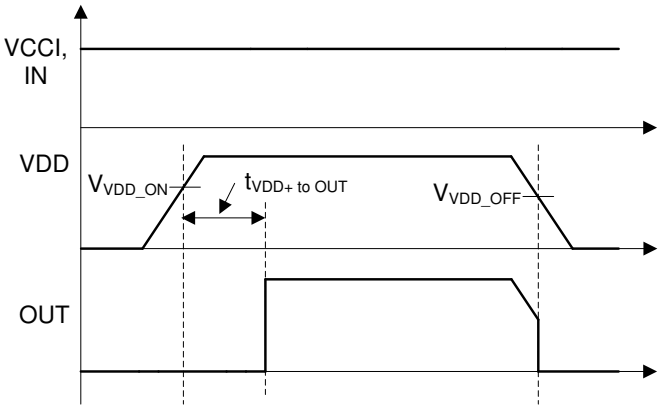


Figure 19. VDD Power-up UVLO Delay

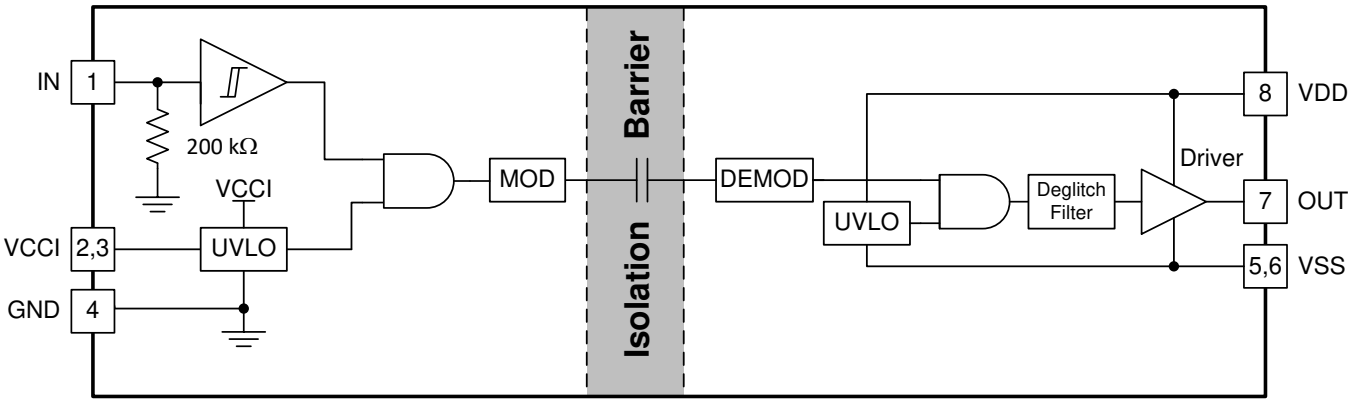
8 Detailed Description

8.1 Overview

In order to switch power transistors rapidly and reduce switching power losses, high-current gate drivers are often placed between the output of control devices and the gates of power transistors. There are several instances where controllers are not capable of delivering sufficient current to drive the gates of power transistors. This is especially the case with digital controllers, since the input signal from the digital controller is often a 3.3-V logic signal capable of only delivering a few mA.

The UCC5304 is a flexible gate driver that can be configured to fit a variety of power supply and motor drive topologies, as well as drive several types of transistors. UCC5304 has many features that allow it to integrate well with control circuitry and protect the gates it drives such as under voltage lock-out (UVLO) for both input and output voltages. The UCC5304 holds its output low when the input is left open or when the input pulse is not wide enough. The driver input pin is CMOS and TTL compatible for interfacing with digital and analog power controllers alike.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 VDD, VCCI, and Under Voltage Lock Out (UVLO)

The UCC5304 has an internal under voltage lock out (UVLO) protection feature on the supply circuit blocks between the VDD and VSS pins. When the VDD bias voltage is lower than V_{VDD_ON} at device start-up or lower than V_{VDD_OFF} after start-up, the VDD UVLO feature holds the effected output low, regardless of the status of the IN pin.

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs (Illustrated in Figure 20). In this condition, the upper PMOS is resistively held off by R_{Hi-Z} while the lower NMOS gate is tied to the driver output through R_{CLAMP}. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, typically around 1.5V, when no bias power is available.

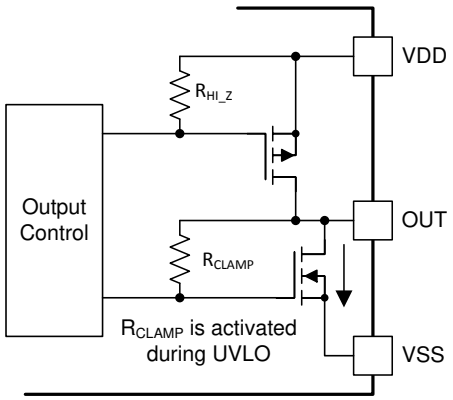


Figure 20. Simplified Representation of Active Pull Down Feature

The VDD UVLO protection has a hysteresis feature (V_{VDD_HYS}). This hysteresis prevents chatter when there is ground noise from the power supply. Also this allows the device to accept small drops in bias voltage, which is bound to happen when the device starts switching and operating current consumption increases suddenly.

The input side of the UCC5304 also has an internal under voltage lock out (UVLO) protection feature. The device isn't active unless the VCCI voltage exceeds V_{VCCI_ON} on start up. The input signal will not be delivered when the VCCI suply is less than V_{VCCI_OFF}. And, just like the UVLO for VDD, there is hystersis (V_{VCCI_HYS}) to ensure stable operation.

Table 1. VCCI UVLO Feature Logic

CONDITION	INPUT	OUTPUT
	IN	OUT
VCCI-GND < V_{VCCI_ON} before device start up	H	L
VCCI-GND < V_{VCCI_ON} before device start up	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	L

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Table 2. VDD UVLO Feature Logic

CONDITION	INPUT	OUTPUT
	IN	OUT
VDD-VSS < V_{VDD_ON} before device start up	H	L
VDD-VSS < V_{VDD_ON} before device start up	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	L
VDD-VSS < V_{VDD_OFF} after device start up	L	L

8.3.2 Input Stage

The input pin of UCC5304 is based on a TTL and CMOS compatible input-threshold logic that is totally isolated from the VDD supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V micro-controllers), since the UCC5304 has a typical high threshold (V_{INAH}) of 1.8 V and a typical low threshold of 1 V, which vary little with temperature (see and). A wide hysterisis (V_{INA_HYS}) of 0.8 V makes for good noise immunity and stable operation. If the input is ever left open, an internal pull-down resistor forces the pin low. This resistance is typically 200 kΩ (see Functional Block Diagram).

Since the input side of UCC5304 is isolated from the output drivers, the input signal amplitude can be larger or smaller than VDD, provided that it doesn't exceed the recommended limit. This allows greater flexibility when integrating with control signal sources, and allows the user to choose the most efficient VDD for their MOSFET/IGBT gate. That said, the amplitude of any signal applied to IN must not exceed VCCI.

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8.3.3 Output Stage

The UCC5304 output stage features a pull-up structure which delivers the highest peak-source current when it is most needed — during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional *Pull-Up* N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a boost in the peak-sourcing current, enabling fast turn on. This is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. The on-resistance of this N-channel MOSFET (R_{NMOS}) is approximately 1.47 Ω when activated.

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-channel device only. This is because the *Pull-Up* N-channel device is held in the off state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore the effective resistance of the UCC5304 pull-up stage during this brief turn-on phase is much lower than what is represented by the R_{OH} parameter.

The pull-down structure of the UCC5304 is comprised of an N-channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pull-down state in the device. The output of the UCC5304 is capable of delivering 4-A peak source and 6-A peak sink current pulses. The output voltage swings between VDD and VSS provides rail-to-rail operation, thanks to the MOS-out stage which delivers very low drop-out.

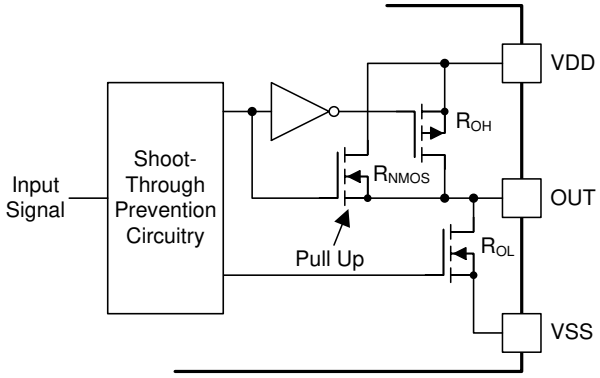


Figure 21. Output Stage

8.4 Device Functional Modes

Assume VCCI and VDD are powered up. See VDD, VCCI, and Under Voltage Lock Out (UVLO) for more information on UVLO operation modes. Table 3 lists the UCC5304's functional modes.

Table 3. INPUT/OUTPUT Logic Table

IN	OUT	NOTE
L	L	
H	H	
OPEN	L	It is recommended to pull IN to ground to achieve better noise immunity if the system has an operational mode that does not assert the input either HIGH or LOW

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCC5304 effectively combines both isolation and buffer-drive functions. The flexible, universal capability of the UCC5304 (with up to 5.5-V VCCI and 18-V VDD) allows the device to be used as a low-side or high-side gate driver for MOSFETs, IGBTs or GaN transistors. With integrated components, advanced protection features (UVLO and disable) and optimized switching performance; the UCC5304 enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

9.2 Typical Application

The circuit in Figure 22 shows a reference design with two UCC5304 devices driving a typical half-bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and 3-phase motor drive applications.

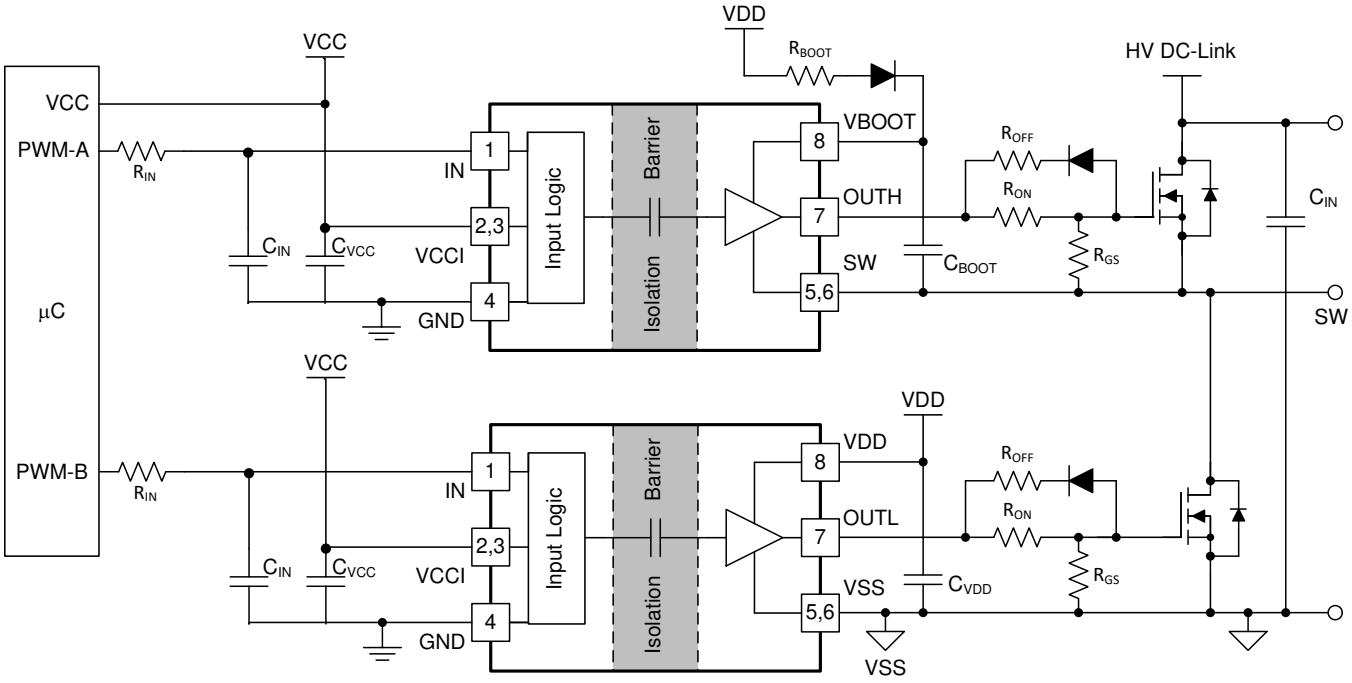


Figure 22. Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

Table 4 lists reference design parameters for an example application: UCC5304 driving a 650-V MOSFET.

Table 4. UCC5304 Design Requirements

PARAMETER	VALUE	UNITS
Power transistor	IPP65R150CFD	-
VCC	5.0	V
VDD	12	V
Input signal amplitude	3.3	V
Switching frequency (f_s)	100	kHz
DC link voltage	400	V

9.2.2 Detailed Design Procedure

9.2.2.1 Designing IN pin Input Filter

It is recommended that users avoid shaping the signal to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input R_{IN}-C_{IN} filter can be used to filter out the ringing introduced by non-ideal layout or long PCB traces.

Such a filter should use an R_{IN} in the range of 0 Ω to100 Ω and a C_{IN} between 10 pF and 100 pF. In the example, an R_{IN} = 51 Ω and a C_{IN} = 33 pF are selected, with a corner frequency of approximately 100 MHz.

When selecting these components, it is important to pay attention to the trade-off between good noise immunity and propagation delay.

9.2.2.2 Estimating Junction Temperature

The junction temperature (T_J) of the UCC5304 can be estimated with:

$$T_J = T_C + \Psi_{JT} \times P_{GD}$$

where

- T_C is the UCC5304 case-top temperature measured with a thermocouple or some other instrument, ψ_{JT} is the junction-to-top characterization parameter from the Thermal Information table. Importantly, ψ_{JT} is developed based on JEDEC standard PCB board and it is subject to change when the PCB board layout is different. For more information, please visit application report - semiconductor and IC package thermal metrics. (1)

Using the junction-to-top characterization parameter (Ψ_{JT}) instead of the junction-to-case thermal resistance ($R_{\Theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). $R_{\Theta JC}$ can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heatsink is applied to an IC package. In all other cases, use of $R_{\Theta JC}$ will inaccurately estimate the true junction temperature. Ψ_{JT} is experimentally derived by assuming that the amount of energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimates can be made accurately to within a few degrees Celsius. For more information, see the Layout Guidelines and Semiconductor and IC Package Thermal Metrics application report.

9.2.2.3 Selecting VCCI and VDD Capacitors

Bypass capacitors for VCCI and VDD are essential for achieving reliable performance. It is recommended that one choose low ESR and low ESL surface-mount multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients and capacitance tolerances. Importantly, DC bias on an MLCC will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15 V_{DC} is applied.

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9.2.2.3.1 Selecting a VCCI Capacitor

A bypass capacitor connected to VCCI supports the transient current needed for the primary logic and the total current consumption, which is only a few mA. Therefore, a 25-V MLCC with over 100 nF is recommended for this application. If the bias power supply output is a relatively long distance from the VCCI pin, a tantalum or electrolytic capacitor, with a value over 1 µF, should be placed in parallel with the MLCC.

9.2.2.3.2 Selecting a VDD Capacitor

A 50-V, 10-µF MLCC and a 50-V, 220-nF MLCC are chosen for C_{VDD}. If the bias power supply output is a relatively long distance from the VDD pin, a tantalum or electrolytic capacitor with a value over 10 µF, should be used in parallel with C_{VDD}.

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10 Power Supply Recommendations

The recommended input supply voltage (VCCI) for UCC5304 is between 3 V and 5.5 V. The output bias supply voltage (VDD) range from 9.2V to 18V. The lower end of this bias supply range is governed by the internal under voltage lockout (UVLO) protection feature of each device. One mustn't let VDD or VCCI fall below their respective UVLO thresholds (For more information on UVLO see VDD, VCCI, and Under Voltage Lock Out (UVLO)). The upper end of the VDD range depends on the maximum gate voltage of the power device being driven by UCC5304. The UCC5304 has a recommended maximum VDD of 18 V.

A local bypass capacitor should be placed between the VDD and VSS pins. This capacitor should be positioned as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is further suggested that one place two such capacitors: one with a value of ≈10-µF for device biasing, and an additional ≤100-nF capacitor in parallel for high frequency filtering..

Similarly, a bypass capacitor should also be placed between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of UCC5304, this bypass capacitor has a minimum recommended value of 100 nF.

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11 Layout

11.1 Layout Guidelines

Consider these PCB layout guidelines for in order to achieve optimum performance for the UCC5304.

11.1.1 Component Placement Considerations

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the switch node VSS pin in a half-bridge application, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.

11.1.2 Grounding Considerations

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This will decrease the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.

11.1.3 High-Voltage Considerations

- To ensure isolation performance between the primary and secondary side, one should avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the UCC5304 isolation performance.
- For half-bridge, or high-side/low-side configurations, one should try to increase the clearance distance of the PCB layout between the high and low-side PCB traces.

11.1.4 Thermal Considerations

- A large amount of power may be dissipated by the UCC5304 if the driving voltage is high, the load is heavy, or the switching frequency is high (Refer to for more details). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to VDD and VSS pins is recommended, with priority on maximizing the connection to VSS (See and). However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VDD and VSS pins to internal ground or power planes through multiple vias of adequate size. Ensure that no traces or coppers from different high-voltage planes overlap.

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11.2 Layout Example

Figure 23 shows a 2-layer PCB layout example.

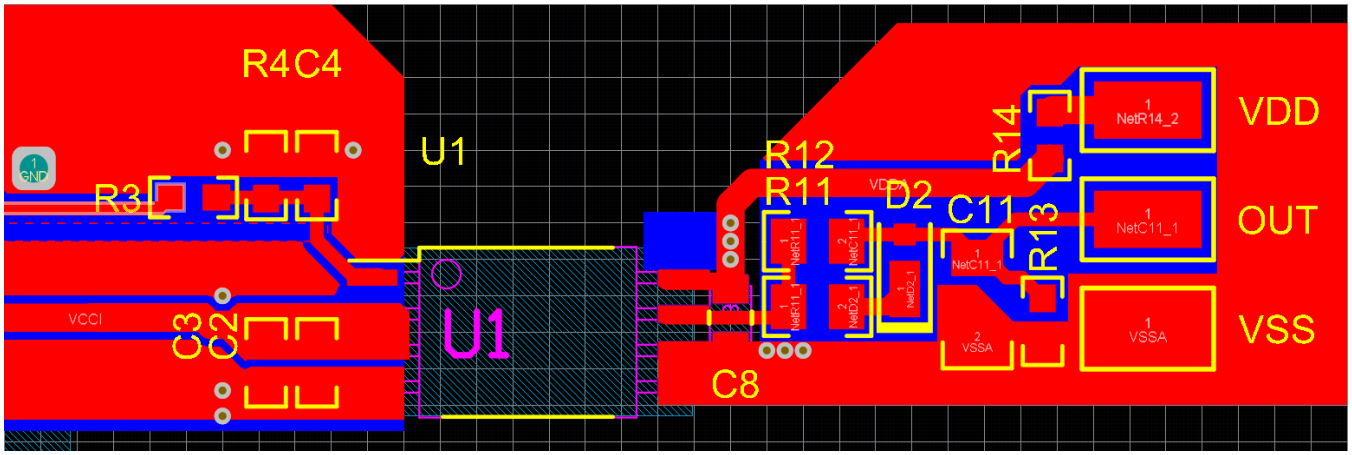


Figure 23. Layout Example

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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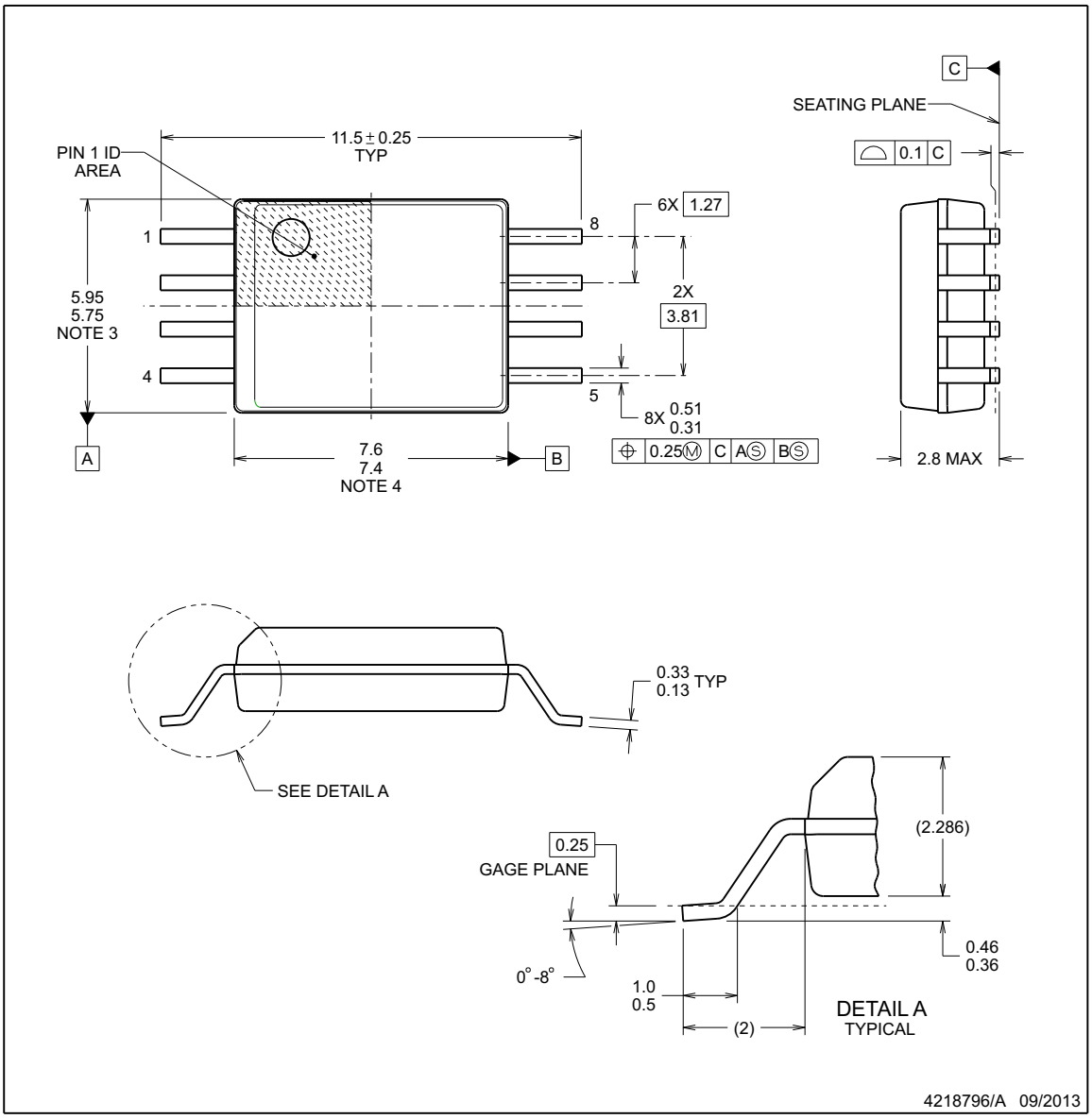
PACKAGE OUTLINE



DWV0008A

SOIC - 2.8 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

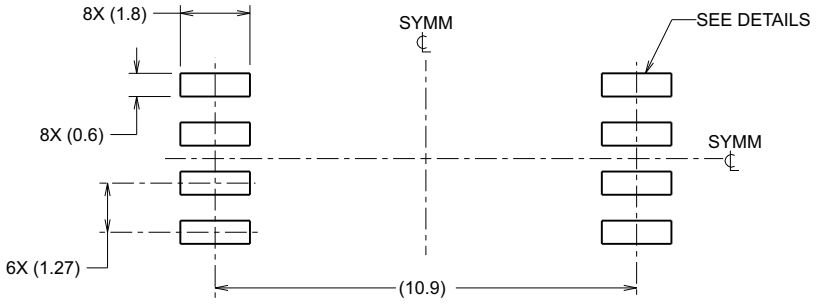
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EXAMPLE BOARD LAYOUT

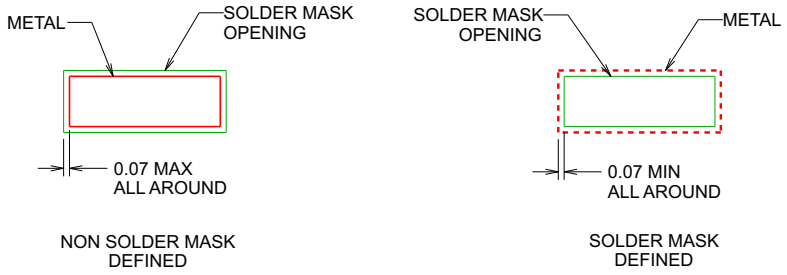
DWV0008A

SOIC - 2.8 mm max height

SOIC



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

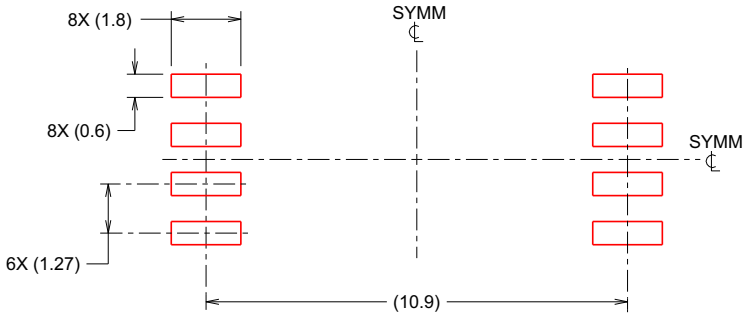
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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EXAMPLE STENCIL DESIGN

DWV0008A — SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC5304DWV	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC5304	Samples
UCC5304DWVR	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC5304	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

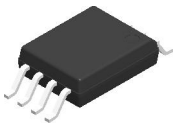
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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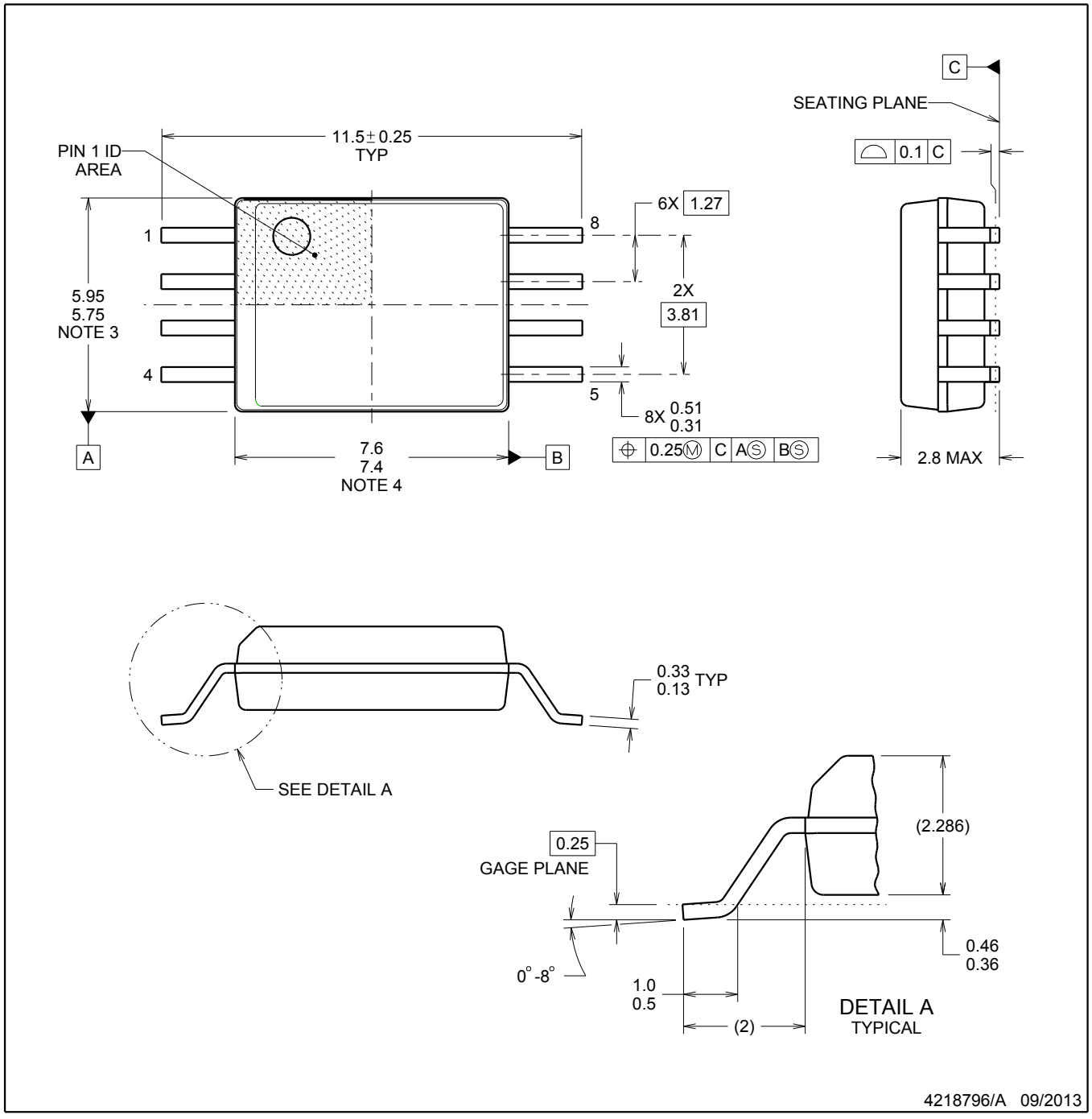
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DWV0008A

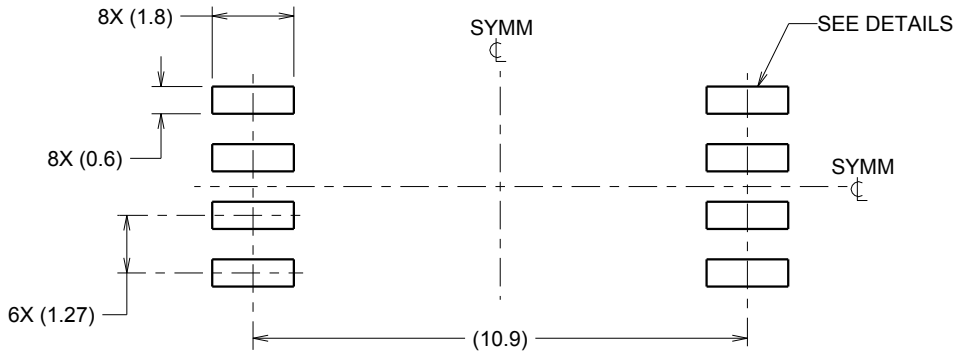
SOIC - 2.8 mm max height

SOIC

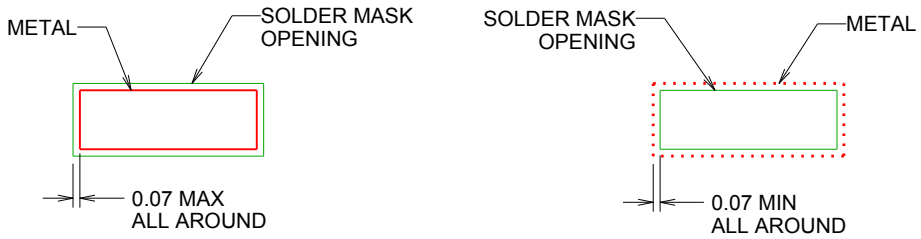


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

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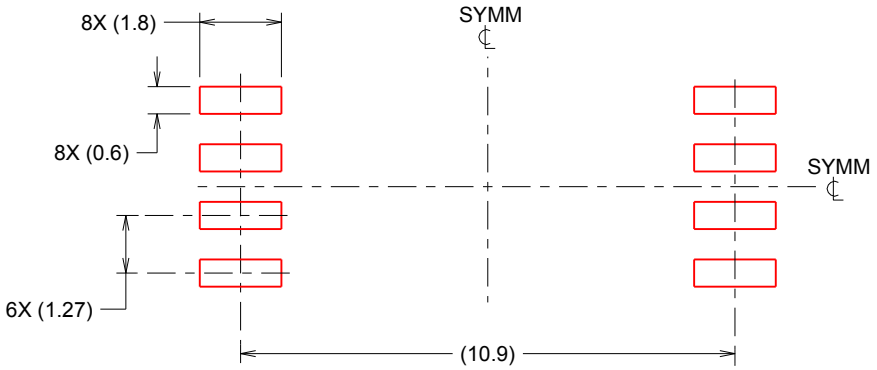
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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