Six-Channel Active DC Output Controller, Monitor, Marginer and Sequencer

FEATURES & APPLICATIONS

- **Extremely accurate (±0.2%) Active DC Output Control (ADOC™)**
- **Undervoltage Lockout function (UVLO)**
- **ADOC™ Automatically adjusts supply output voltage level under all DC load conditions**
- **Monitors, controls, sequences and margins up to six supplies from 0.3V to 5.5V with 1.25V Vref**
- **Wide Margin/ADOC range from 0.3V to VDD**
- **Programmable Power-on/-off sequencing**
- **Monitors internal temperature sensor**
- **Operates from any intermediate bus supply from 8V to 15V and from 2.7V to 5.5V**
- **Monitors 12V input and VDD**
- **Monitors two general-purpose 10-bit ADC inputs**
- **Programmable threshold limits (2 OV/2 UV) for each monitored input**
- **Programmable RESET, HEALTHY and FAULT**
- **4k-bit general purpose nonvolatile memory**
- **I²C 2-wire serial bus for programming configuration and monitoring status, including 10-bit ADC conversion results**

Applications

- **Monitor/Control Distributed and POL Supplies**
- **Multi-voltage Processors, DSPs, ASICs used in Telecom, CompactPCI or server systems**

INTRODUCTION

The SMM665C is an Active DC Output power supply Controller (ADOC™) that monitors, margins and cascade sequences. The ADOC feature is unique and maintains extremely accurate settings of system supply voltages to within ±0.2% under full load. The device actively controls up to six DC/DC converters that use a Trim or Regulator VADJ/FB pin to adjust the output voltage. For system test, the part also controls margining of the supplies using I²C commands. It can margin supplies with either positive or negative control within a range of 0.3V to VDD depending on the specified range of the converter. The SMM665C also intelligently sequences or cascades the power supplies on and off in any order using enable outputs with programmable polarity. It can operate off any intermediate bus supply ranging from 8V to 15V or from 5.5V to as low as 2.7V. The part monitors six power supply channels as well as VDD, 12V input, two general-purpose analog inputs and an internal temperature sensor using a 10-bit ADC. The 10-bit ADC can measure the value on any one of the monitor channels and output the data via the I²C bus. A host system can communicate with the SMM665C status register, optionally control Power-on/off, margining and utilize 4K-bits of nonvolatile memory.

SIMPLIFIED APPLICATIONS DRAWING

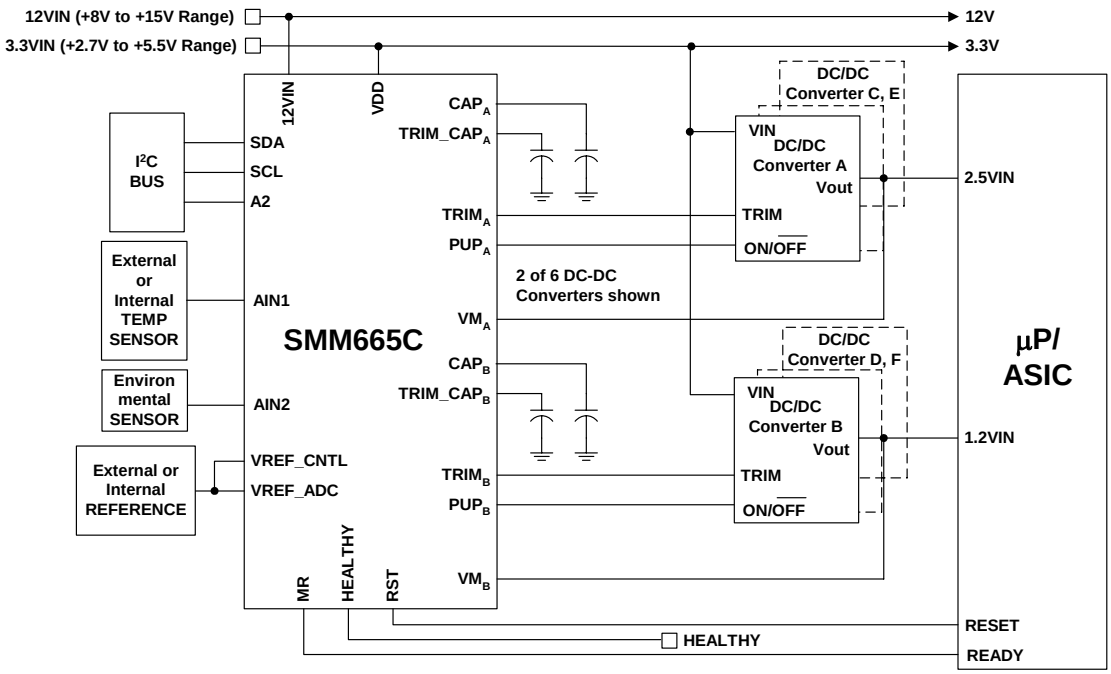


Figure 1 – Applications Schematic using the SMM665C Controller to actively control the output levels of up to six DC/DC Converters while also providing power on/off, cascade sequencing and output margining.

Note: This is an applications example only. Some pins, components and values are not shown.

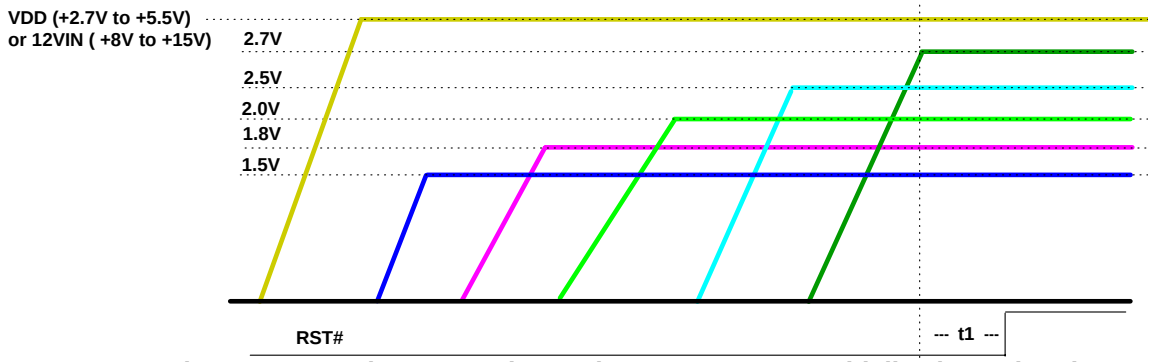


Figure 2 – Example Power Supply Sequencing and System Start-up Initialization using the SMM665C. Any order of supply sequencing can be applied using the SMM665C. Power supply ordering, trimming and Active DC control allows supply cascade sequencing, automatic level adjustment, margin testing and reset control.

GENERAL DESCRIPTION

The SMM665C is a highly integrated and accurate power supply controller, monitor and sequencer. It has the ability to automatically control, monitor and cascade sequence up to six power supplies. Also, the SMM665C can monitor the VDD input, the 12V input, two general-purpose analog inputs and the internal temperature sensor. The SMM665C has four operating modes: Power-on sequencing mode, monitor mode, supply margining mode using Active DC Output Control (ADOC™), and Power-off sequencing mode.

Power-on sequencing can be initiated via the PWR_ON/OFF pin or I^2C control. In this mode, the SMM665C will sequence the power supply channels on in any order by activating the PUP outputs and monitoring the respective converter voltages to ensure cascading of the supplies. Cascade sequencing is the ability to hold off the next sequenced supply until the first supply reaches a programmed threshold. A programmable sequence termination timer can be set to disable all channels if the Power-on sequence stalls. Once all supplies have sequenced on and the voltages are above the UV settings, the Active DC Control, if enabled, will bring the supply voltages to their nominal settings. During this mode, the HEALTHY output will remain inactive and the RST output will remain active.

Once the Power-on sequencing mode is complete, the SMM665C enters monitor mode. In the monitor mode, the SMM665C starts the ADOC control of the supplies and adjusts the output voltage to the programmed setting under all load conditions, especially useful for supplies without sense lines. Typical converters have ±2% accuracy ratings for their output voltage, the Active DC Output Control feature of the SMM665C increases the accuracy to ±0.2% (using a ±0.1% external voltage reference). The part also enables the triggering of outputs by monitored fault conditions. The 10-bit ADC cycles through all 11 channels every 2ms and checks the conversions against the programmed threshold limits. The results can be used to trigger RST, HEALTHY and FAULT outputs as well as to trigger a Power-off or a Force Shutdown operation.

While the SMM665C is in its monitoring mode, an I^2C command to margin the supply voltages can bring the part into margining mode. In margining mode the SMM665C can margin six supply voltages in any combination of nominal, high and low voltage settings using the ADOC feature, all to within ±0.2% using a ±0.1% external reference. The margin high and low voltage settings can range from 0.3V to VDD around the converters' nominal output voltage setting depending on the specified margin range of the DC-DC converter. During this mode the HEALTHY output is always active and the RST output is always inactive regardless of the voltage threshold limit settings and triggers. Furthermore, the triggers for Power-off and Force Shutdown are temporarily disabled.

The Power-off sequencing mode can only be entered while the SMM665C is in the monitoring mode. It can be initiated by either bringing the PWR_ON/OFF pin inactive, through I^2C control or triggered by a channel exceeding its programmed thresholds. Once Power-off is initiated, it will disable the Active DC Control and sequence the PUP outputs off in either the same or reverse order as Power-on sequencing and monitor the supply voltages to ensure cascading of the supplies as they turn off. The sequence termination timer can be programmed to immediately disable all channels if the Power-off sequencing stalls. The RST output will remain active throughout this mode while the HEALTHY output remains inactive.

INTERNAL FUNCTIONAL BLOCK DIAGRAM

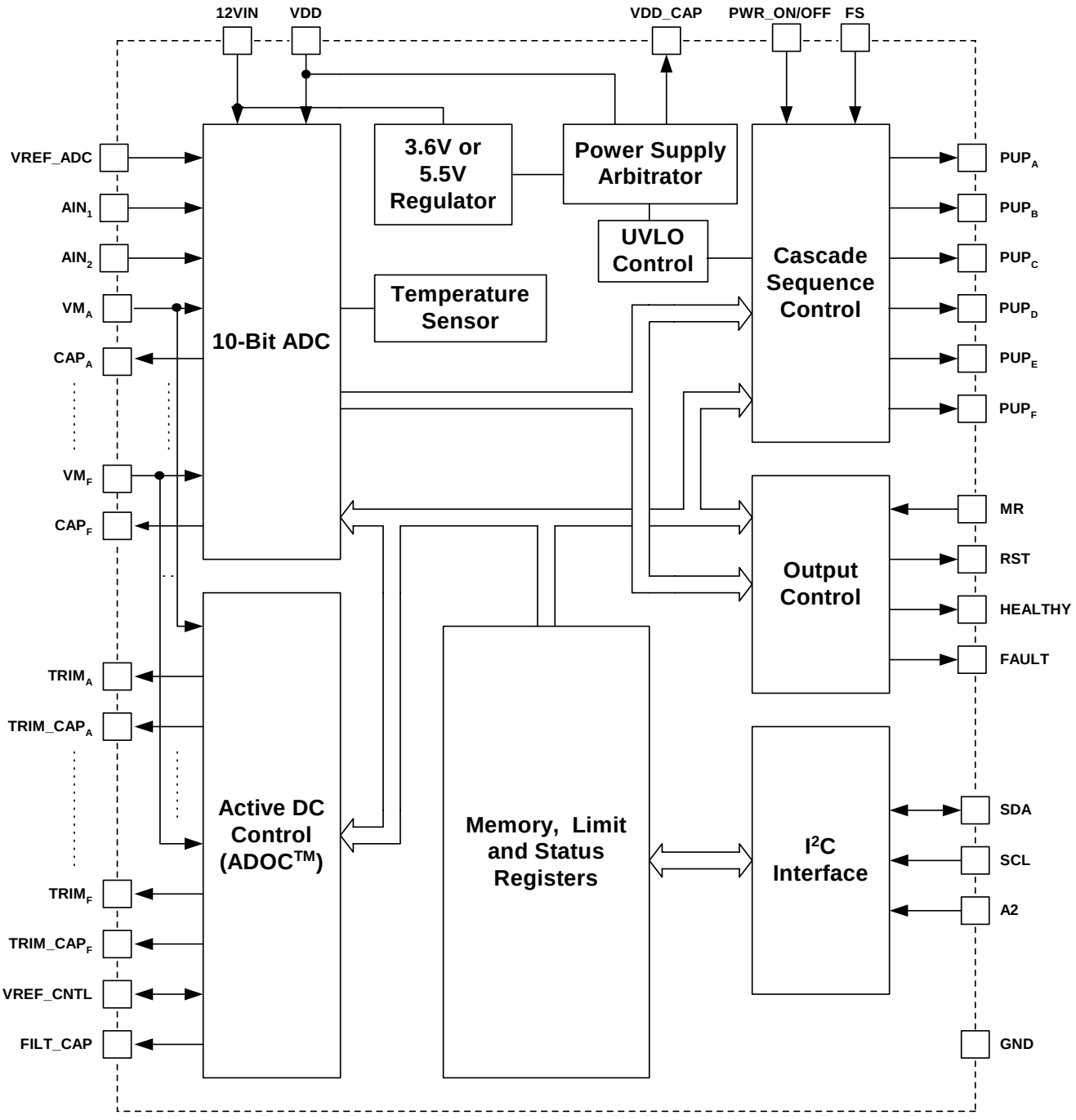


Figure 3 – SMM665C Internal Functional Block Diagram.

PIN DESCRIPTIONS

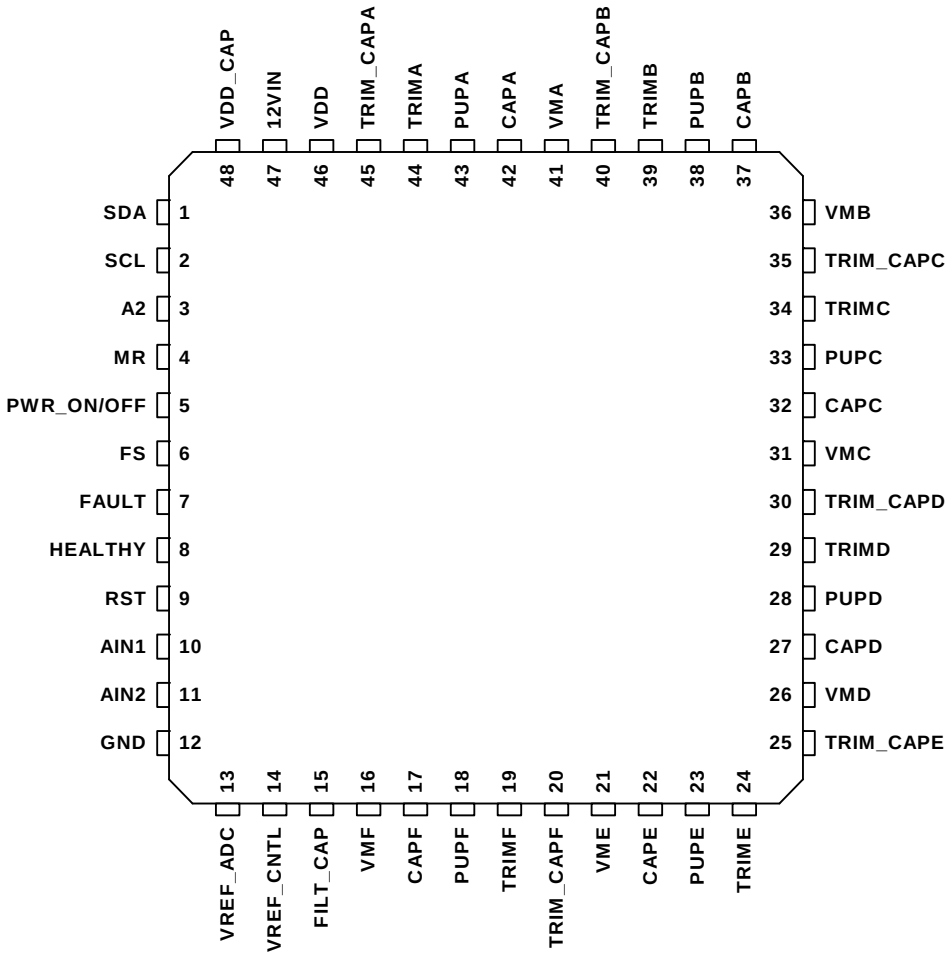
Pin Number	Pin Type	Pin Name	Pin Description
1	DATA	SDA	I^2C Bi-directional data line
2	CLK	SCL	I^2C Clock line
3	IN	A2	The address pin is biased either to VDD_CAP or GND. When communicating with the SMM665C over the 2-wire bus A2 provides a mechanism for assigning a unique bus address.
4	IN	MR	Programmable active high/low input. When asserted the RST output will be go active. When de-asserted the RST output will go inactive immediately after a reset timeout period (t_{PRTO}) if there are no RST trigger sources active. This timeout period makes it suitable to use a pushbutton for manual reset.
5	IN	PWR_ON/OFF	Programmable active high/low input signals the start of the power sequencing. When asserted the part will sequence the supplies on and when de-asserted the part will sequence the supplies off. Note: The SMM665C does not monitor for faults during sequencing. The PWR_ON/OFF pin is overridden by the I^2C power on/off command. To get the pin to work again requires the part be given an I^2C 'Clear' command (see page 14, “RESTART OF POWER-ON CASCADE SEQUENCING”).
6	IN	FS	Programmable active high/low input. Force shutdown is used to immediately turn off all converter enable signals (PUP outputs) when a fault is detected.
7	OUT	FAULT	Programmable active high/low open drain Fault output. Active when a programmed fault condition exists on AIN1, AIN2, or the internal temperature sensor.
8	OUT	HEALTHY	Programmable active high/low open drain Healthy output. Active when all programmed power supply inputs and monitored inputs are within OV and UV limits.
9	OUT	RST	Programmable active high/low open drain Reset output. Active when a programmed fault condition exists on any power supply inputs or monitored inputs or when MR is active. RST has a programmable timeout period with options for 0.64ms, 25ms, 100ms and 200ms.
10	IN	AIN1	General purpose monitored analog input
11	IN	AIN2	General purpose monitored analog input
12	GND	GND	Ground
13	IN	VREF_ADC	Voltage reference input used for A/D conversion where: (4XVREF_ADC) = Full Scale (FS) for VM_{A-F} and VDD (12XVREF_ADC) = FS for 12VIN (2XVREF_ADC) = FS for AIN1 and AIN2. VREF_ADC can be connected to VREF_CNTL in most applications.

PIN DESCRIPTIONS (Cont.)

Pin Number	Pin Type	Pin Name	Pin Description
14	I/O	VREF_CNTL	Voltage reference input used for DC output control and margining. VREF_CNTL can be programmed to output the internal 1.25V reference.
15	CAP	FILT_CAP	External capacitor input used to filter VM_X inputs
41,36, 31, 26, 21,16	IN	VM_X	Positive converter sense line, VM_A through VM_F
42, 37, 32, 27, 22, 17	CAP	CAP_X	External capacitor input used to filter the VM_X inputs to the 10-bit ADC, CAP_A through CAP_F. This provides an RC filter where R = 25kΩ.
43, 38, 33, 28, 23, 18	OUT	PUP_X	Programmable active high/low open drain converter enable output, PUP_A through PUP_F
44, 39, 34, 29, 24, 19	OUT	$TRIM_X$	Output voltage used to control the output of DC/DC converters, $TRIM_A$ through $TRIM_F$. If the ADOC/margining functionality is not used on a channel the associated $TRIM_X$ pin should be left floating
45, 40, 35, 30, 25, 20	CAP	$TRIM_CAP_X$	External sample and hold capacitor input used to set the voltage on the TRIM pins, $TRIM_CAP_A$ through $TRIM_CAP_F$
46	PWR	VDD	Power supply of the part
47	PWR	12VIN	12V power supply input internally regulated to either 3.6V or 5.5V
48	CAP	VDD_CAP	External capacitor input used to filter the internal supply

PACKAGE AND PIN CONFIGURATION

48-LEAD TQFP



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias..... -55°C to 125°C
Storage Temperature..... -65°C to 150°C
Terminal Voltage with Respect to GND:
VDD Supply Voltage ..... -0.3V to 6.0V
12VIN Supply Voltage..... -0.3V to 15.0V
PUP_A, through PUP_F..... -0.3V to 15.0V
All Others .....-0.3V to V_{DD} + 0.7V
Output Short Circuit Current 100mA
Lead Solder Temperature (10 secs) ..... 300°C
Junction Temperature.....150°C
ESD Rating per JEDEC[B]……..2000V
Latch-Up testing per JEDEC……±100mA

Note A - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

RECOMMENDED OPERATING CONDITIONS

Temperature Range (Industrial).....–40°C to +85°C
(Commercial) .....–5°C to +70°C
VDD Supply Voltage .....2.7V to 5.5V
12VIN Supply Voltage[C] .....8.0V to 14.0V
VIN ..... GND to VDD
VOUT ..... GND to 14.0V
Package Thermal Resistance (θ_{JA})
48-Lead TQFP……80°C/W

Moisture Classification Level 1 (MSL 1) per J-STD- 020. MSL 3 for 100% Sn, RoHS compliant, see Ordering Information.

Note B – Pin # 46 and pin #48 meet 1kV.
Note C – Range depends on internal regulator set to 3.6V or 5.5V, see 12VIN specification below.

RELIABILITY CHARACTERISTICS

Data Retention……..100 Years
Endurance…….100,000 Cycles

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min	Typ	Max	Unit
VDD	Supply Voltage		2.7		5.5	V
12VIN	Supply Voltage	Internally regulated to 5.5V	10		14	V
		Internally regulated to 3.6V	6		14	V
I_{DD}	Power Supply Current from VDD	All TRIM pins floating, 12VIN floating		1.4	5	mA
I_{12VIN}	Power Supply Current from 12VIN	All TRIM pins floating, VDD floating, Note 10		3.6	5	mA
TRIM characteristics						
I_{TRIM}	TRIM output current through 100Ω to 1.0V, Note 10	TRIM Sourcing Maximum Current	1.5			mA
		TRIM Sinking Maximum Current	1.5			mA
V_{TRIM}	Margin Control and ADOC Range	Depends on Trim range of DC-DC Converter	VREF_CNT L/4		VDD	V
TRIM_CAP characteristics						
I_{TRIM_CAP}	TRIM output current through 1uF capacitor to ground, Note 2	Max acceptable board and cap leakage is 50nA		100		nA
All other input and output characteristics						
V_{VDD_CAP}	VDD_CAP voltage	Internally regulated to 3.6V	3.4	3.6	3.8	V
		Internally regulated to 5.5V	5.3	5.5	5.7	V
		No voltage on 12VIN, Note 10	VDD - 0.1	VDD	VDD + 0.1	V

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min	Typ	Max	Unit
V_{IH}	Input High Voltage (FS, PWR_ON/OFF, MR#, SDA, SCL), Note 3	VDD = 2.7V	0.7 x VDD_CAP			V
		VDD = 5.0V	0.7 x VDD_CAP			V
V_{IL}	Input Low Voltage (FS, PWR_ON/OFF, MR#, SDA, SCL), Note 3	VDD = 2.7V			0.3 x VDD_CAP	V
		VDD = 5.0V			0.3 x VDD_CAP	V
V_{IH}	Input High Voltage (FS, PWR_ON, MR#, SDA, SCL), Notes 3, 10	Internally regulated to 3.6V	0.7 x VDD_CAP			V
		Internally regulated to 5.5V	0.7 x VDD_CAP			V
V_{IL}	Input Low Voltage (FS, PWR_ON, MR#, SDA, SCL), Notes 3, 10	Internally regulated to 3.6V			0.3 x VDD_CAP	V
		Internally regulated to 5.5V			0.3 x VDD_CAP	V
I_{OL}	Output Low Current, Note 6		0		1.0	mA
I_{OLSDA}	Output low current for SDA	VOL=0.4V	3			mA
I_S	Leakage current on SDA and SCL	When SDA or SCL are at 3.6V			1.0	µA
V_{SENSE}	Positive Sense Voltage	VM pin	+0.3		VDD_CAP	V
$V_{Monitor}$	Monitor Threshold Step Size	VM, AIN1/AIN2 pins		5		mV
T_{SA}	Internal Temperature Sensor Accuracy (Notes 5, 8)	Commercial Temp Range	-4	±4	+4	°C
		Industrial Temp Range	-6	±6	+6	°C
$T_{Monitor}$	Temperature Threshold Step Size	Internal Temp Sensor		0.25		°C
V_{REF}	Internal 1.25V_{REF} Output Voltage Accuracy	T = +25°C	-0.4		+0.4	%
		T = -40°C to +85°C	-0.8		+0.8	%
Ext V_{REF}	External V_{REF} Voltage Range		0.5		VDD_CAP	V
$ADOC_{ACC}$	ADOC/Margin Accuracy	External V_{REF}=1.25V, ±0.1%, Total PUPx I_{SINK} = 6ma, $V_{SENSE} \leq$ 3.5V, T = 0°C to +50°C	-0.20	±0.1	+0.20	%
		External V_{REF}=1.25V, ±0.1%, Total PUPx I_{SINK} = 6ma, $V_{SENSE} \leq$ 3.5V, T = 0°C to +70°C	-0.35	±0.1	+0.35	%
		External V_{REF}=1.25V, ±0.1%, Total PUPx I_{SINK} = 6ma, $V_{SENSE} \geq$ 3.5V, T = 0°C to +50°C	-0.50	±0.3	+0.50	%
		Internal V_{REF}=1.25V, Total PUPx I_{SINK} = 6ma, T = 0°C to +50°C	-0.50	±0.3	+0.50	%

DC OPERATING CHARACTERISTICS (CONTINUED)						
Symbol	**Parameter**	**Notes**	**Min**	**Typ**	**Max**	**Unit**
V_{OUT_VALID}	Minimum Output Valid Voltage	VDD_CAP voltage at which the PUP, RST, HEALTHY and FAULT outputs are valid		1		V
UVLO	UVLO (Under Voltage Lockout) threshold (Note 4)	VDD_CAP rising		2.6		V
		VDD_CAP falling		2.5		V
I_{VDD_CAP}	Maximum load on VDD_CAP, Note 10				10	mA
AIN1/AIN2 ADC characteristics						
N	Resolution		10			Bits
MC	Missing codes	Minimum resolution for which no missing codes are guaranteed	10			Bits
S/N	Signal-to-noise Ratio	Conversion rate = 500Hz		72		dB
DNL	Differential non-linearity		-1/2		+1/2	LSB
INL	Integral non-linearity	Note 7	-1		+1	LSB
GAIN	Positive full scale gain error	Note 7	-0.5	±0.16	+0.5	%
OFFSET	Offset error	Note 7	-1		+1	LSB
ADC_TC	Full scale temperature coefficient			±15		ppm/°C
IM_{ADC}	Analog ADC Input Impedance			10		MΩ
II_{VREF}	V_{REF} input current			250		nA
IC_{VREF}	V_{REF} input capacitance			200		pF
IR_{VREF}	V_{REF} input impedance			1		kΩ
VMA-VMF, VDD ADC characteristics						
N	Resolution		10			Bits
MC	Missing codes	Minimum resolution for which no missing codes are guaranteed	10			Bits
S/N	Signal-to-noise Ratio	Conversion rate = 500Hz		72		dB
ERR_ADC	Total ADC Error	Total ADC Read Error	-4		+4	LSB
IM_{ADC}	Analog ADC Input Impedance	VMA-VMF		100		KΩ
12VIN ADC characteristics						
N	Resolution		10			Bits
MC	Missing codes	Minimum resolution for which no missing codes are guaranteed	10			Bits
S/N	Signal-to-noise Ratio	Conversion rate = 500Hz		72		dB
ERR_ADC	Total ADC Error	Total ADC Read Error	-4		+4	LSB

Note 1 – Range depends on internal regulator set to 3.6V or 5.5V see 12VIN specification.
Note 2 – See Application Note 37 which describes the type of capacitors to use to obtain minimum leakage.
Note 3 – All logic levels are with respect to the voltage on VDD_CAP, when supplied from VDD; VDD_CAP is equal to VDD, under no load.
Note 4 – (100mV typical Hysteresis)
Note 5 – Under certain operating conditions, self-heating could result in additional temperature sensor error.
Note 6 – SDA not included (separate electrical specification). The device can sink more than 20mA, however total I_{SINK} from all PUPx pins should not exceed 6mA or $ADOC_{ACC}$ specification will be affected.
Note 7 – The formula for the total ADC inaccuracy is: [((ADC read voltage) +/- INL)*(range of gain error)]+range of offset error
Note 8 – When temperature sensor is not used (determined by the hex file configuration setting) sensor accuracy is tested for typical values only.
Note 9 – The term "FAULT#" throughout this document describes a pin and output signal, whereas the term "fault" describes an operating condition that may or may not activate the FAULT# pin. The FAULT# pin can only be activated by Ain1, Ain2 and Temperature fault conditions.
Note 10 – Guaranteed by Design and/or Characterization – not 100% tested in production.

AC OPERATING CHARACTERISTICS

Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND. See Figure 5 and 6 Timing diagrams.

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_{DPON}	Programmable Power-on delay from VM_X out-of-fault to PUP_Y active	t_{DPON} = 0.64ms	-15	t_{DPON}	+15	%
		t_{DPON} = 12.5ms				
		t_{DPON} = 25ms				
		t_{DPON} = 50ms				
t_{DPOFF}	Programmable Power-off delay from VM_X off to PUP_Y inactive	t_{DPOFF} = 0.64ms	-15	t_{DPOFF}	+15	%
		t_{DPOFF} = 12.5ms				
		t_{DPOFF} = 25ms				
		t_{DPOFF} = 50ms				
t_{PRTO}	Programmable Reset Time-Out Period	t_{PRTO} = 0.64ms	-15	t_{PRTO}	+15	%
		t_{PRTO} = 25ms				
		t_{PRTO} = 100ms				
		t_{PRTO} = 200ms				
t_{STT}	Programmable Sequence Termination Timer	t_{STT} = OFF	-15	t_{STT}	+15	%
		t_{STT} = 100ms				
		t_{STT} = 200ms				
		t_{STT} = 400ms				
t_{ADC}	10-bit ADC sampling period	Time for ADC conversion of all 11 channels		2		ms
$t_{DC_CONTROL}$	Active DC Control sampling period	Update period for Active DC Control of channels A – F		1.7		ms
t_{conv}	Single ADC channel conversion time	Update period for Active DC Control per channel		182		µs
T_{MARGIN}	Margin Time from Nominal	Slow Margin, ± 10% change in voltage with 0.1% ripple TRIM_CAP=1µF		850		ms
		Fast Margin, ± 10% change in voltage with 0.1% ripple TRIM_CAP=1µF		85		ms
$t_{A\text{-}M_SUSPEND}$	Auto-Monitor Suspend Period	Auto-Monitor suspended indefinitely by a faulty I^2C transaction		25	100	ms

I²C 2-WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS – 100/400kHz

T =-40C to +85C, VDD = +2.8V to +5.5V, unless otherwise noted. All voltages are relative to GND.
See Figure 4 Timing Diagram.

Symbol	Description	Conditions	100kHz			400kHz			
			Min	Typ	Max	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency		0		100	0		400	KHz
t_{LOW}	Clock Low Period		4.7			1.3			µs
t_{HIGH}	Clock High Period		4.0			0.6			µs
t_{BUF}	Bus Free Time	Before New Transmission – Note 11	4.7			1.3			µs
$t_{SU:STA}$	Start Condition Setup Time		4.7			0.6			µs
$t_{HD:STA}$	Start Condition Hold Time		4.0			0.6			µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7			0.6			µs
t_{AA}	Clock Edge to Data Valid	SCL low to valid SDA (cycle n)	0.2		3.5	0.2		0.9	µs
t_{DH}	Data Output Hold Time	SCL low (cycle n+1) to SDA change	0.2			0.2			µs
t_R	SCL and SDA Rise Time	Note 11			1000			1000	ns
t_F	SCL and SDA Fall Time	Note 11			300			300	ns
$t_{SU:DAT}$	Data In Setup Time		250			150			ns
$t_{HD:DAT}$	Data In Hold Time		0			0			ns
TI	Noise Filter SCL and SDA	Noise suppression, Note 11		100			100		ns
t_{WR_CONFIG}	Write Cycle Time Config	Configuration Registers			10			10	ms
t_{WR_EE}	Write Cycle Time EE	Memory Array			5			5	ms

Note 11 – Guaranteed by Design.

TIMING DIAGRAMS

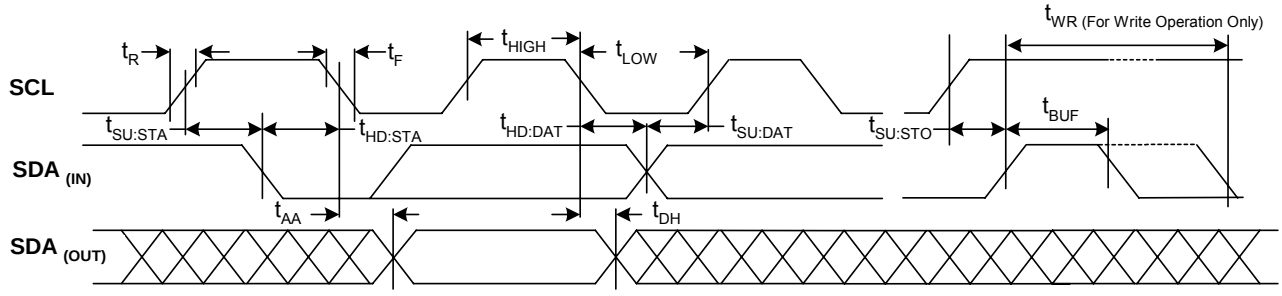


Figure 4 - Basic I²C Serial Interface Timing

TIMING DIAGRAMS (CONTINUED)

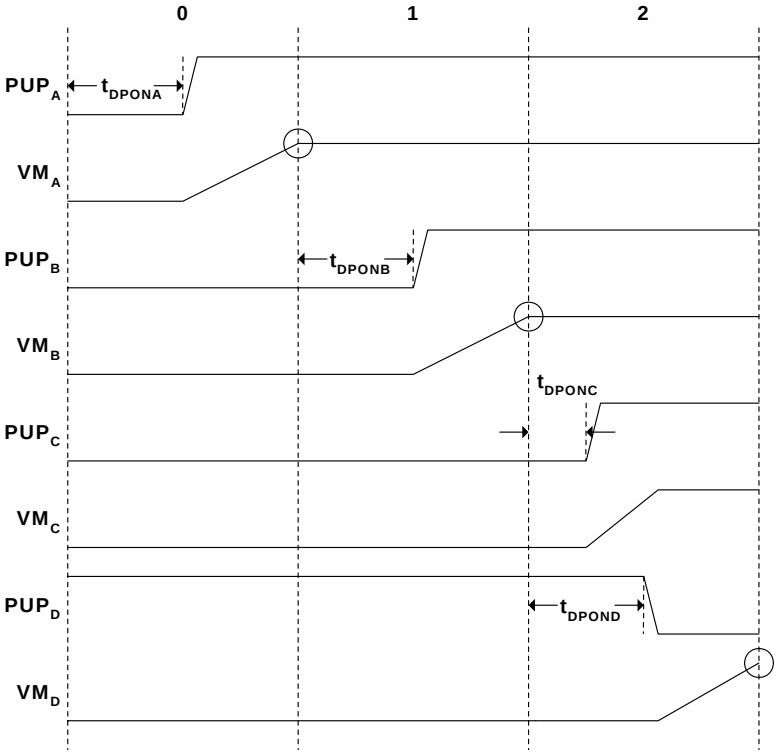


Figure 5 - The SMM665C cascade sequencing the supplies on and then monitoring for fault conditions.

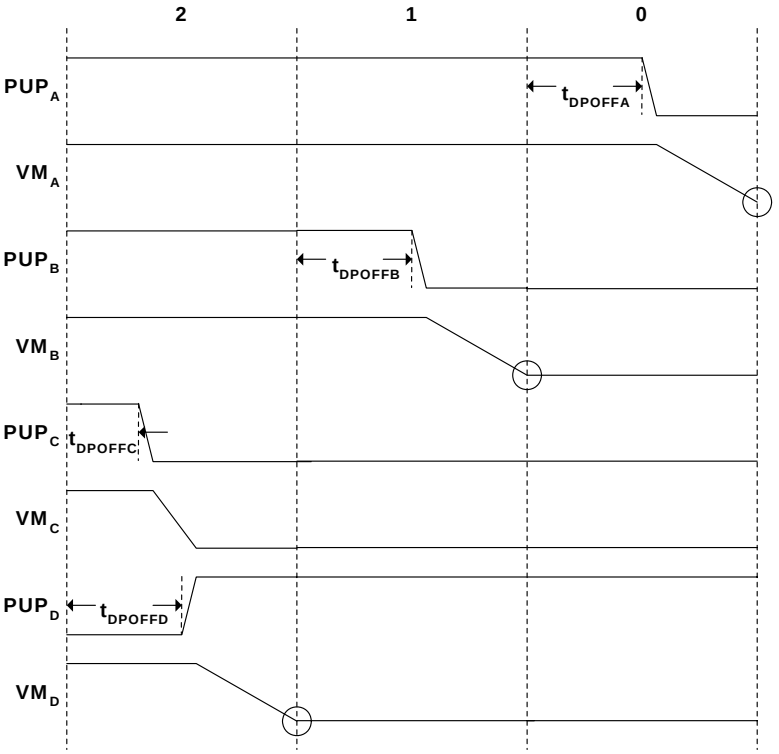


Figure 6 - The SMM665C cascade sequencing the supplies off.

APPLICATIONS INFORMATION

DEVICE OPERATION

POWER SUPPLY

The SMM665C can be powered by either a 12V input through the 12VIN pin or by a 3.3V or 5.0V input through the VDD pin. The 12VIN pin feeds an internal programmable regulator that internally generates either 5.5V or 3.6V. A voltage arbitration circuit allows the device to be powered by the highest voltage from either the regulator output or the VDD input. This voltage arbitration circuit continuously checks for these voltages to determine which will power the SMM665C. The resultant internal power supply rail is connected to the VDD_CAP pin that allows both filtering and hold-up of the internal power supply. To ensure that the input voltage is high enough for reliable operation, an under voltage lockout circuit holds the controlled supplies off until the UVLO thresholds are met.

MODES OF OPERATION

The SMM665C has four basic modes of operation (shown in Figures 5 through 8): Power-on cascade sequencing mode, ongoing operations-monitoring mode, supply margining mode and Power-off cascade sequencing mode. In addition, there are two features: ADOC and forced shutdown which can be used during monitoring and margining mode. A detailed description of each mode and feature follows.

ACTIVE DC OUTPUT CONTROL (ADOC™)

The SMM665C can actively control the DC output voltage of bricks or DC/DC converters that have a trim pin during monitoring and margining mode. The converter may be an off-the shelf compact device, or may be a "roll your own" circuit on the application board. In either case, the SMM665C dramatically improves voltage accuracy (down to 0.2%) by implementing closed-loop ADOC active control. This utilizes the DC-DC's "trim" pin as shown in Figure 12, or an equivalent output voltage feedback adjustment "VADJ" or "FB" node in a user's custom circuit, Figure 13. Each of the $TRIM_X$ pins on the SMM665C is connected to the trim input pins on the power supply converters. A sense line from the channel's point-of-load connects to the corresponding VM input. The ADOC function cycles through all six channels (A-F) every 1.7ms making slight adjustments to the voltage on the associated $TRIM_X$ output pins based on the voltage inputs on the VM_X pins. These voltage adjustments allow the SMM665C to control the output voltage of power supply converters to within ±0.2% when using a ±0.1% external voltage reference.

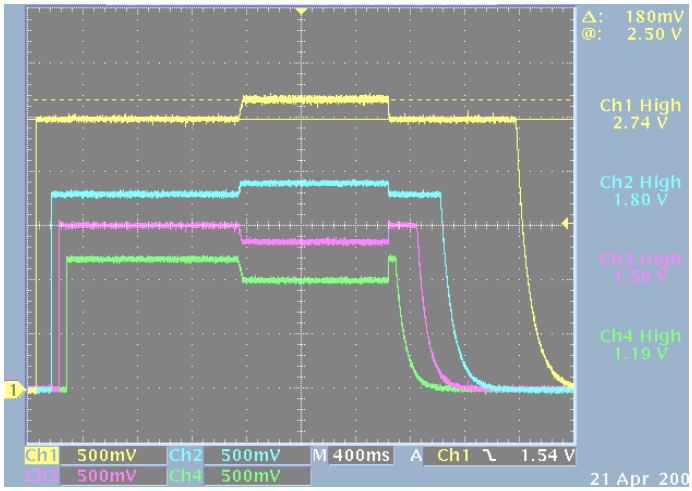


Figure 7 - Waveform shows four SMM665C channels exhibiting Sequence-on to Nominal voltage, Margin High or Low, Nominal voltage and then sequence-off

Ch 1 = 2.5V DC-DC converter output (Yellow trace)
Ch 2 = 1.8V DC-DC converter output (Blue trace)
Ch 3 = 1.5V DC-DC converter output (Purple trace)
Ch 4 = 1.2V DC-DC converter output (Green trace

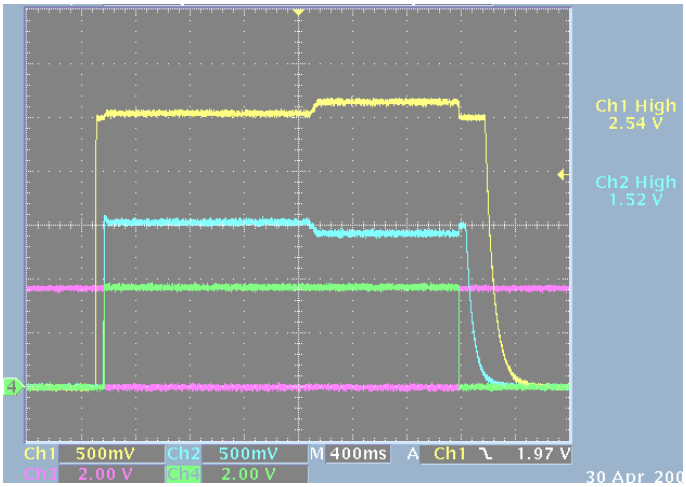


Figure 8 - Waveform shows two SMM665C channels Sequencing-on to Nominal voltage, Margin High and Low, and then sequence-off. Channel 3 and 4 shows the RST and HEALTHY signals.

Ch 1 = 2.5V DC-DC converter output (Yellow trace)
Ch 2 = 1.5V DC-DC converter output (Blue trace)
Ch 3 = RST signal output (Purple trace)
Ch 4 = HEALTHY signal output (Green trace)

APPLICATIONS INFORMATION (CONTINUED)

A pulse of current, either sourced or sunk for 5µs every 1.7ms, to the capacitors connected to the TRIM_CAP$_X$ pins adjusts the voltage output on the TRIM$_X$ pins. The voltages on the TRIM_CAP$_X$ pins are buffered and applied to the TRIM$_X$ pins. The voltage adjustments on the TRIM$_X$ pins cause a slight ripple of less than 1mV on the power supply voltages. The amplitude of this ripple is a function of the TRIM_CAP capacitor and the trim gain of the converter. Application Note 37 details the calculation of the TRIM_CAP capacitor to achieve a desired minimum ripple.

Each channel can be programmed to either enable or disable the Active DC Control function. When disabled or not active, the TRIM$_X$ pins on the SMM665C are high impedance inputs. If disabled and not used, they can be connected to ground. The voltages on the TRIM$_X$ pins are buffered and applied to the TRIM_CAP$_X$ pins charging the capacitors. This allows a smooth transition from the converter powering up to its nominal voltage; to the SMM665C controlling that voltage, and to the Active DC Control nominal setting.

The pulse of current can be increased to a 10X pulse of current until the power supply voltages are at their nominal settings by selecting the programmable Speed-Up Convergence option. As the name implies, this option decreases the time required to bring a supply voltage from the converter's nominal output voltage to the Active DC Control nominal voltage setting.

POWER-ON CASCADE SEQUENCING

The SMM665C can be programmed to sequence up to six power supplies in any order. Each of these six channels (A-F) has an associated open drain PUP output that, when connected to a converter's enable pin, controls the turn-on of the converter. The channels are assigned sequence positions to determine the order of the sequence. Any channel can also be programmed to not take part in the sequencing in applications with fewer than six supplies. The polarity of each of the PUP$_X$ outputs is programmable for use with various types of converters.

Power-on sequencing can be initiated by the PWR_ON/OFF pin or via I^2C control. The polarity of the PWR_ON/OFF pin is programmable. If hard wired in its active state the SMM665C will automatically initiate the Power-on sequence. Otherwise, toggling the PWR_ON/OFF pin to its active state will initiate the Power-on sequence. To enable software control of the sequencing feature, the SMM665C offers an I^2C command to initiate Power-on sequencing while the PWR_ON/OFF pin is in its inactive state.

The SMM665C can be programmed to wait until either or both VDD and 12VIN inputs are within their respective voltage threshold limits before Power-on sequencing is allowed to begin. This ensures that the converters have their full supply voltage before they are enabled.

Once Power-on sequencing begins, the SMM665C will wait a Power-on delay time (t_{DPON}) for any channel in the first sequence position (0) and then activate the PUP$_X$ outputs for those channels. The Power-on delay times are individually programmable for each channel. The SMM665C will then wait until all VM$_X$ inputs of the channels assigned to the first sequence position (0) are above their programmed UV1 thresholds which is called cascade sequencing. At this point, the SMM665C will enter the second sequence position (1) and begin to timeout the Power-on delay times for the associated channels. This process continues until all of channels in the sequence have turned on and are above their UV1 threshold. The status registers indicates that all sequenced power supply channels have turned on. Once these channels are above their UV1 thresholds, the SMM665C will begin the Active DC Control of the enabled channels. The Power-on sequencing mode ends when the Active DC Controlled channels are at their nominal voltage setting. The "Ready" bit in the status registers signifies that the voltages are at their set points.

The programmable sequence termination timer can be used to protect against a stalled Power-on sequence. This timer resets itself at the beginning of each sequence position. All channels in the sequence position must go above their UV1 threshold before the sequence termination timer times out (t_{STT}) or the sequence will terminate and all PUP$_X$ outputs will be switched to their inactive state. The status registers contain bits that indicate the sequence has been terminated and in which sequence position the timer timed out. This timer has four settings of OFF, 100ms, 200ms and 400ms.

APPLICATIONS INFORMATION (CONTINUED)

While the SMM665C is in the Power-on sequencing mode the RST output is held active and the HEALTHY output is held inactive regardless of trigger sources (Figure 8). The Power-off and Force Shutdown trigger options are also disabled while in this mode. Furthermore, the SMM665C will not respond to activity on the PWR_ON/OFF pin or to a Power-off I^2C command during Power-on sequencing mode.

ONGOING OPERATIONS-MONITORING MODE

During ongoing operations mode, the part can (1) monitor (2) actively control via ADOC, and (3) use force shutdown if necessary.

Once the Power-on sequence is complete and before a Power-off sequence has been initiated, the SMM665C continues to monitor all VM_X inputs, the VDD and 12VIN inputs, and two temperature sensor inputs with a 10-bit ADC. Each of these inputs is sampled and converted by the ADC every 2ms. The ADC input has a range of 0V to four times the voltage on VREF_ADC for inputs VM_{A-F} and the VDD input. The range is extended to 12 times VREF_ADC for the 12VIN input and is reduced to two times VREF_ADC for the AIN1 and AIN2 inputs.

The SMM665C monitors internal temperature using the 10-bit ADC and the auto-monitor function. Two under temperature and two over temperature thresholds can be set, each with its own programmable trigger options and consecutive conversion before trigger counter. Resolution is 0.25 C per bit scaled over the range of -128 C to 127.75 C. The temperature value can be acquired over the I^2C bus as a 10-bit signed two's complement value.

The SMM665C compares each resulting ADC conversion with two programmable 10-bit under-voltage limits (UV1, UV2) and two programmable 10-bit over-voltage limits (OV1, OV2) for the corresponding input. A consecutive conversion counter is used to provide filtering of the ADC inputs. Each limit can be programmed to require 1, 2, 4 or 6 consecutive out-of-limit conversions before it is said to be in fault. One in-limit conversion will remove the fault from the threshold limit. This provides digital filtering of the monitored inputs. The ADC inputs VM_{A-F} can use additional filtering by connecting a capacitor from the corresponding CAP_X pins to ground to form an analog RC filter (R=25kΩ). The input is considered to be in a fault condition if any of its limit thresholds are in fault. Setting an OV threshold limit to full-scale ($3FF_{HEX}$), or setting an UV threshold limit to 000_{HEX} ensures that the limit can never be in fault.

The status registers provide the real-time status of all monitored inputs.

The voltage threshold limits for inputs VM_{A-F}, VDD and 12VIN can be programmed to trigger the RST and HEALTHY outputs as well as a Force Shutdown and Power-off operation when exceeded. The threshold limits for the internal temperature sensor and the AIN1 and AIN2 inputs can be programmed to trigger the RST, HEALTHY, and FAULT outputs.

The HEALTHY and FAULT outputs of the SMM665C are active as long as the triggering limit remains in a fault condition. The RST output also remains active as long as the triggering limit remains in a fault condition; however, once the trigger source goes away the RST will remain active for a reset timeout period (t_{PRTO}).

AUTO-MONITOR MODE

The auto-monitor mode, responsible for monitoring all voltage thresholds and triggering the programmable options, is paused during an I^2C transaction. This is done to allow the I^2C interface to access the internal data bus that is used in the auto-monitor function Specifically, the auto-monitor is paused approximately 100ns after the falling edge of SCL during transmission of the R/W bit of a valid slave address. For normal I^2C transactions, the auto-monitor function is resumed following an I^2C STOP issued at the end of the transaction or upon the NACK of an invalid slave address. For I2C ADC conversion transactions, which employ acknowledge polling, the auto-monitor function is resumed after the conversion has completed (approximately 300us after the second ACK of the transaction) and following a I^2C STOP issued at the end of the transaction or upon the NACK of an invalid slave address.

During every suspension of the auto-monitor, a 25ms timer is activated. The clock stage will determine the exact timeout period, typically between 25msec and 50msec. Should the I^2C transaction fail, this timer will expire and restart the auto-monitor.

See “Auto-Monitor Function” section for timing details and conditions under which the auto-monitor timer will be asserted.

APPLICATIONS INFORMATION (CONTINUED)

TEMPERATURE SENSOR ACCURACY

The internal temperature sensor accuracy is ±5°C from -40 to +90°C. The sensor measures the temperature of the SMM665C die and the ambient temperature. If VDD is at 5V, the die temperature is +2°C and at 12V, it is +4°C. In order to calculate this difference in specific applications measure the Vdd or 12VIN supply current and calculate the power dissipated and multiply by 80°C/W. For instance, 5V and 5mA is 25mW, which creates a 2°C offset.

Note: For hex files (configuration settings) that indicate no use of the temperature sensor, only the typical temperature sensor accuracy is valid.

MARGINING

The SMM665C has two additional Active DC Output Control voltage settings for channels A-F; margin high and margin low. The margin high and margin low voltage settings can range from 0.3V to VDD of the converters' nominal output voltage depending on the specified margin range of the DC-DC converter. These settings are stored in the configuration registers and are loaded into the Active DC Control voltage setting by margin commands issued via the I^2C bus. The channel must be enabled for Active DC Control in order to enable margining. The margin command registers contain two bits for each channel that decode the commands to margin high, margin low, or control to the nominal setting. Therefore, any combination of margin high, margin low, and nominal control is allowed in the margining mode.

Once the SMM665C receives the command to margin the supply voltages, it begins adjusting the supply voltages to move toward the desired setting. When all channels are at their voltage setting, a bit is set in the margin status registers.

Note: Configuration writes or reads of registers 00_{HEX} to $0F_{HEX}$ should not be performed while the SMM665C is margining.

POWER-OFF CASCADE SEQUENCING

The SMM665C can be programmed to perform Power-off sequencing in either the same order or reverse order of Power-on cascade sequencing.

Power-off cascade sequencing can be initiated by the PWR_ON/OFF pin, via I^2C control or triggered by a fault condition on any of the monitored inputs. Toggling the PWR_ON/OFF pin to its inactive state will initiate the Power-off sequence.

To enable software control of the Power-off sequencing feature, the SMM665C offers an I^2C command to initiate Power-off sequencing regardless of the state of the PWR_ON/OFF pin. Furthermore, Power-off sequencing can be initiated by a fault condition on a monitored input.

Once Power-off sequencing begins, the SMM665C will wait a Power-off delay time (t_{DPOFF}) for any channel in the last sequence position (reverse order) and then deactivate the PUP outputs for those channels. The Power-off delay times are individually programmable for each channel. The SMM665C will then wait until all VM_X inputs of the channels assigned to that sequence position are below the programmed OFF thresholds.

At this point, the SMM665C will decrement to the next sequence position and begin to timeout the Power-off delay times for the associated channels. This process continues until all of channels in the sequence have turned off and are below their OFF thresholds. The status register reveals that all sequenced channels have turned off. The Power-off sequencing mode ends when all sequenced supplies are below their OFF thresholds.

The programmable sequence termination timer can be used to protect against a stalled Power-off sequence. This timer resets itself at the beginning of each sequence position. All channels in the sequence position must go below their OFF threshold before the sequence termination timer times out (t_{STT}) or the sequence will terminate and all PUP outputs will be switched to their inactive state. This timer has four settings of OFF, 100ms, 200ms and 400ms. The sequence termination timer can be disabled separately for Power-off sequencing.

While the SMM665C is in the Power-off sequencing mode the RST output is held active and the HEALTHY output is held inactive regardless of trigger sources (Figure 8). The Force Shutdown trigger option is also disabled while in this mode. Furthermore, the SMM665C will not respond to activity on the PWR_ON/OFF pin or to a Power-on I^2C command during Power-off sequencing mode.

APPLICATIONS INFORMATION (CONTINUED)

FORCE SHUTDOWN

The Force Shutdown operation brings all PUP_X outputs to their inactive state. This operation is used for an emergency shutdown when there is not enough time to sequence the supplies off. The Force Shutdown operation shuts off all sequenced channels and waits for the supply voltages to drop below their respective OFF thresholds.

A Force Shutdown operation can be initiated by any one of four events. The first two methods for initiating a Force Shutdown are always enabled. Simply taking the FS pin to its active state will initiate a Force Shutdown operation and maintain it until the pin is brought to its inactive state. An I^2C Force Shutdown command allows the Force Shutdown operation to be initiated via software control. This I^2C Force Shutdown command sets a volatile register bit that triggers a Force Shutdown. This bit is cleared after all sequenced channels have dropped below their OFF voltage threshold. During Power-on and Power-off sequencing, the sequence termination timer can initiate a Force Shutdown operation.

As described in the previous sections, the sequence termination timer triggers a Force Shutdown operation if it times out before the power supply voltages surpass their voltage thresholds. This Force Shutdown will remain active until all sequenced power supply channels have dropped below their OFF voltage threshold. While the SMM665C is in ongoing operations-monitor mode, a programmed fault condition on any power supply channel or on the 12VIN or VDD inputs can trigger a Force Shutdown. A Force Shutdown resulting from this will remain active until all sequenced power supply channels have dropped below their OFF voltage threshold.

For restarting the device, the FS command needs to be cleared by writing that bit to a zero. This will clear the command and, if the POWER-ON/OFF pin is not being forced low externally the SMM665C will begin a power-on sequence

APPLICATIONS INFORMATION (CONTINUED)

SMM665C BROWNOUT RECOVERY/HANDLING

During a power 'brown-out' (Figure 9) the SMM665C can default to a power-off state, thus requiring toggling of the PWR_ON/OFF pin to enable the device to perform a power-on sequence. For applications using I^2C control of the power-on/power-off function, the same result may be effected by, upon recovery of power, issuing a software (I^2C) 'Power-Off' command followed by a 'Power-On' command and ending with a 'Clear' command. If the PWR_ON/OFF pin is in the asserted state, the SMM665C will initiate a power-on sequence once all input conditions are met. Otherwise the PWR_ON/OFF pin may require toggling if, upon recovery from the 'brownout', it is in the de-asserted state.

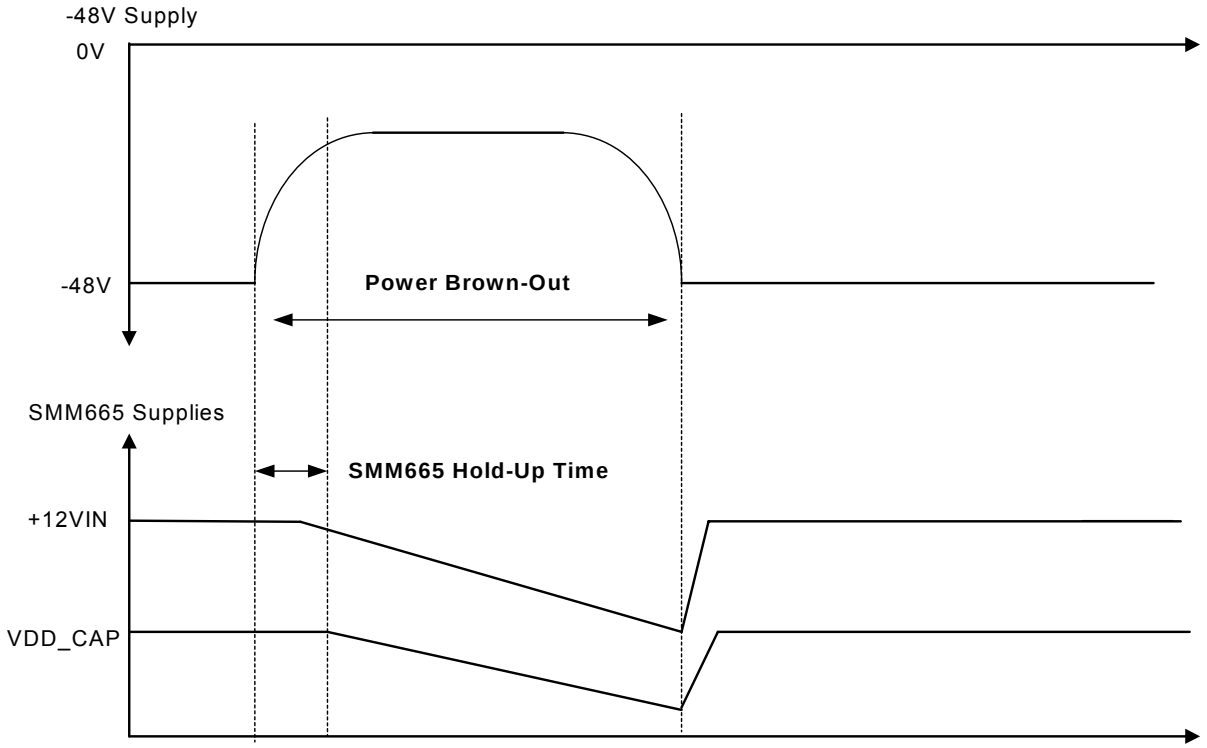


Figure 9 - Power Brown-Out with Resulting Loss of SMM665C Supply Voltages

APPLICATIONS INFORMATION (CONTINUED)

AUTO-MONITOR FUNCTION

The auto-monitor function is used for monitoring all supplies throughout the power-on and power-off sequencing, force shutdown operation, and monitor mode. The auto-monitor function is paused during an I^2C transaction. This function is re-enabled by several methods as described in the diagrams below.

Pausing Auto-Monitor: I^2C Transaction Addressing the SMM665C

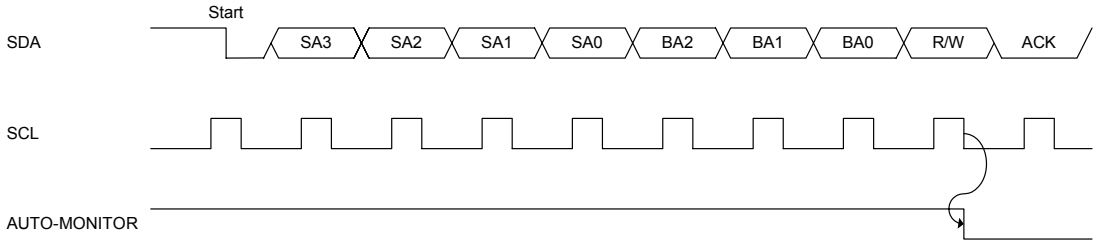


Figure 9A: Auto-monitor is paused on the falling edge of SCL during the R/W bit following a valid slave address.

Re-Enabling Auto-Monitor: I^2C Read Transaction

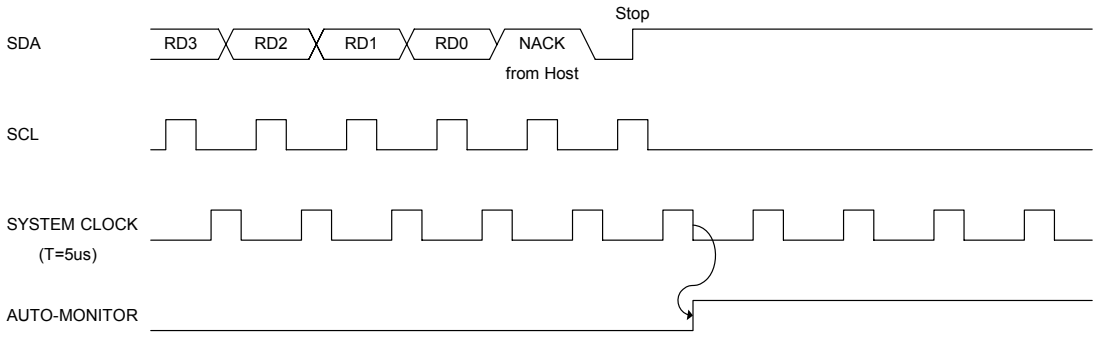


Figure 9B: At the end of an I^2C read transaction, auto-monitor is re-enabled on the falling edge of the internal system clock after the Stop.

APPLICATIONS INFORMATION (CONTINUED)

Re-Enabling Auto-Monitor: I²C Command Write Transaction

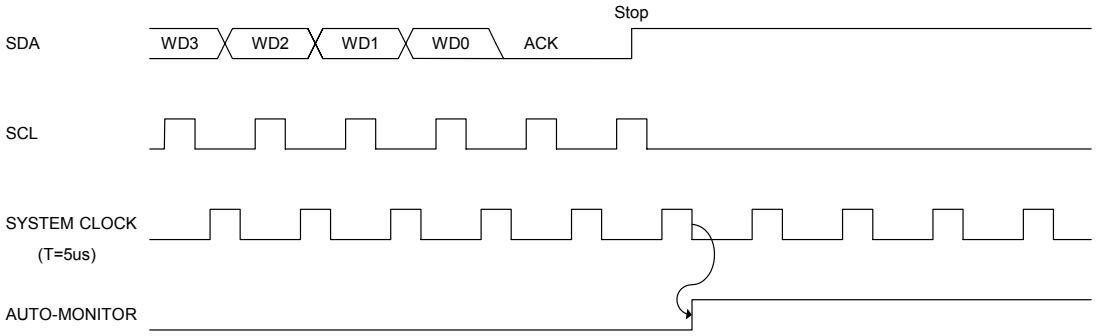


Figure 9C: At the end of an I²C command write transaction, auto-monitor is re-enabled on the falling edge of the internal system clock after the Stop. The I²C command write is any write to slave address 9Xh, word address 8Xh.

Re-Enabling Auto-Monitor: I²C Writes to Configuration, General Purpose Memory and Margin Control Registers

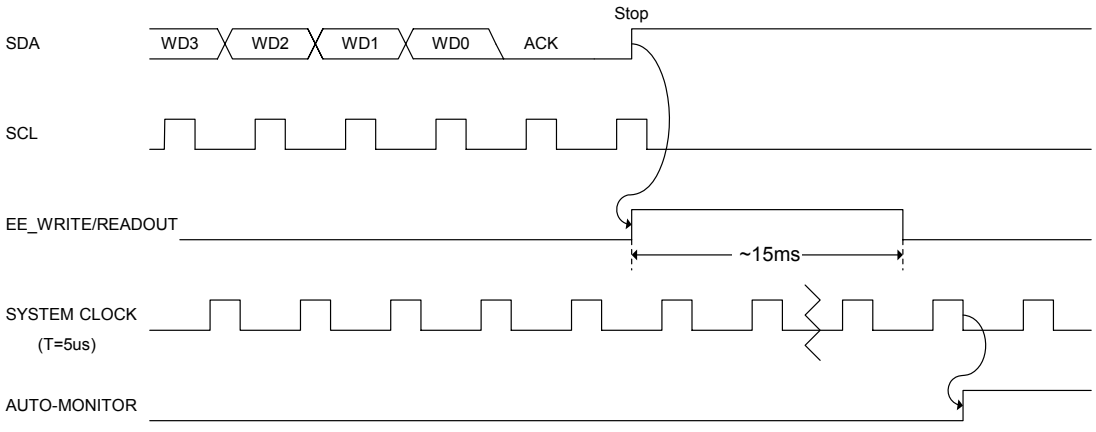


Figure 9D: At the end of an I²C write to configuration, general purpose memory or margin control registers, auto-monitor is re-enabled on the falling edge of the internal system clock after the EE_WRITE/READOUT has completed.

APPLICATIONS INFORMATION (CONTINUED)

Re-Enabling Auto-Monitor: Auto-Monitor Timeout

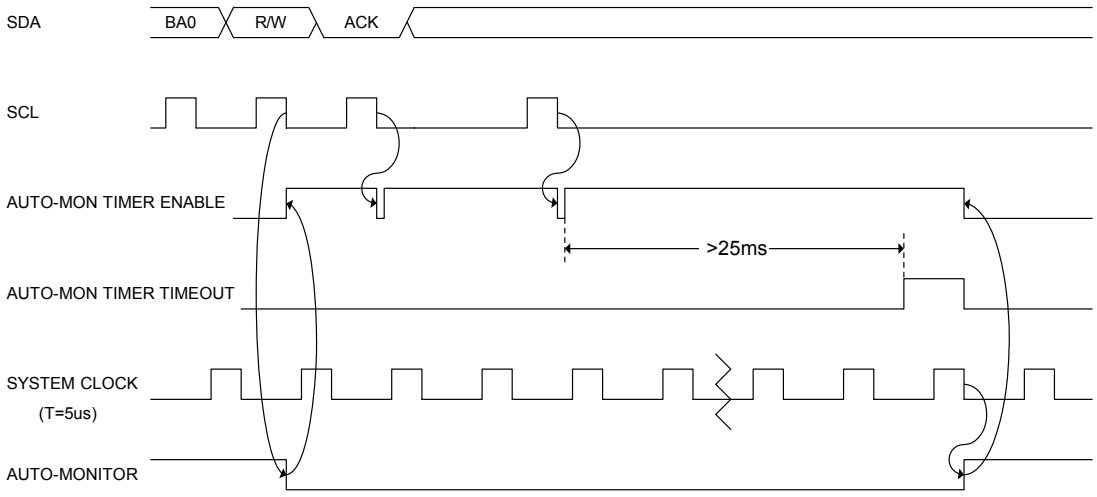


Figure 9E: Auto-monitor is re-enabled on the falling edge of the internal system clock after the auto-monitor timer has timed out. The auto-monitor timer is enabled when auto-monitor is paused and is restarted on the falling edge of SCL.

APPLICATIONS INFORMATION (CONTINUED)

Re-Enabling Auto-Monitor: Invalid Slave Address

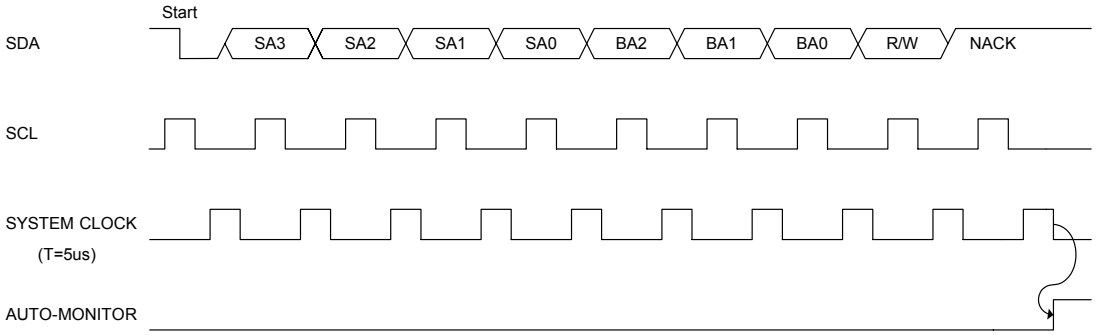


Figure 9F: Auto-monitor is re-enabled on the falling edge of the internal system clock after the falling edge of SCL during the NACK following a invalid slave address.

Re-Enabling Auto-Monitor: Invalid Slave Address During an I²C A-to-D Conversion

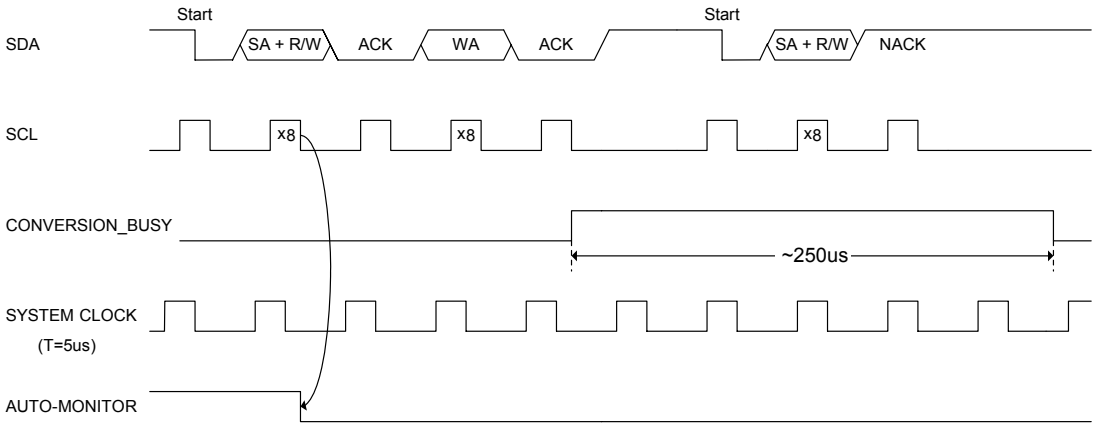


Figure 9G: During the 250us A-to-D conversion time, the activity on SDA and SCL are ignored.

APPLICATIONS INFORMATION (CONTINUED)

Re-Enabling Auto-Monitor: Invalid Slave Address During an I²C A-to-D Conversion

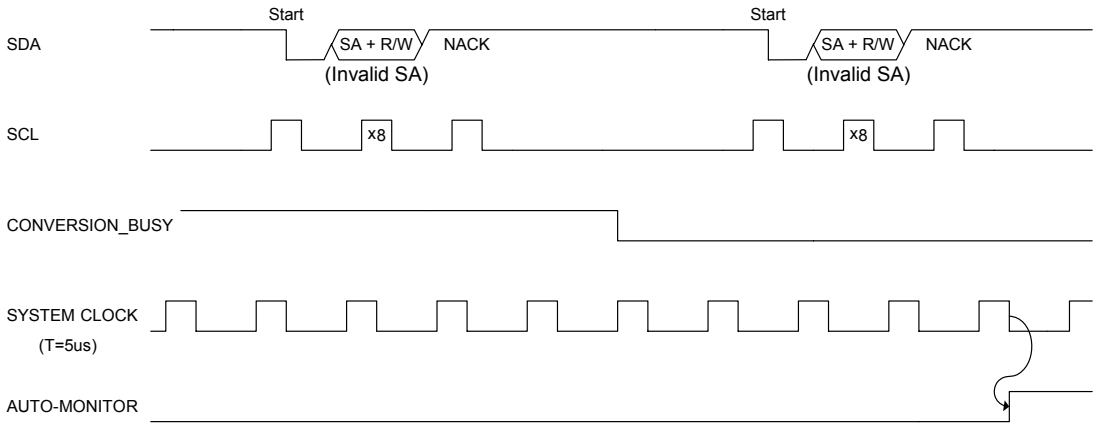


Figure 9H: Auto-monitor is re-enabled on the falling edge of the internal system clock after the falling edge of SCL during the NACK following a invalid slave address after the conversion has completed.

APPLICATIONS INFORMATION (CONTINUED)

RESTART OF POWER-ON CASCADE SEQUENCING

Once a Force Shutdown or Power-off operation has completed, the SMM665C can restart the Power-on cascade sequencing. The device can be programmed to automatically restart after a Force Shutdown provided the PWR_ON/OFF pin remains in the active state or the I^2C Power-on command remains in the command register. If this option is not selected, the SMM665C requires toggling of the PWR_ON/OFF pin or toggling of the I^2C commands by issuing a Power-off command and then reissuing the Power-on command in order to restart Power-on sequencing.

In either case, assertion of the FS pin will prevent the SMM665C from restarting Power-on sequencing. In addition, the device can be programmed to check that VDD and the 12VIN are within their programmed voltage thresholds before restarting Power-on sequencing.

In cases where brownout conditions (Figure 10) or loss of power are used to cause a sequence off of the supplies or a Force Shutdown, it is best to toggle the PWR_ON/OFF pin or use the I^2C Power commands after the brownout condition is over or if the supplies do not fully discharge before initiating a Power-on sequence.

Recommended Use of the PWR_ON/OFF pin:

The PWR_ON/OFF pin is edge-triggered to lock out false or nuisance signals during both the power-on and power-off sequences. If during a system power-down, whether deliberate or due to a failed power system, the VDD_CAP voltage falls below 2.5V, the SMM665C internal UVLO (UnderVoltage LockOut) circuit resets all internal logic. Once power has recovered above 2.6V the SMM665C will restart assuming the PWR_ON/OFF pin is in the asserted state or an I^2C power command is issued. The SMM665C can be used with the PWR_ON/OFF pin either toggled by a logic level, controlled by a software command or tied either high or low as described in the data sheet.

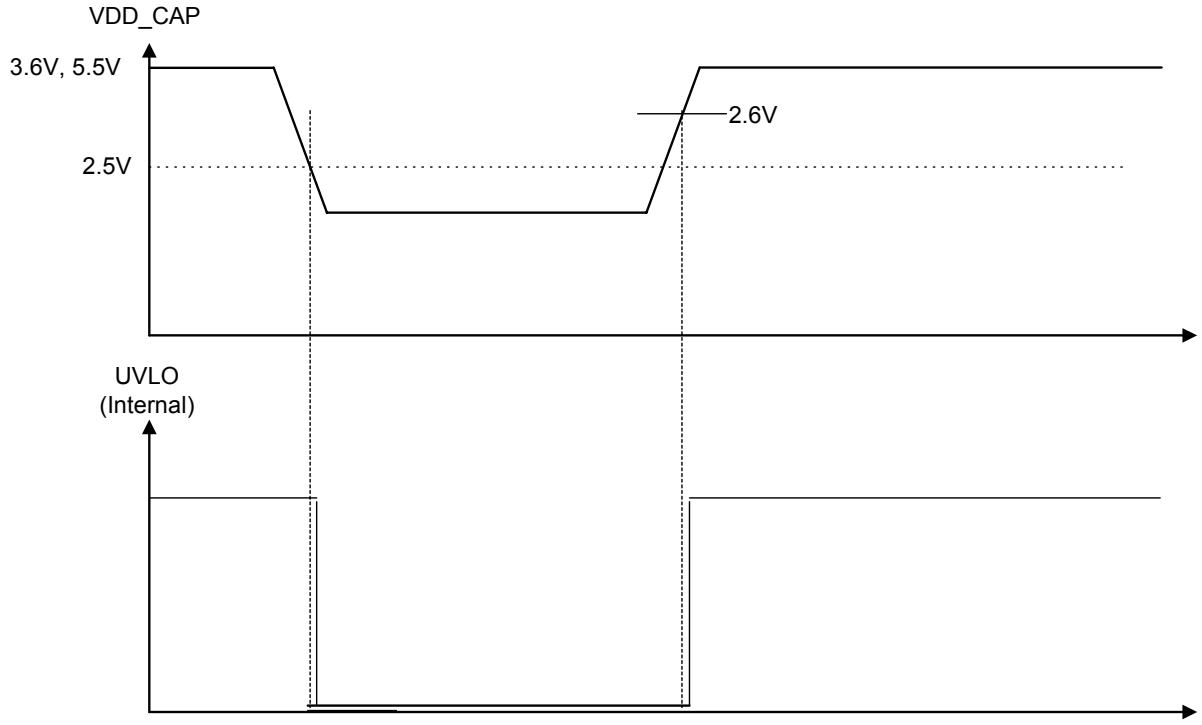


Figure 10 - Timing Sequence recovering from a VDD_CAP Power 'Brown-Out'

APPLICATIONS INFORMATION (CONTINUED)

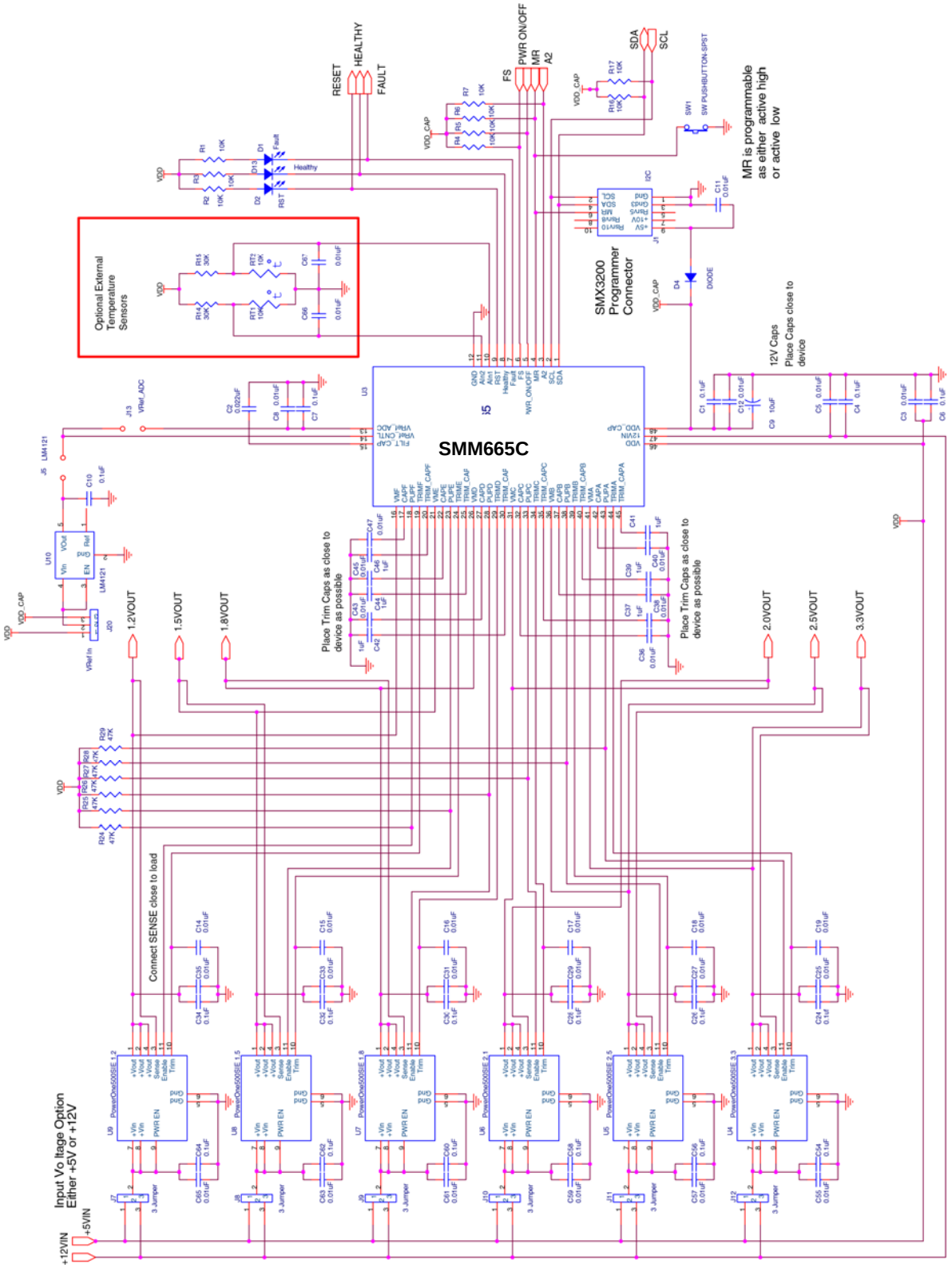


Figure 11 – SMM665C Distributed power applications schematic. The accuracy of the external reference (U10) sets the accuracy of the ADOC function. Total accuracy with a ±0.1% external reference is ±0.2%.

APPLICATIONS INFORMATION (CONTINUED)

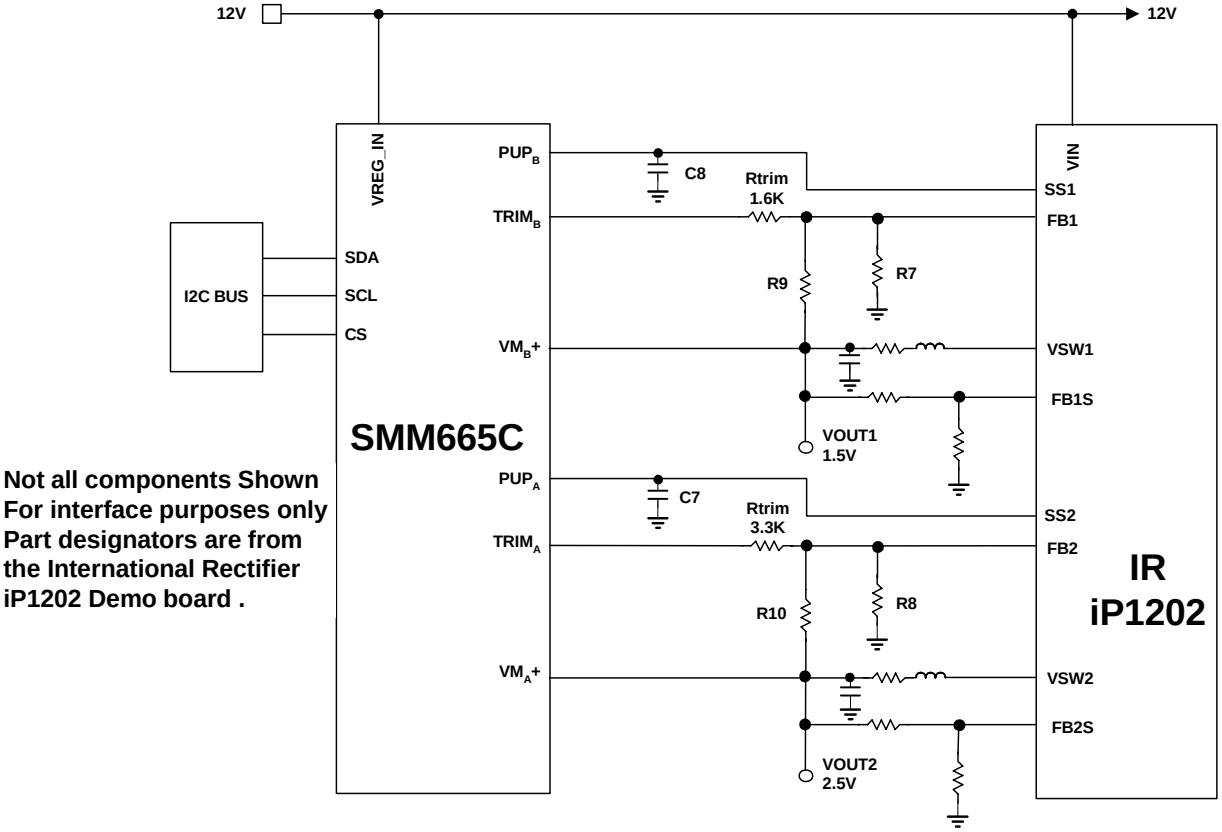


Figure 12 – The SMM665C can be used to sequence and control discrete DC switching regulators. The ADOC function sets the output voltage of the IR iP1202 Regulator through the FBX feedback pins. Accuracy is improved even under full load, essentially acting as a "SENSE" pin. The sequence function is applied through the iP1202 SSX soft start pins.

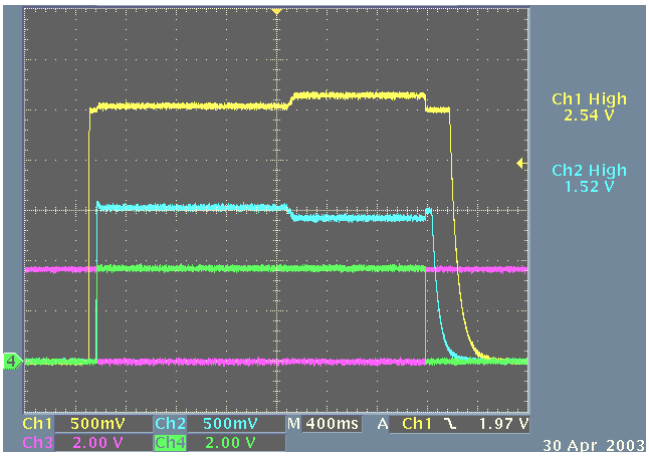


Figure 13 – Ch1 is set to 2.5V and Ch2 is set to 1.5V on the ip1202 board. Ch1 is set to sequence on first followed by Ch2 after 50ms. Then Ch1 is margined high while Ch2 is margined low. Ch2 is then sequenced off followed by Ch1 after 50ms.

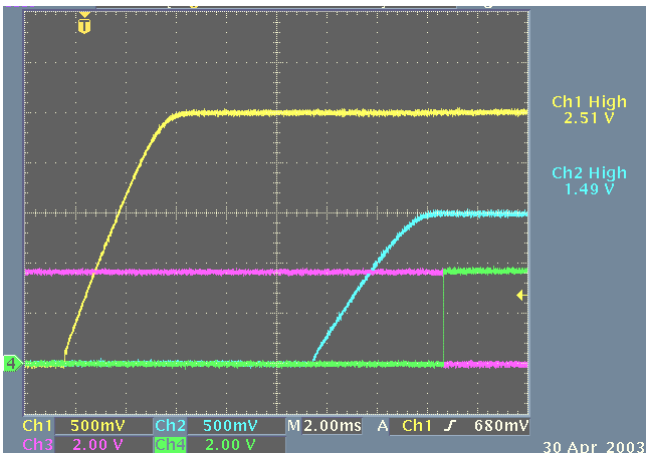


Figure 14 – This is the same sequencing-on function but with a shorter delay between channels, the HEALTHY and RESET flags are also shown.

DEVELOPMENT HARDWARE & SOFTWARE

The end user can obtain the Summit SMX3200 programming system for device prototype development. The SMX3200 system consists of a programming Dongle, cable and Windows™ GUI software. It can be ordered on the website or from a local representative.

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus.

The Windows GUI software will generate the data and send it in I^2C serial bus format so that it can be directly downloaded to the SMM665C via the programming Dongle and cable. An example of the connection interface is shown in Figure 15.

When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

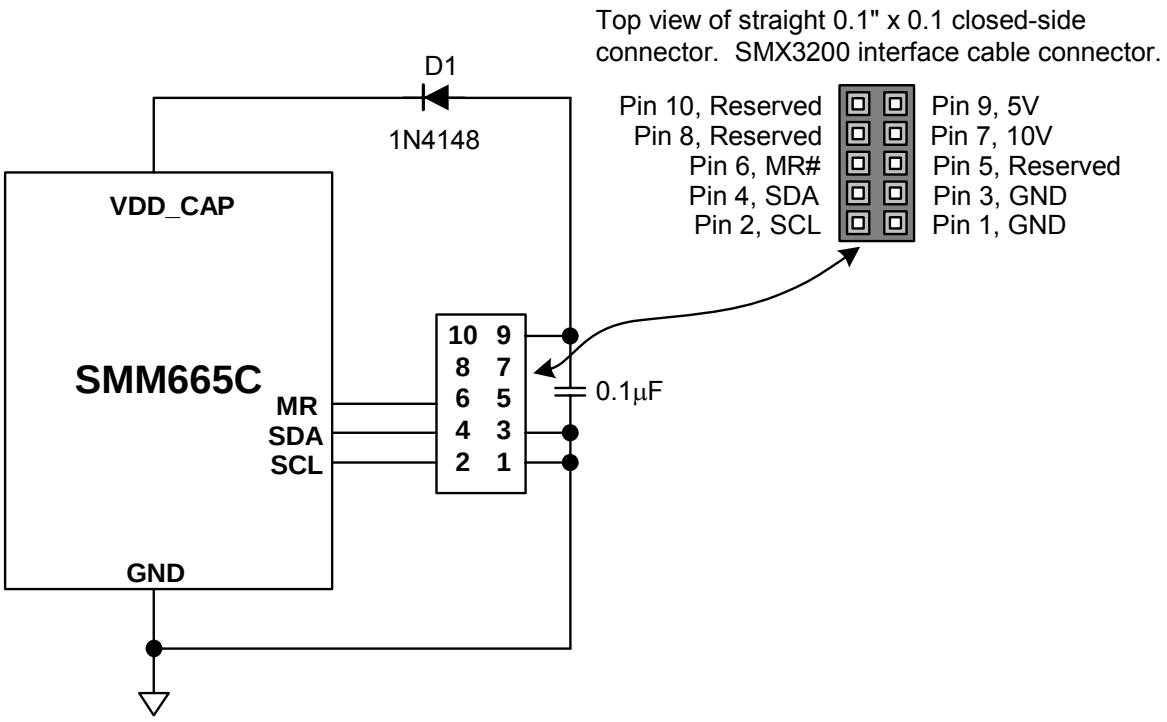


Figure 15 – SMX3200 Programmer I^2C serial bus connections to program the SMM665C. Note that the MR pin does not need to be connected to pin 6 for programming purposes.

The latest revisions of all software and an application brief describing the SMX3200 is available from the website at:

http://www.summitmicro.com/tech_support/program_kit/SMX3200.htm

I²C PROGRAMMING INFORMATION

SERIAL INTERFACE

Access to the configuration registers, general-purpose memory and command and status registers is carried out over an industry standard 2-wire serial interface (I^2C). SDA is a bi-directional data line and SCL is a clock input. Data is clocked in on the rising edge of SCL and clocked out on the falling edge of SCL. All data transfers begin with the MSB. During data transfers SDA must remain stable while SCL is high. Data is transferred in 8-bit packets with an intervening clock period in which an Acknowledge is provided by the device receiving data. The SCL high period (t_{HIGH}) is used for generating Start and Stop conditions that precede and end most transactions on the serial bus. A high-to-low transition of SDA while SCL is high is considered a Start condition while a low-to-high transition of SDA while SCL is high is considered a Stop condition.

The interface protocol allows operation of multiple devices and types of devices on a single bus through unique device addressing. The address byte is comprised of a 4-bit device type identifier (slave address) and a 3-bit bus address. The remaining bit indicates either a read or a write operation. Refer to Table 1 for a description of the address bytes used by the SMM665C.

The device type identifier for the memory array is generally set to 1010_{BIN} following the industry standard for a typical nonvolatile memory. There is an option to change the identifier to 1011_{BIN} allowing it to be used on a bus that may be occupied by other memory devices. The configuration registers are grouped with the memory array and thus use 1010_{BIN} or 1011_{BIN} as the device type identifier. The command and status registers as well as the 10-bit ADC are accessible with the separate device type identifier of 1001_{BIN}.

The bus address bits A[1:0] are programmed into the configuration registers. Bus address bit A[2] can be programmed as either 0 or biased by the A2 pin. The bus address accessed in the address byte of the serial data stream must match the setting in the SMM665C and on the A2 pin.

Any access to the SMM665C on the I^2C bus will temporarily halt the monitoring function. This does not affect the ADOC function, which will continue functioning and control the DC outputs. This is true not only during the monitor mode, but also during Power-on and Power-off sequencing when the device is monitoring the channels to determine if they have turned on or turned off.

The SMM665C halts the monitor function from when it acknowledges the address byte until a valid stop is received.

WRITE

Writing to the memory or a configuration register is illustrated in Figures 16, 17, 19, 21 and 22. A Start condition followed by the address byte is provided by the host; the SMM665C responds with an Acknowledge; the host then responds by sending the memory address pointer or configuration register address pointer; the SMM665C responds with an acknowledge; the host then clocks in on byte of data. For memory and configuration register writes, up to 15 additional bytes of data can be clocked in by the host to write to consecutive addresses within the same page. After the last byte is clocked in and the host receives an Acknowledge, a Stop condition must be issued to initiate the nonvolatile write operation.

READ

The address pointer for the configuration registers, memory, command and status registers and ADC registers must be set before data can be read from the SMM665C. This is accomplished by a issuing a dummy write command, which is simply a write command that is not followed by a Stop condition. The dummy write command sets the address from which data is read. After the dummy write command is issued, a Start command followed by the address byte is sent from the host. The host then waits for an Acknowledge and then begins clocking data out of the slave device. The first byte read is data from the address pointer set during the dummy write command. Additional bytes can be clocked out of consecutive addresses with the host providing an Acknowledge after each byte. After the data is read from the desired registers, the read operation is terminated by the host holding SDA high during the Acknowledge clock cycle and then issuing a Stop condition. Refer to Figures 18, 20 and 23 for an illustration of the read sequence.

I²C PROGRAMMING INFORMATION (CONTINUED)

WRITE PROTECTION

The SMM665C powers up into a write protected mode. Writing a code to the volatile write protection register can disable the write protection. The write protection register is located at address 87_{HEX} of slave address 1001_{BIN}.

Writing 0101_{BIN} to bits [7:4] of the write protection register allow writes to the general-purpose memory while writing 0101_{BIN} to bits [3:0] allow writes to the configuration registers. The write protection can re-enable by writing other codes (not 0101_{BIN}) to the write protection register. Writing to the write protection register is shown in Figure 16.

CONFIGURATION REGISTERS

The majority of the configuration registers are grouped with the general-purpose memory located at either slave address 1010_{BIN} or 1011_{BIN}. The bus address bits, A[1:0], used to differentiate the general-purpose memory from the configuration registers are set to 11_{BIN}. Bus address bit A[2] can be programmed as either 0 or biased by the A2 pin.

Two additional configuration registers are located at addresses 83_{HEX} and 84_{HEX} of slave address 1001_{BIN}.

Writing and reading the configuration registers is shown in Figures 17, 18, 19, 20 and 21

Note: Configuration writes or reads of registers 00_{HEX} to $0F_{HEX}$ should not be performed while the SMM665C is margining.

GENERAL-PURPOSE MEMORY

The 4k-bit general-purpose memory is located at either slave address 1010_{BIN} or 1011_{BIN}. The bus address bits, A[1:0], used to differentiate the general-purpose memory from the configuration registers are set to 00_{BIN} for the first 2k-bits and 01_{BIN} for the second 2k-bits. Bus address bit A[2] can be programmed as either 0 or biased by the A2 pin. The word address must be set each time the memory is accessed.

Memory writes and reads are shown in Figures 22, 23 and 24.

COMMAND AND STATUS REGISTERS

The command and status registers are located at slave address 1001_{BIN}. Writes and reads of the command and status registers are shown in Figures 25 and 26.

ADC CONVERSIONS

An ADC conversion on any monitored channel can be performed and read over the I²C bus using the ADC read command and requires 182µs to complete. The ADC read command, shown in Figure 27, starts with a dummy write to the 1001_{BIN} slave address. Bits [6:3] of the word address byte are used to address the desired monitored input. Once the device acknowledges the channel address, it begins the ADC conversion of the addressed input. This conversion requires 70µs to complete. During this conversion time, acknowledge polling can be used. The SMM665C will not acknowledge the address bytes until the conversion is complete. When the conversion has completed, the SMM665C will acknowledge the address byte and return the 10-bit conversion along with a 4-bit channel address echo.

GRAPHICAL USER INTERFACE (GUI)

Device configuration utilizing the Windows based SMM665C graphical user interface (GUI) is highly recommended. The software is available from the Summit website at:
(http://www.summitmicro.com/tech_support/tech.htm#GUI.
Using the GUI in conjunction with this datasheet and Application Note 33, simplifies the process of device prototyping and the interaction of the various functional blocks. A programming Dongle (SMX3200) is available from Summit to communicate with the SMM665C. The Dongle connects directly to the parallel port of a PC and programs the device through a cable using the I²C bus protocol.

Slave Address	Bus Address	Register Type
1001_{BIN}	A2 A1 A0	Write Protection Register, Command and Status Registers, Two Configuration Registers, ADC Conversion Readout
1010_{BIN} or 1011_{BIN}	A2 0 0	1st 2-k Bits of General-Purpose Memory
	A2 0 1	2nd 2-k Bits of General-Purpose Memory
	A2 1 1	Configuration Registers

Table 1 - Address bytes used by the SMM665C.

I²C PROGRAMMING INFORMATION (CONTINUED)

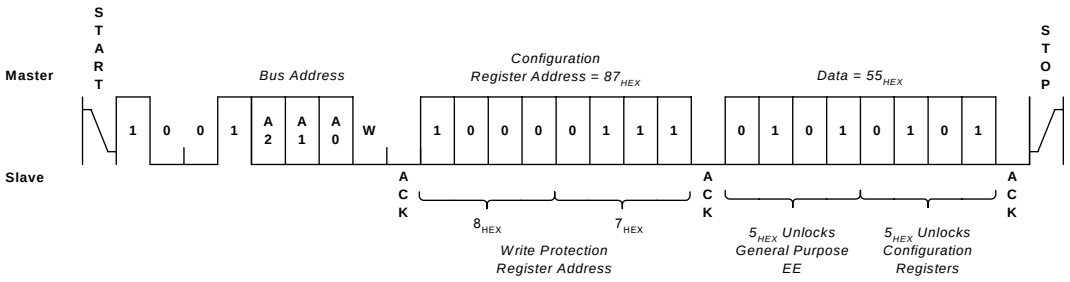


Figure 16 – Write Protection Register Write

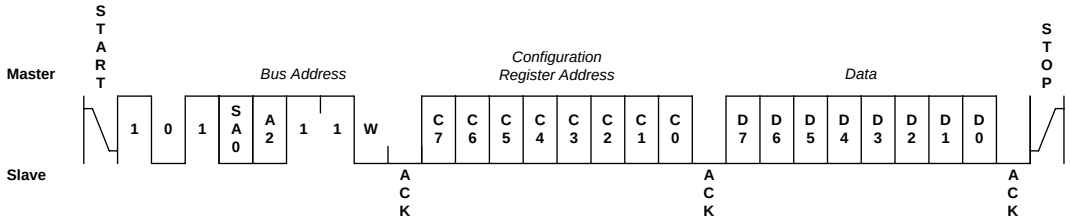


Figure17 – Configuration Register Byte Write

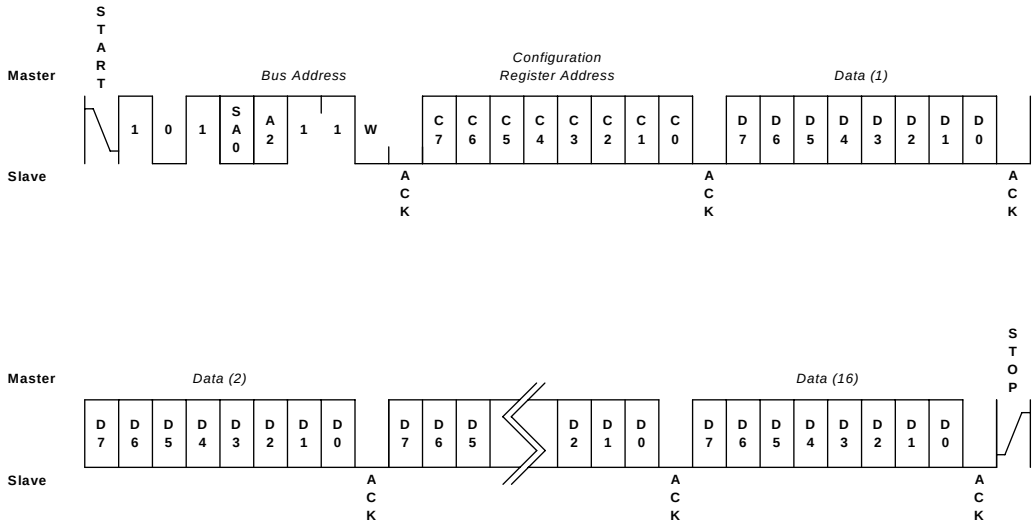


Figure 18 – Configuration Register Page Write

I²C PROGRAMMING INFORMATION (CONTINUED)

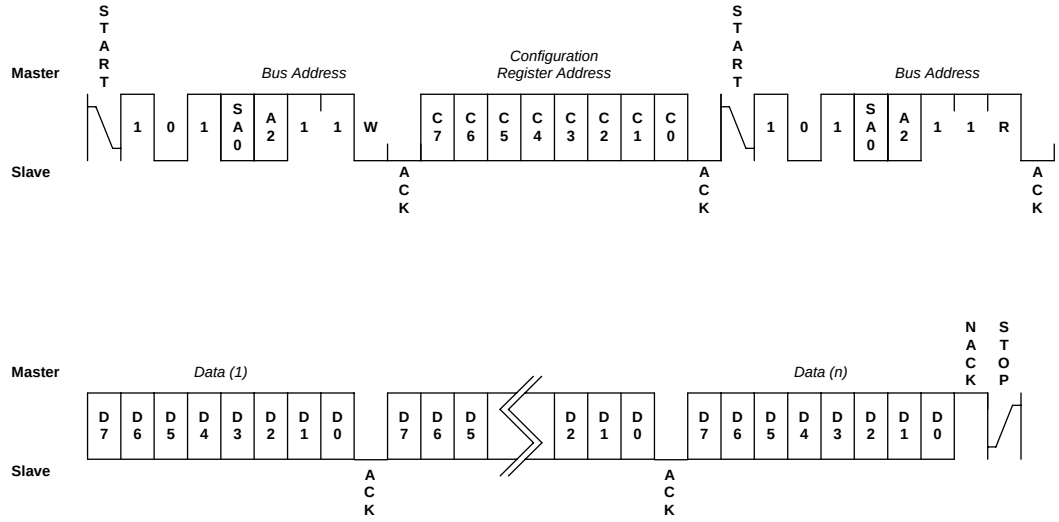


Figure 19 - Configuration Register Read

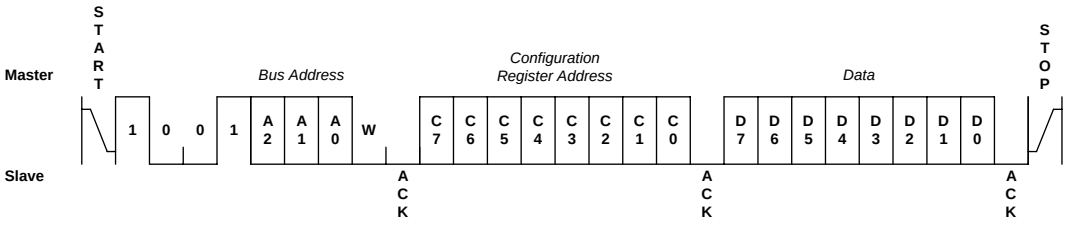


Figure 20 - Configuration Register with Slave Address 1001_{BIN} Write

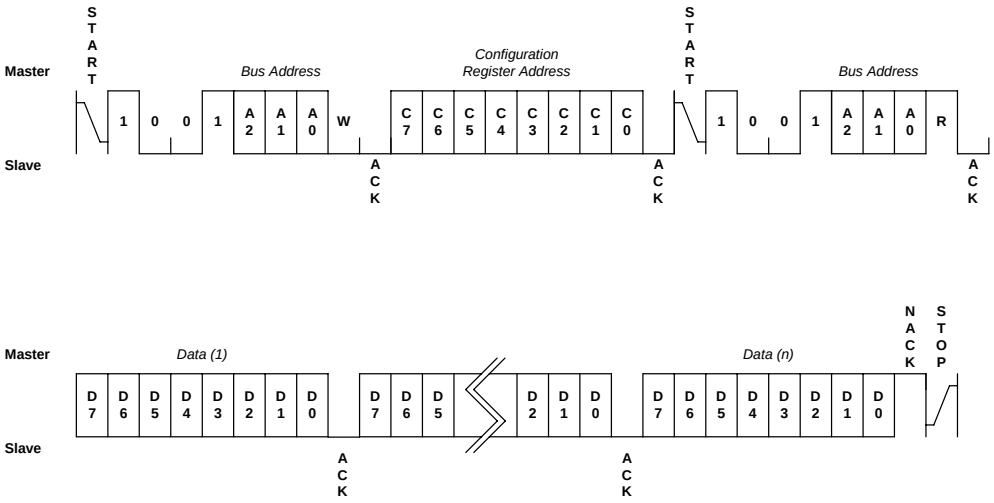


Figure 21 - Configuration Register with Slave Address 1001_{BIN} Read

I²C PROGRAMMING INFORMATION (CONTINUED)

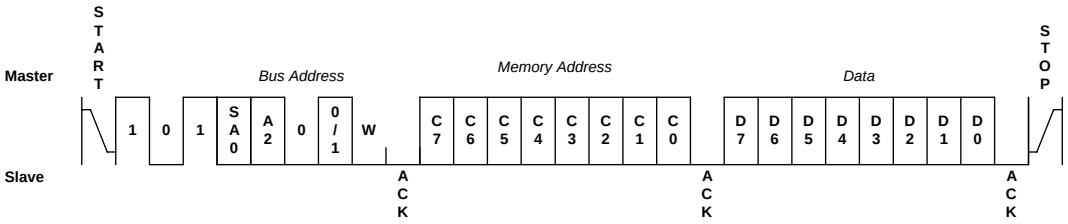
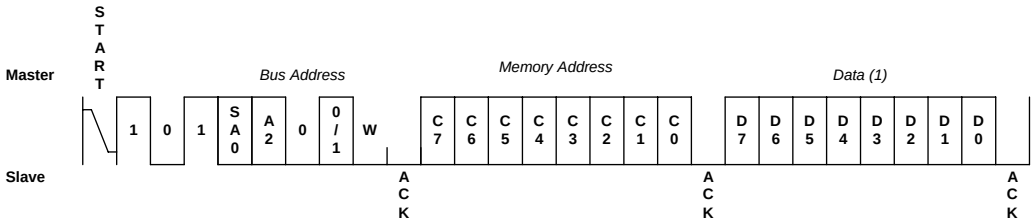


Figure 22 – General Purpose Memory Byte Write



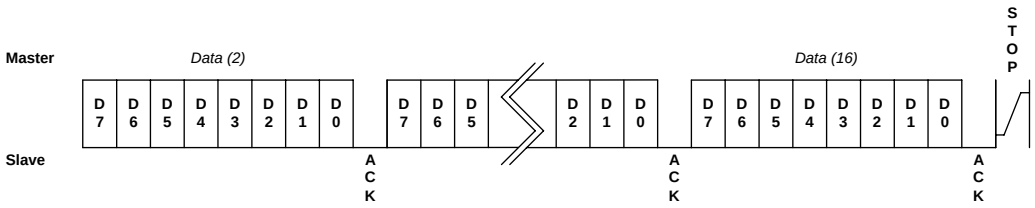
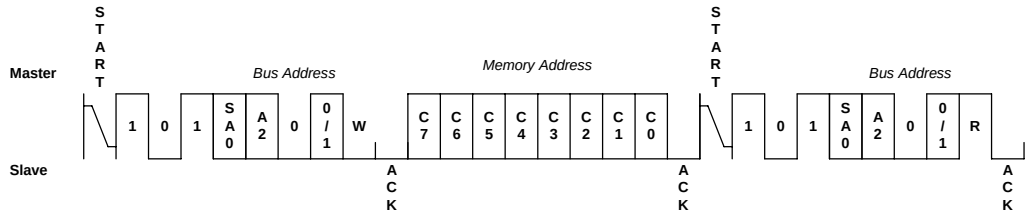


Figure 23 - General Purpose Memory Page Write



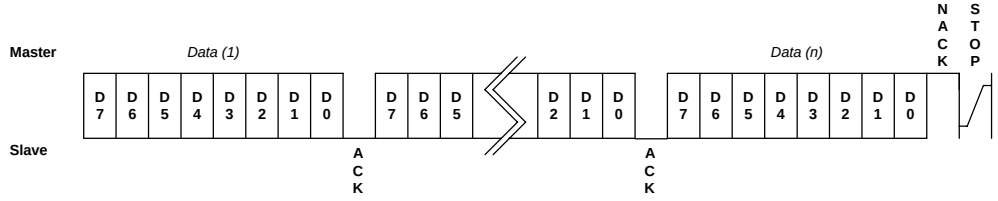


Figure 24 - General Purpose Memory Read

I²C PROGRAMMING INFORMATION (CONTINUED)

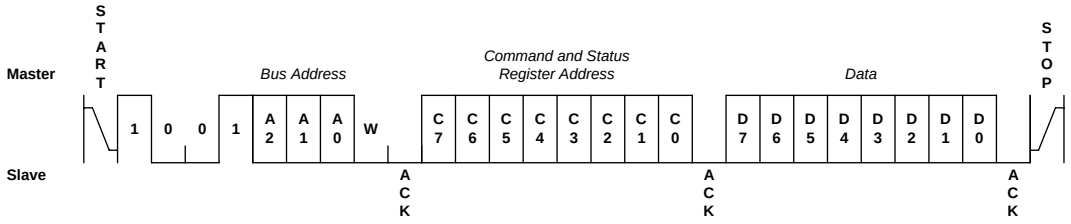
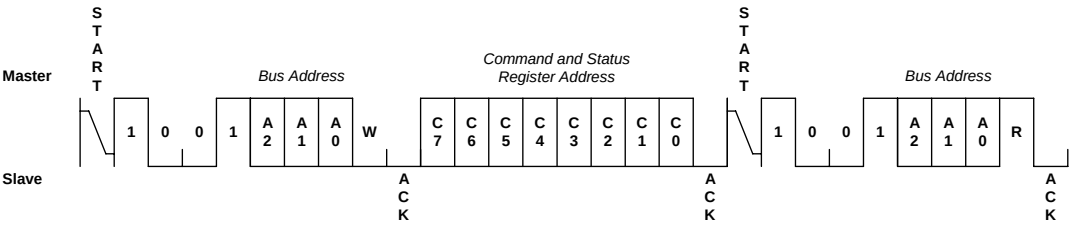


Figure 25 – Command and Status Register Write



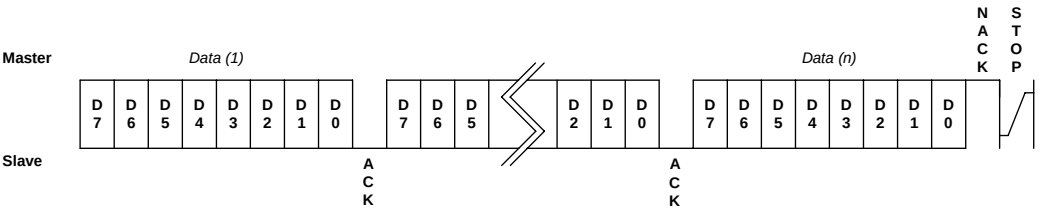


Figure 26 - Command and Status Register Read

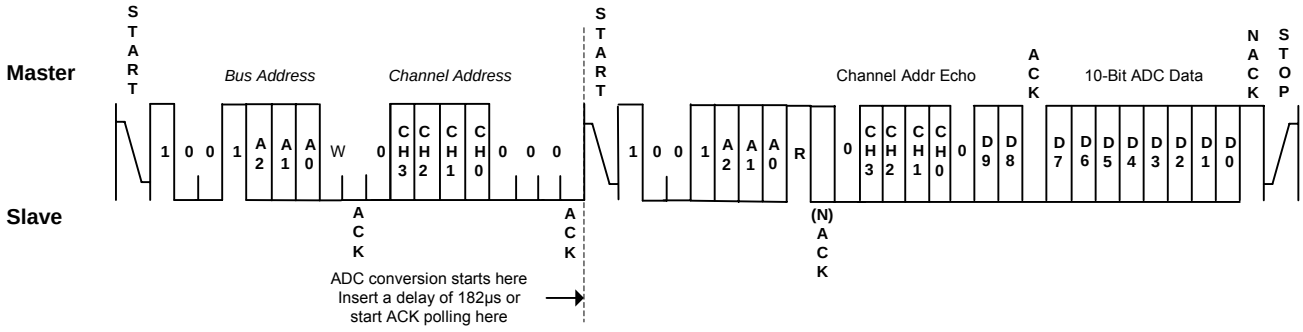


Figure 27 – ADC Conversion Read

DEFAULT CONFIGURATION REGISTER SETTINGS – SMM665CFC-802

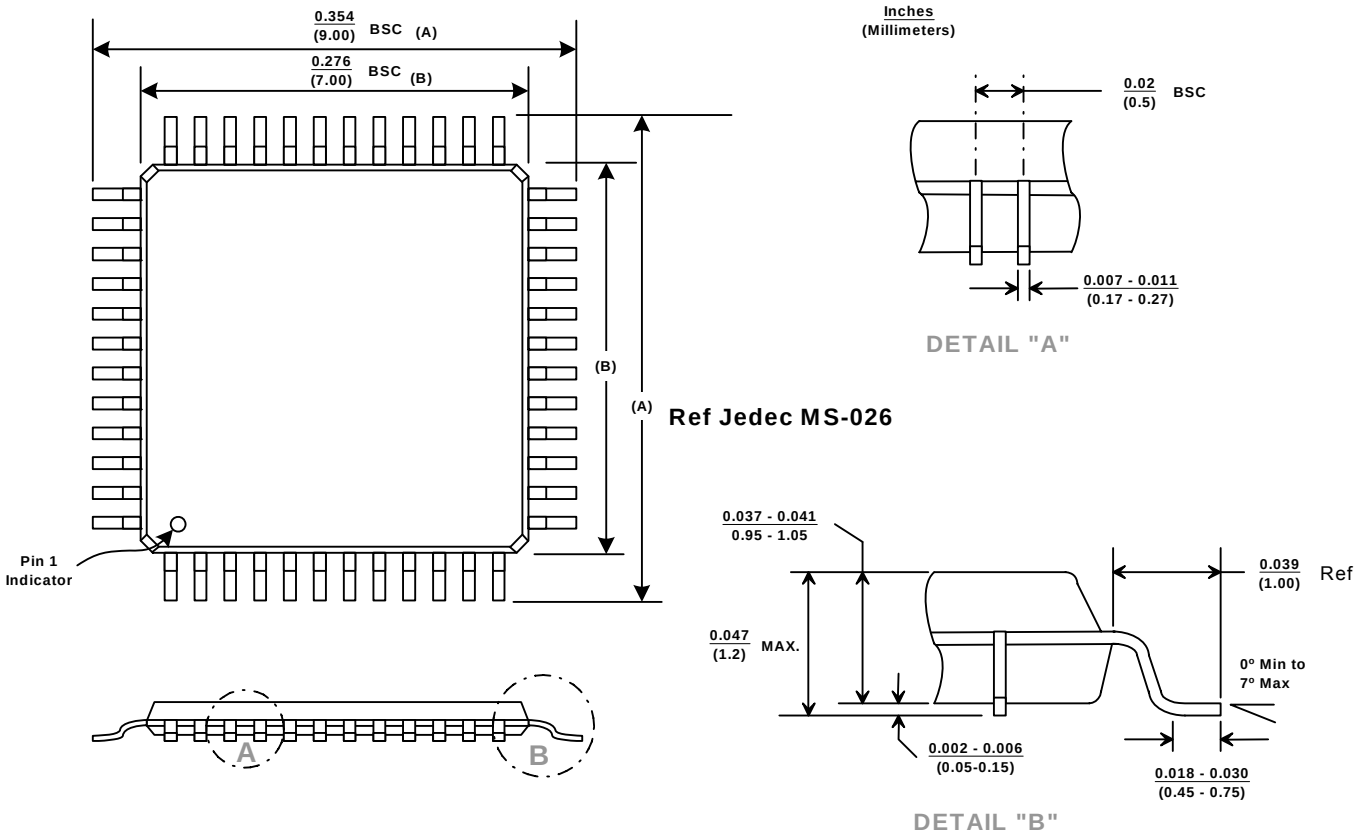
Register	Contents	Register	Contents	Register	Contents	Register	Contents
R0	0D	R40	0D	R98	41	RBF	E0
R1	83	R41	B9	R99	3E	RC0	0B
R2	0D	R42	0E	R9A	81	RC1	38
R3	FF	R43	39	R9B	33	RC2	0B
R4	0E	R44	0E	R9C	29	RC3	38
R5	61	R45	A4	R9D	9A	RC4	09
R6	0E	R46	0F	R9E	11	RC5	90
R7	C7	R47	16	R9F	AE	RC6	09
R8	0F	R48	0F	RA0	41	RC7	90
R9	54	R49	B4	RA1	0B	RC8	0C
RA	0B	R4A	06	RA2	80	RC9	00
RB	22	R4B	7F	RA3	F6	RCA	0C
RC	7F	R4C	00	RA4	29	RCB	00
RD	3F	R4D	12	RA5	5D	RCC	0F
RE	03	R4E	50	RA6	11	RCD	FF
RF	01	R80	42	RA7	71	RCE	0F
R10	8F	R81	48	RA8	40	RCF	FF
R11	9F	R82	82	RA9	CE	RD0	0C
R12	AF	R83	3E	RAA	80	RD1	00
R13	BF	R84	2A	RAB	8F	RD2	0C
R14	CF	R85	B8	RAC	29	RD3	00
R15	DF	R86	12	RAD	1F	RD4	0F
R18	00	R87	F6	RAE	11	RD5	D8
R19	00	R88	26	RAF	33	RD6	0F
R30	0D	R89	C8	RB0	2A	RD7	D8
R31	60	R8A	81	RB1	67	RE0	00
R32	0D	R8B	B9	RB2	0A	RE1	3D
R33	DC	R8C	2A	RB3	52	RE2	00
R34	0E	R8D	34	RB4	03	RE3	3D
R35	45	R8E	12	RB5	FF	RE4	00
R36	0E	R8F	49	RB6	03	RE5	3D
R37	A2	R90	49	RB7	FF	RE6	00
R38	0F	R91	5C	RB8	0D	RE7	3D
R39	08	R92	81	RB9	9A	RE8	00
R3A	0F	R93	52	RBA	0D	RE9	3D
R3B	D6	R94	29	RBB	56	REA	00
R3C	00	R95	D7	RBC	0F	REB	3D
R3D	12	R96	11	RBD	E0		
R3E	50	R97	EB	RBE	0F		

The default device ordering number is SMM665CFC-802. It is programmed with the register contents as shown above and tested over the commercial temperature range with a default VREF setting of 1.25V. Other standard external VREF voltage settings that can be specified and tested are values of: 1.024, 1.225, 1.250, 2.048, 2.500, 3.000 or 3.300. The value is derived from the customer supplied hex file. New device suffix numbers are assigned for all non-default VREF requirements. If other VREF values are required, please contact a Summit Microelectronics Sales Representative.

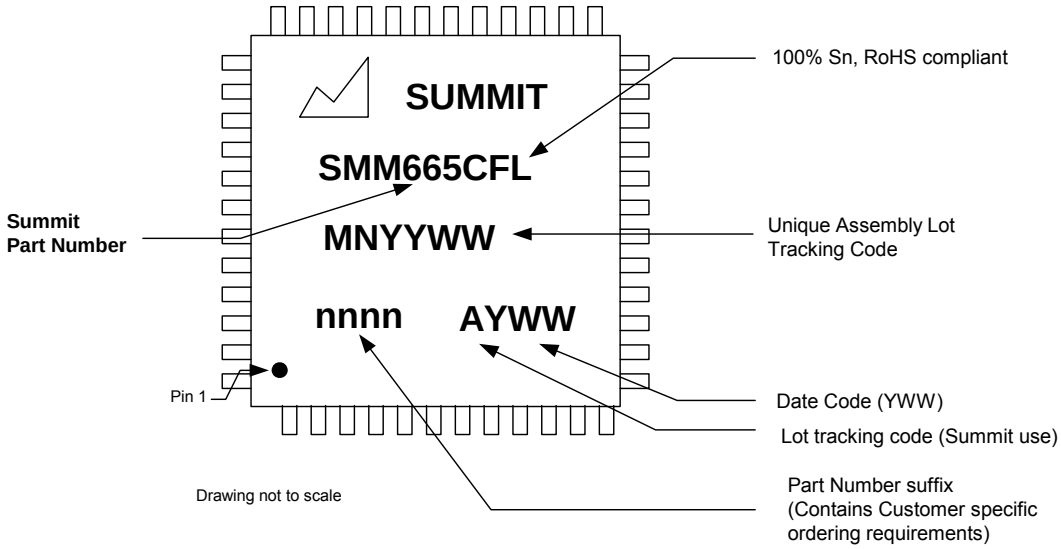
Application Note 33 contains a complete description of the Windows GUI and the default settings of each of the 154 individual Configuration Registers.

PACKAGE

48 PIN TQFP PACKAGE



PART MARKING



ORDERING INFORMATION

Summit Part Number **SMM665C** **F** **C** **nnnn** **L** — **Environmental Attribute**

Package
F = 48-Lead TQFP

Temp Range
C=Commercial
Blank=Industrial

Part Number Suffix
Specific requirements are contained in the suffix such as Hex code, Hex code revision, etc. The calibrated VREF voltage settings are standard values of: 1.024, 1.225, 1.250, 2.048, 2.500, 3.000 or 3.300

NOTICE

NOTE 1 - This is a ***Final*** data sheet that describes a Summit product currently in production.

Revision 3.2 - This document supersedes all previous versions.

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