1.4MHz, 18V，2A Synchronous Step-Down Converter

FEATURES

- High Efficiency: Up to 94%
- 1.4MHz Frequency Operation
- 2A Output Current
- No Schottky Diode Required
- 4.7V to 18V Input Voltage Range
- Output Voltages from 0.923V to 15V
- Slope Compensated Current Mode Control for Excellent Line and Load Transient Response
- Integrated internal compensation
- Low RDS(ON) Internal Power MOSFETs
- OCP, SCP, OVP, UVP Protection
- Thermal Shutdown
- Inrush Current Limit and Soft Start
- Available in SOP8 Package
- -40°C to +85°C Temperature Range

APPLICATIONS

- Distributed Power Systems
- Digital Set Top Boxes
- Flat Panel Television and Monitors
- Wireless and DSL Modems
- Notebook Computer

GENERAL DESCRIPTION

The MT2482 is a fully integrated, high–efficiency 2A synchronous rectified step-down converter. The MT2482 operates at high efficiency over a wide output current load range.

This device offers two operation modes, PWM control and PFM Mode switching control, which allows a high efficiency over the wider range of the load.

The MT2482 requires a minimum number of readily available standard external components and is available in an 8-pin SOIC ROHS compliant package.

Typical Application

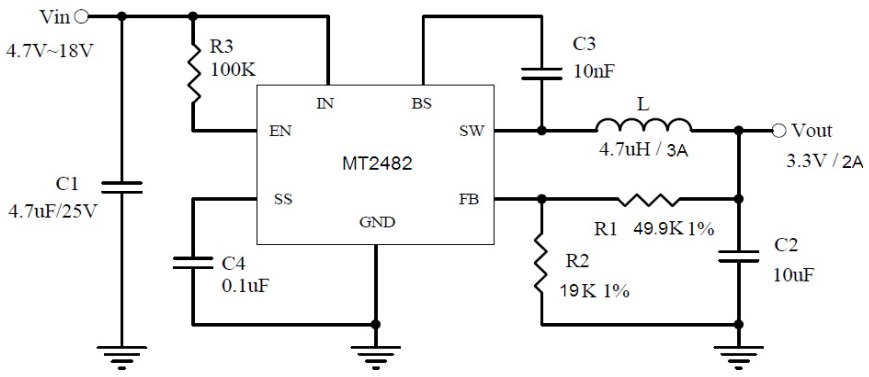


Figure 1. Basic Application Circuit

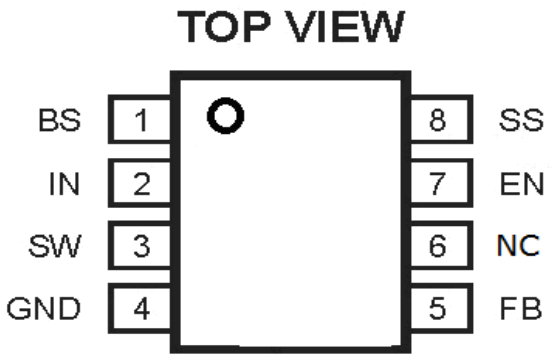
Absolute Maximum Ratings (Note 1)

Input Supply Voltage …… -0.3V to 20V
EN,FB Voltages ……..…-0.3 to 6V
SW Voltage ……-0.3V to (Vin+0.5V)
BS Voltage …….. (Vsw-0.3) to (Vsw+6V)
Operating Temperature Range … -40°C to +85°C
Lead Temperature(Soldering,10s) ……...+300°C
Storage Temperature Range …….-65°C to 150°C

Pin Description

PIN	NAME	FUNCTION
1	BS	Bootstrap. A capacitor connected between SW and BST pins is required to form a floating supply across the high-side switch driver.
2	VIN	Power supply Pin
3	SW	Switching Pin
4	GND	Ground
5	FB	Adjustable version feedback input. Connect FB to the center point of the external resistor divider.
6	NC	No Connect
7	EN	Enable Pin
8	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS unconnected.

Pin Configuration



Electrical Characteristics (Note 3)

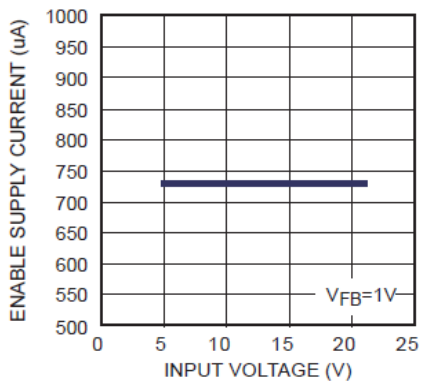
(V_{IN}=12V, V_{OUT}=3.3V, T_A = 25°C, unless otherwise noted.)

Parameter	Conditions	MIN	TYP	MAX	unit
Input Voltage Range		4.7		18	V
UVLO Threshold		3.8	4.2	4.5	V
Supply Current	V_{EN}=2.0V, V_{FB}=1.0V		1.3	1.5	mA
Regulated Feedback Voltage	T_A = 25°C, 4.7V≤V_{IN} ≤18V	0.900	0.925	0.950	V
Feedback Overvoltage Threshold			1.1		V
Error Amplifier Voltage Gain			500		V/V
High-Side/Low-Side Switch On-Resistance			100		m Ω
High-Side Switch Leakage Current	V_{EN}=0V, V_{SW}=0V		0	10	uA
Upper Switch Current Limit	Minimum Duty Cycle	2.2	3.4		A
Lower Switch Current Limit	From Drain to Source		0.9		A
Oscillation Frequency			1.4		MHz
EN Lockout Threshold Voltage		2.2	2.5	2.7	V
Soft-Start Current	Vss=0V		6		uA
Thermal Shutdown			160		℃

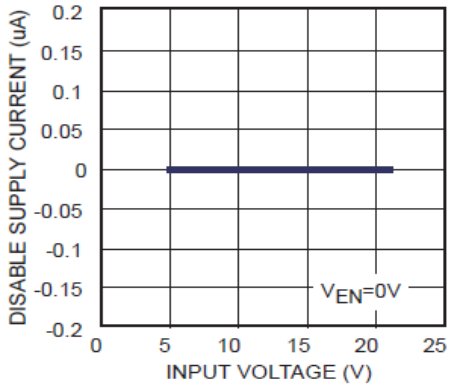
Typical Performance Characteristics

VIN = 12V, VOUT = 1.2V, L = 4.7μH, TA = +25ºC, unless otherwise noted.

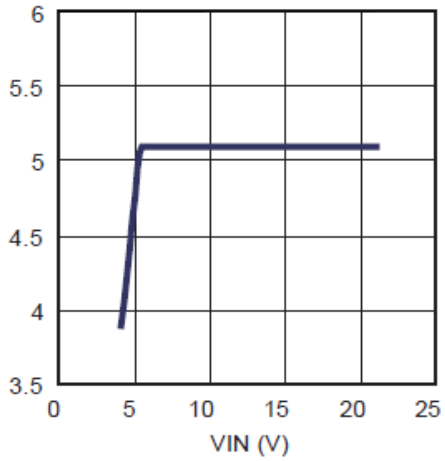
Enable Supply Current vs Input Voltage



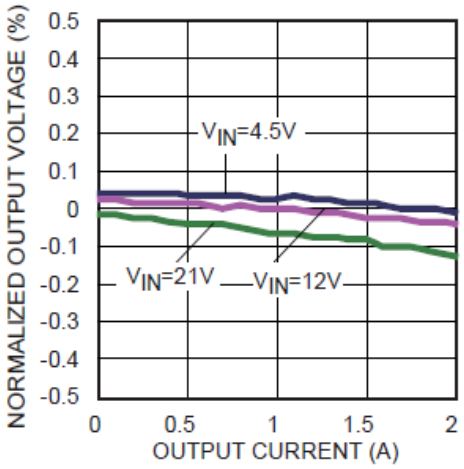
Disable Supply Current vs Input Voltage



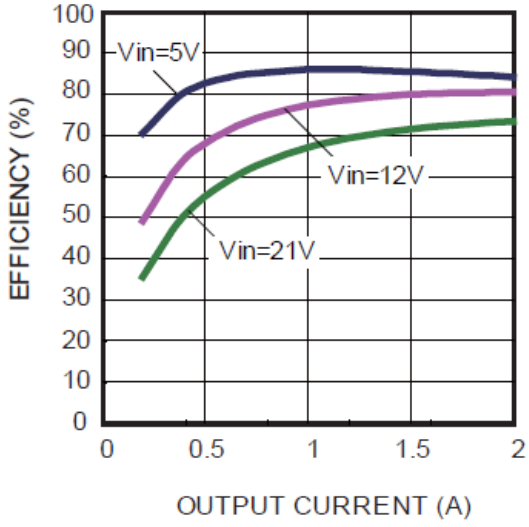
VCC Regulator Line Regulation



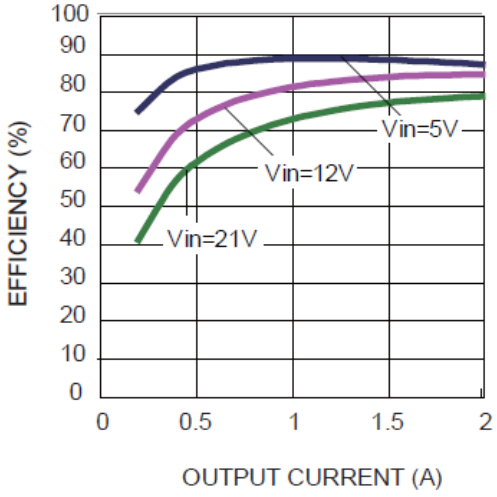
Load Regulation



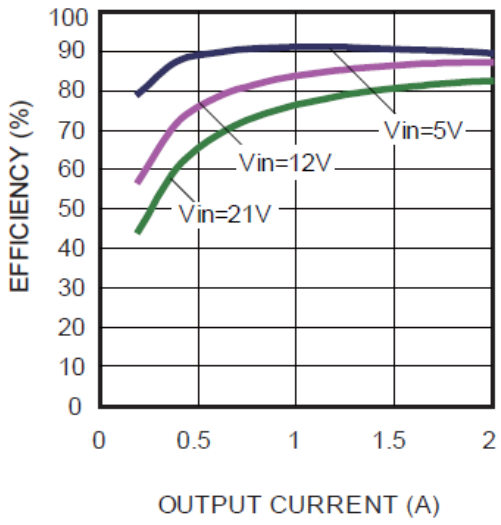
Efficiency VOUT=1.2V



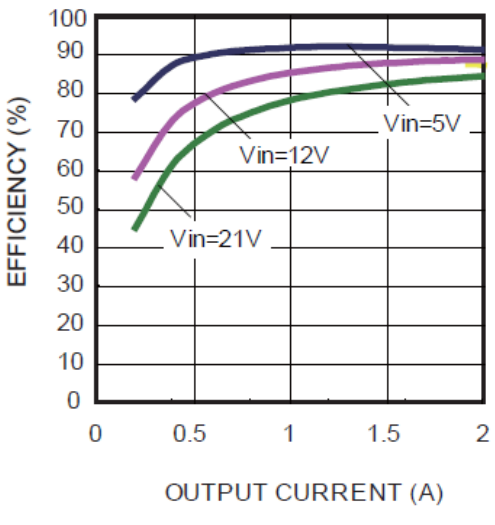
Efficiency VOUT=1.8V



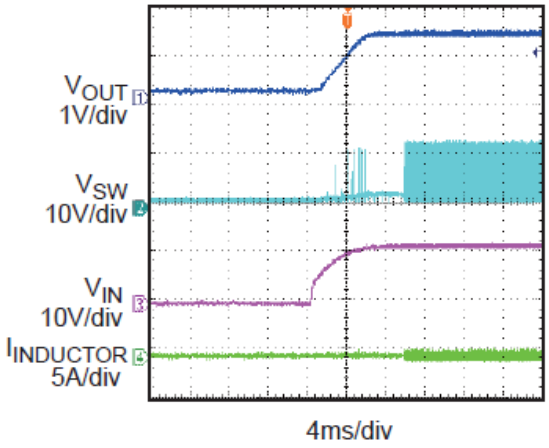
Efficiency VOUT=2.5V



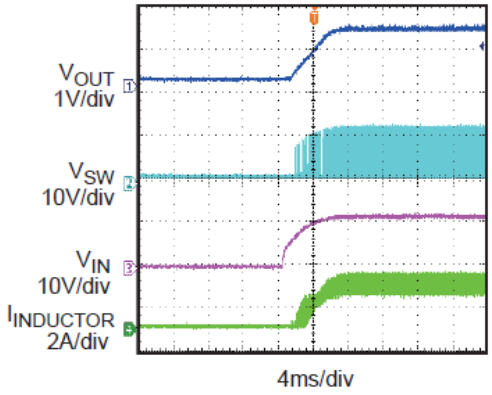
Efficiency VOUT=3.3V



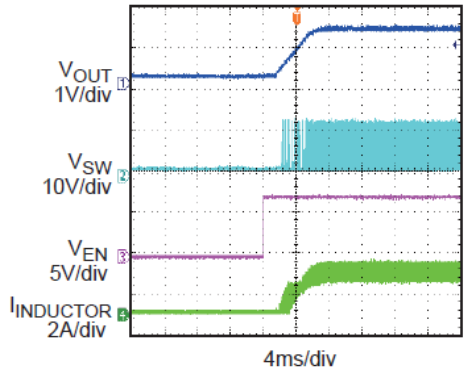
Power Up without Load



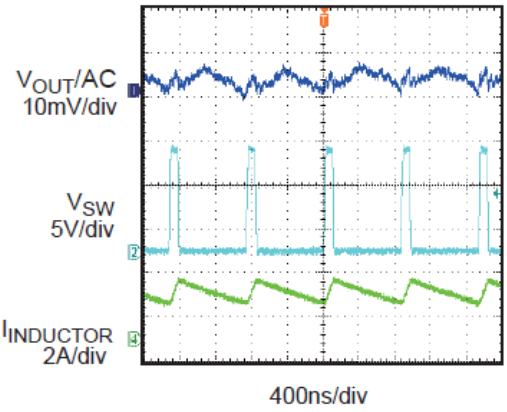
Power up with 2A Load



Enable Startup with 2A Load



Output Ripple Voltage IOUT=2A



Functional Block Diagram

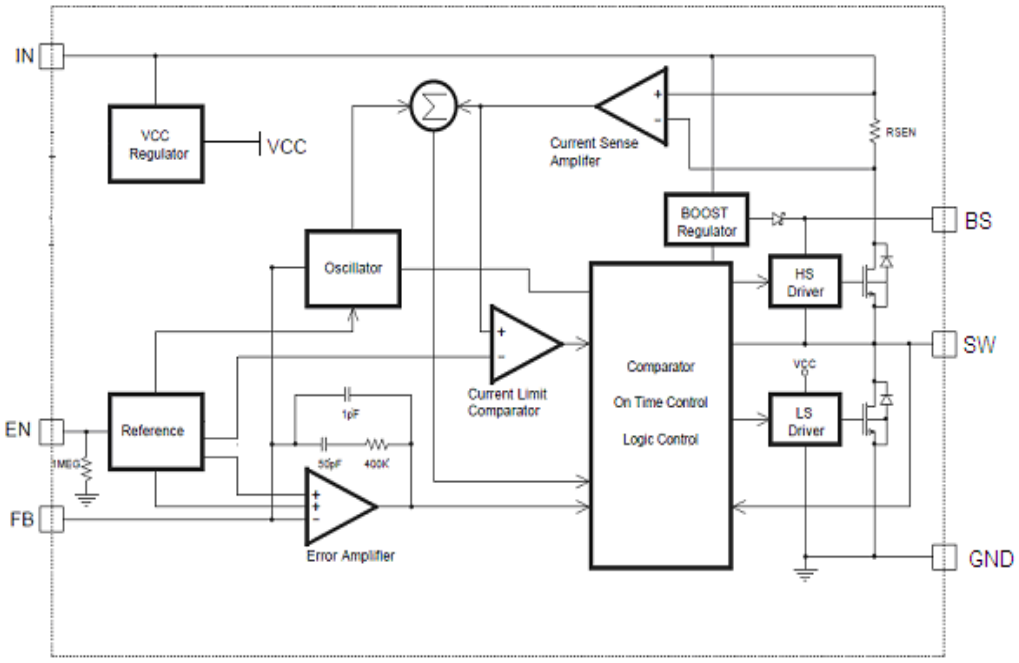


Figure 2. MT2482 Block Diagram

Functional Description

Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation. When VIN is lower than 5.0V, the output decreases, 0.1uF ceramic capacitor for decoupling purpose is required.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal FB reference (VFB) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The MT2482 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.0V while its falling threshold is a consistent 3.2V.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 1.2V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally fixed to

4ms.

Over-Current-Protection and Hiccup

The MT2482 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 30% below the reference. Once a UV is triggered, the MT2482 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The MT2482 exits the hiccup mode once the over current condition is removed.

Startup and Shutdown

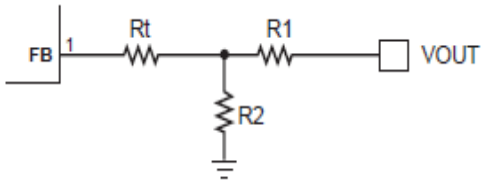
If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Application Information

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Typical Application on page 1). Choose R1 to be around 49.9kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{FB}} - 1}$$



Selecting the Inductor

A 1μH to 10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔIL is the inductor ripple current. Choose inductor ripple current to be approximately 30% if the maximum load current, 2A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MT2482 can be optimized for a wide range of capacitance and ESR values.

PCB Layout Guide

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines and take Figure 4 to Figure 5 for reference.

1) Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.

2) Bypass ceramic capacitors are suggested to be put close to the Vin Pin.

3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.

4) VOUT, SW away from sensitive analog areas such as FB.

5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

6) An example of 2-layer PCB layout is shown in Figure 4 to Figure 5 for reference.

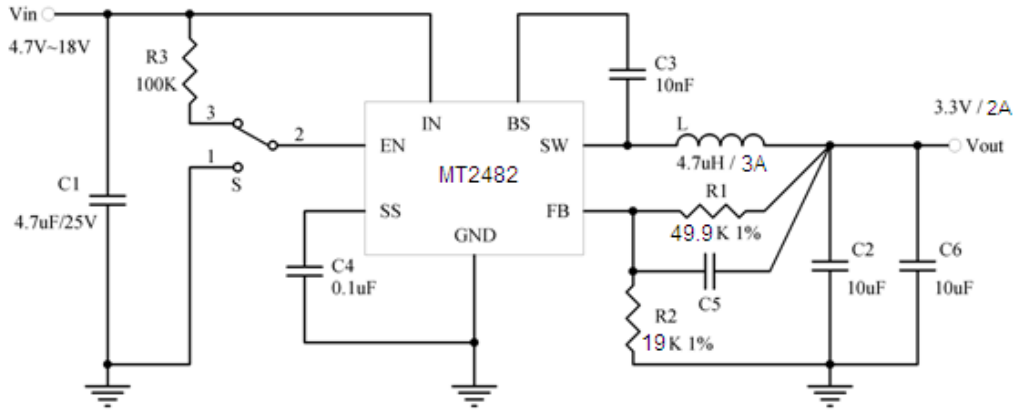


Figure 3 .Evaluation Board Schematic

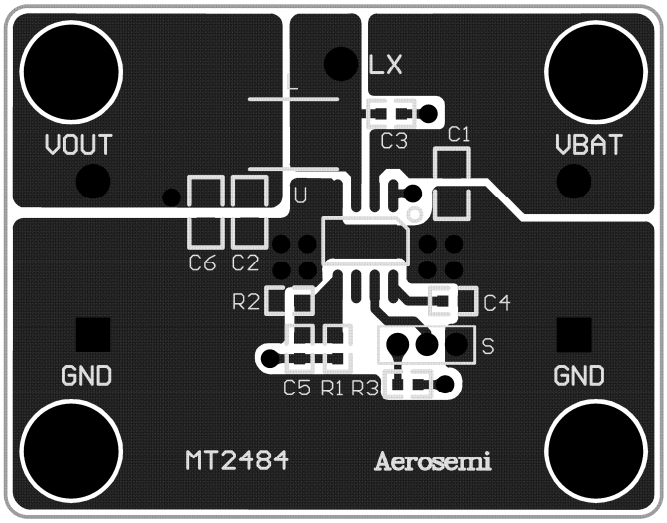


Figure 4. Evaluation Board Top Layer

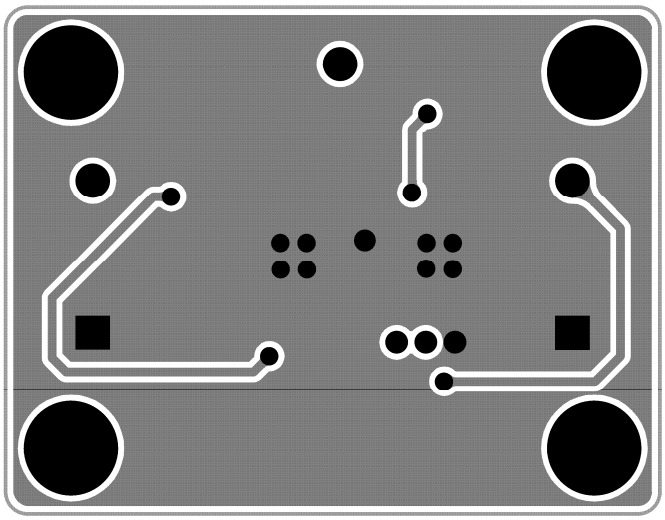
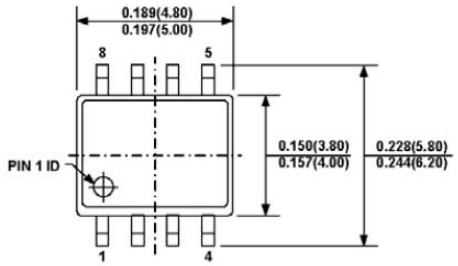
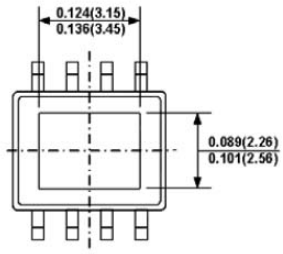


Figure 5. Evaluation Board Bottom Layer

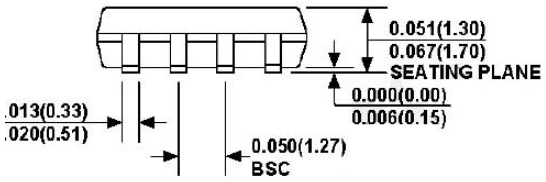
PACKAGE INFORMATION



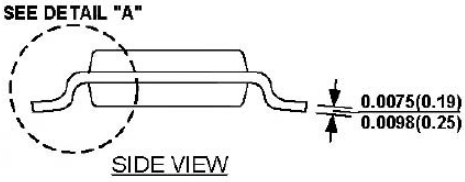
TOP VIEW



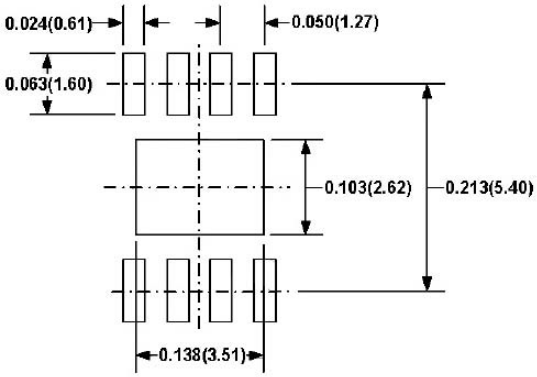
BOTTOM VIEW

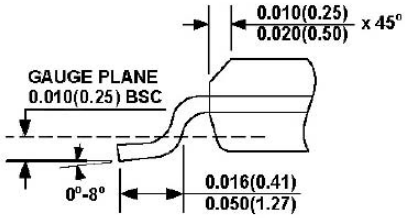


FRONT VIEW



SIDE VIEW





DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.