Product Specification

PE9311

1500 MHz Low Power UltraCMOS™ Divide-by-2 Prescaler
Rad hard for Space Applications

Product Description

The PE9311 is a high-performance static UltraCMOS™ prescaler with a fixed divide ratio of 2. Its operating frequency range is DC to 1500 MHz. The PE9311 operates on a nominal 3 V supply and draws only 6.5 mA. It is packaged in a small 8-lead ceramic SOIC and is ideal for frequency scaling and clock generation solutions.

The PE9311 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- Rad hard for Space Applications
- DC to 1500 MHz operation
- Fixed divide ratio of 2
- Low-power operation: 6.5 mA typical @ 3 V
- Ultra small package: 8-lead Ceramic SOIC
- Guaranteed 100 Krads(Si) Total Dose Performance
- Superior Single Event Upset Immunity

Figure 1. Functional Diagram

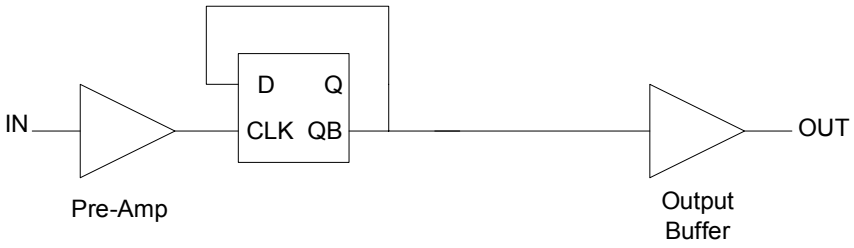

Figure 2. Package Type

8-lead CSOIC

Table 1. Electrical Specifications ($Z_S = Z_L = 50\ \Omega$)

V_{DD} = 3.0 V, -40° C ≤ T_A ≤ 85° C, unless otherwise specified

Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Voltage		2.85	3.0	3.15	V
Supply Current			6.5	11	mA
Input Frequency (F_{in})		DC		1500	MHz
Input Power (P_{in})	DC < Fin • 1000 MHz	-8		+10	dBm
	1000 < Fin • 1500 MHz	0		+10	dBm
Output Power (P_{out})	DC < Fin • 1500 MHz	0			dBm

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Figure 3. Pin Configuration

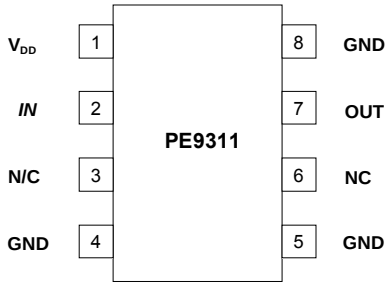

Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V_{DD}	Power supply pin. Bypassing is required (eg 1000 pF & 100 pF).
2	IN	Input signal pin. Should be coupled with a capacitor (eg 1000 pF).
3	NC	No connection. This pin should be left open.
4	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance.
5	GND	Ground pin.
6	NC	No connection. This pin should be left open.
7	OUT	Divided frequency output pin. This pin should be coupled with a capacitor (eg 1000 pF).
8	GND	Ground Pin.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage		4.0	V
Pin	Input Power		15	dBm
V_{IN}	Voltage on input	-0.3	V_{DD} +0.3	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
V_{ESD}	ESD voltage (Human Body Model, MIL-STD 883)		1000	V

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Device Functional Considerations

The *PE9311* divides an input signal, up to a frequency of 1500 MHz, by a factor of two thereby producing an output frequency at half the input frequency. To work properly at higher frequency, the input and output signals (pins 2 & 7) must be AC coupled via an external capacitor, as shown in the test circuit in Figure 7. The input may be DC coupled for low frequency operation with care taken to remain within the specified DC input range for the device.

The ground pattern on the board should be made as wide as possible to minimize ground impedance. See Figure 8 for a layout example.

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Typical Performance Data: V_{DD} = 3.0 V

Figure 4. Input Sensitivity

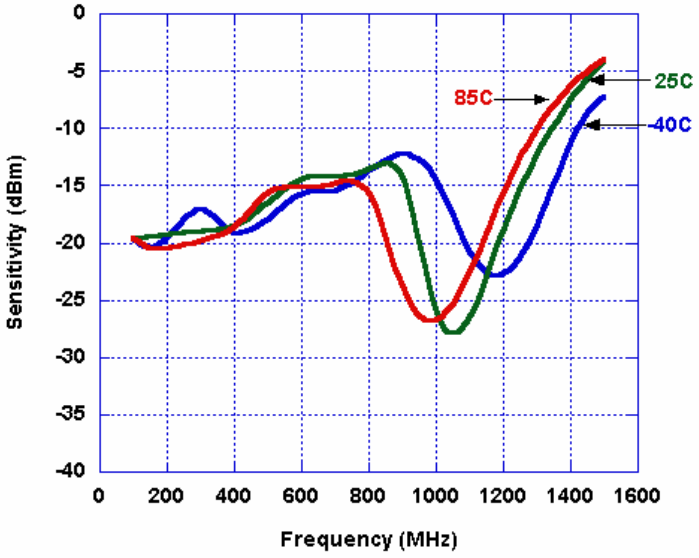

Figure 5. Device Current

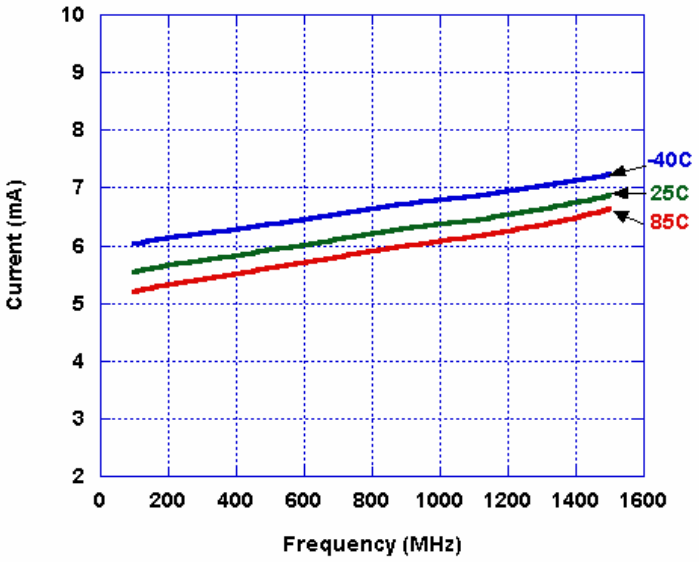

Figure 6. Output Power

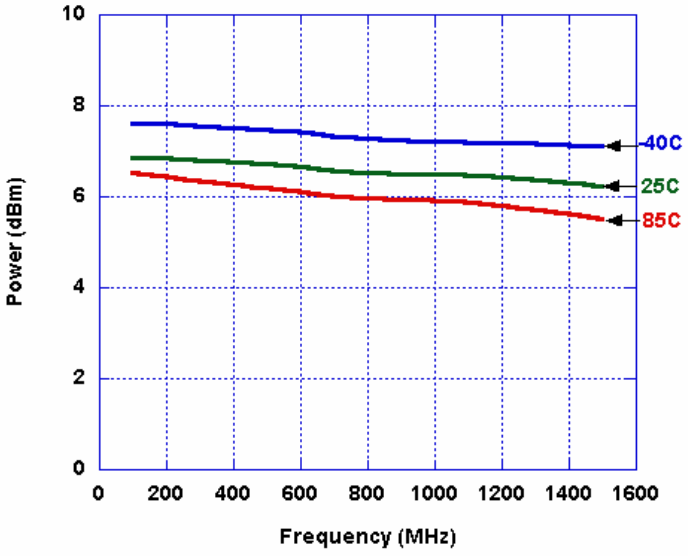

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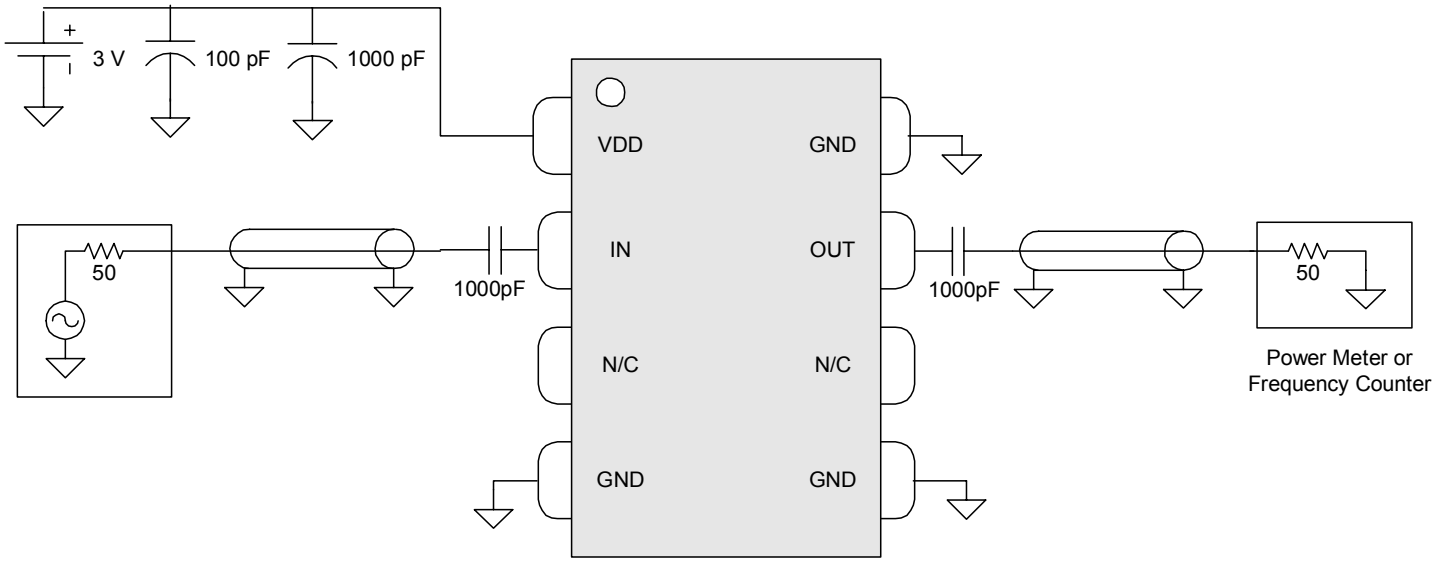
Figure 7. Test Circuit Block Diagram



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Evaluation Kit Operation

The Ceramic SOIC Prescaler Evaluation Board was designed to help customers evaluate the *PE9311* divide-by-2 prescaler. On this board, the device input (pin 2) is connected to the SMA connector J1 through a 50 Ω transmission line. A series capacitor (C3) provides the necessary DC block for the device input. A value of 1000 pF was used for the evaluation board; other applications may require a different value. It is also possible to place a 0 Ω resistor in this location for very low frequency applications.

The device output (pin 7) is connected to SMA connector J3 through a 50 Ω transmission line. A series capacitor (C1) provides the necessary DC block for the device output. This capacitor value must be chosen to have a low impedance at the desired output frequency of the device. A value of 1000 pF was chosen for the evaluation board.

The board is constructed of a two-layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide above ground plane model with trace width of 0.030", trace gaps of 0.0061", dielectric thickness of 0.028", metal thickness of 0.0014", and ε_r of 4.6. Note that the predominate mode of these transmission lines is coplanar waveguide.

J2 provides DC power to the device via pin 1. Two decoupling capacitors (C2=100 pF, C10=1000 pF) are included on this trace. It is the responsibility of the customer to determine proper supply decoupling for their design application.

Figure 8. Evaluation Board Layout
Peregrine specification 102/0034

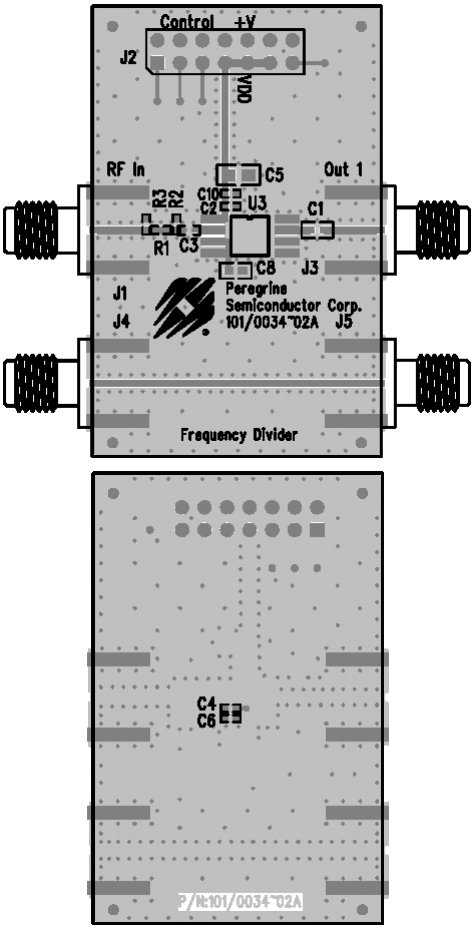

Figure 9. Evaluation Board Schematic
Peregrine specification 102/0202

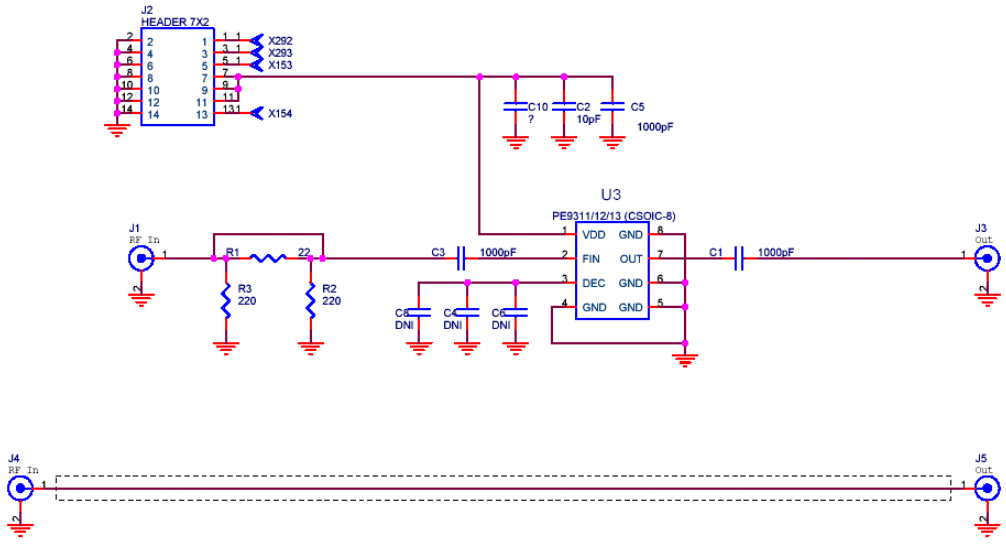

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Figure 10. Package Drawing
8-lead CSOIC

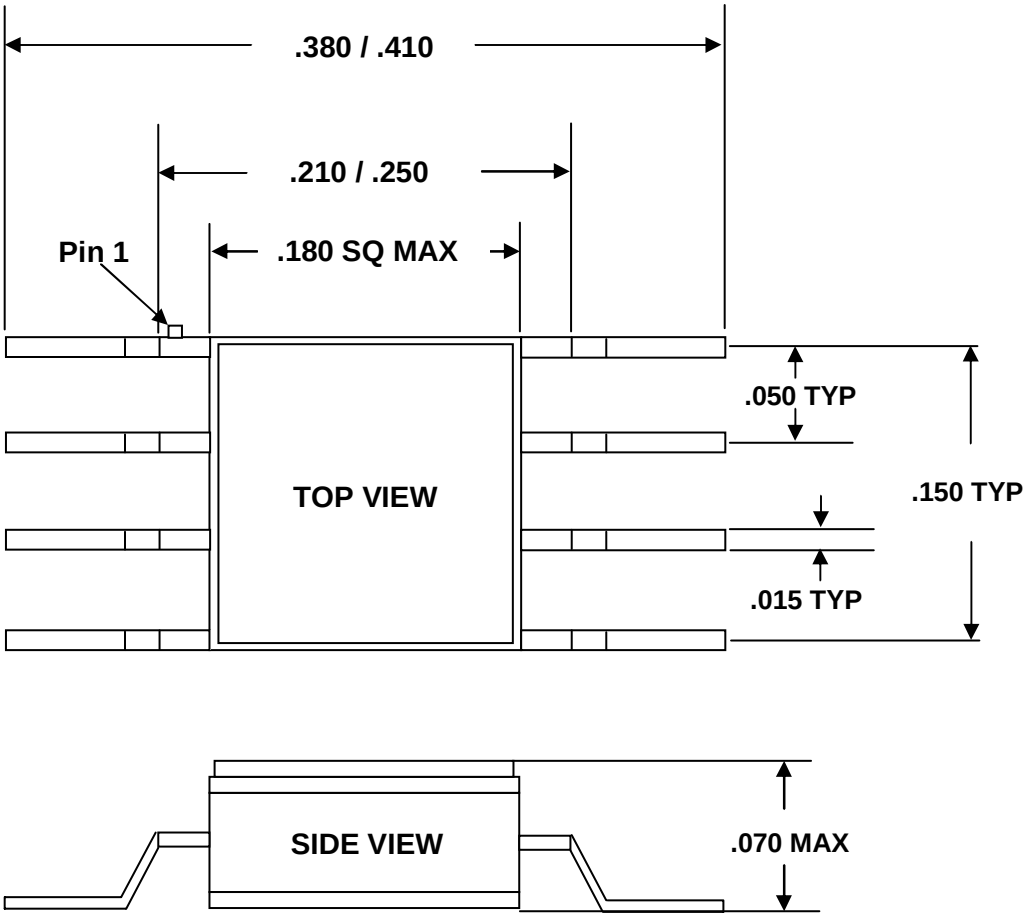

Table 4. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
9311-01	PE9311	PE9311-08CFPG-B Engineering Samples	Gullwing Glass Flatpack	50 / Tray
9311-11	PE9311	PE9311-08CFPG-B Production Units	Gullwing Glass Flatpack	50 / Tray
9311-00	PE9311-EK	PE9311 Evaluation Kit	Evaluation Kit	1 / Box

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Data Sheet Identification

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