SONY

CXA2647N

RF Signal Processor for CD Players

Description

The CXA2647N is an RF signal processing IC for compact disc players.

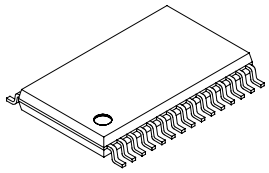
Features

- RF signal processor supporting 6× speed CD
- RF system VCA circuit
- RF system equalizer
- Supports pickups with built-in RF summing amplifier
- Low current consumption mode (RF off mode)
- ROM/RW switching mode
- Center error amplifier
- Output DC level shift circuit
- TE balance adjustment function

Functions

- RF AC summing amplifier, equalizer, VCA
- RF DC summing amplifier
- Focus error amplifier
- Tracking error amplifier
- Center error amplifier
- Automatic power control
- VC buffer amplifier (analog block, digital block)

30 pin SSOP (Plastic)



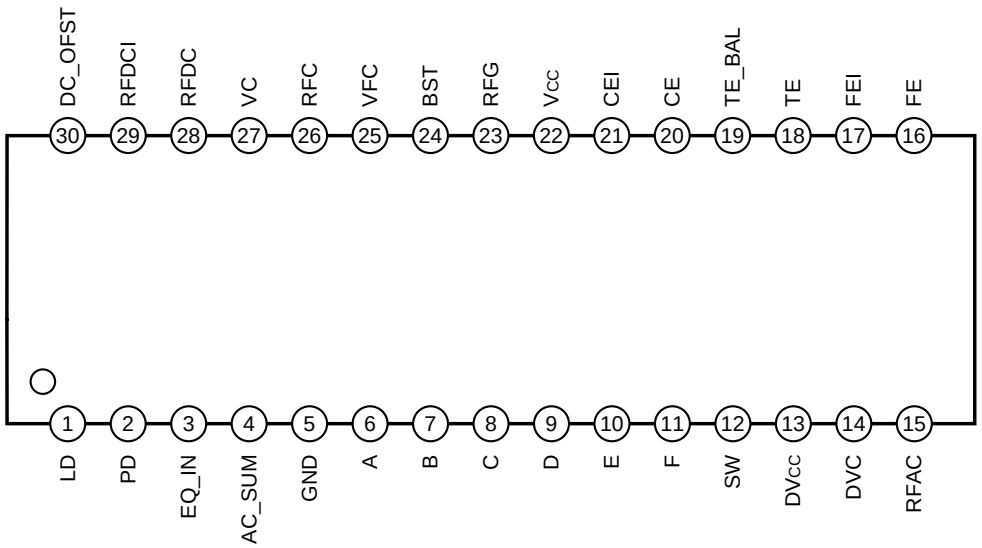
Absolute Maximum Ratings

• Supply voltage	V_{CC}	7	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	620	mW

Operating Conditions

• Operating supply voltage range			
	V_{CC} – GND	3.0 to 3.6	V
	DV_{CC} – GND	3.0 to 3.6	V
		(0V ≤ V_{CC} – DV_{CC} < 2V)	
• Operating temperature	Topr	–30 to +85	°C

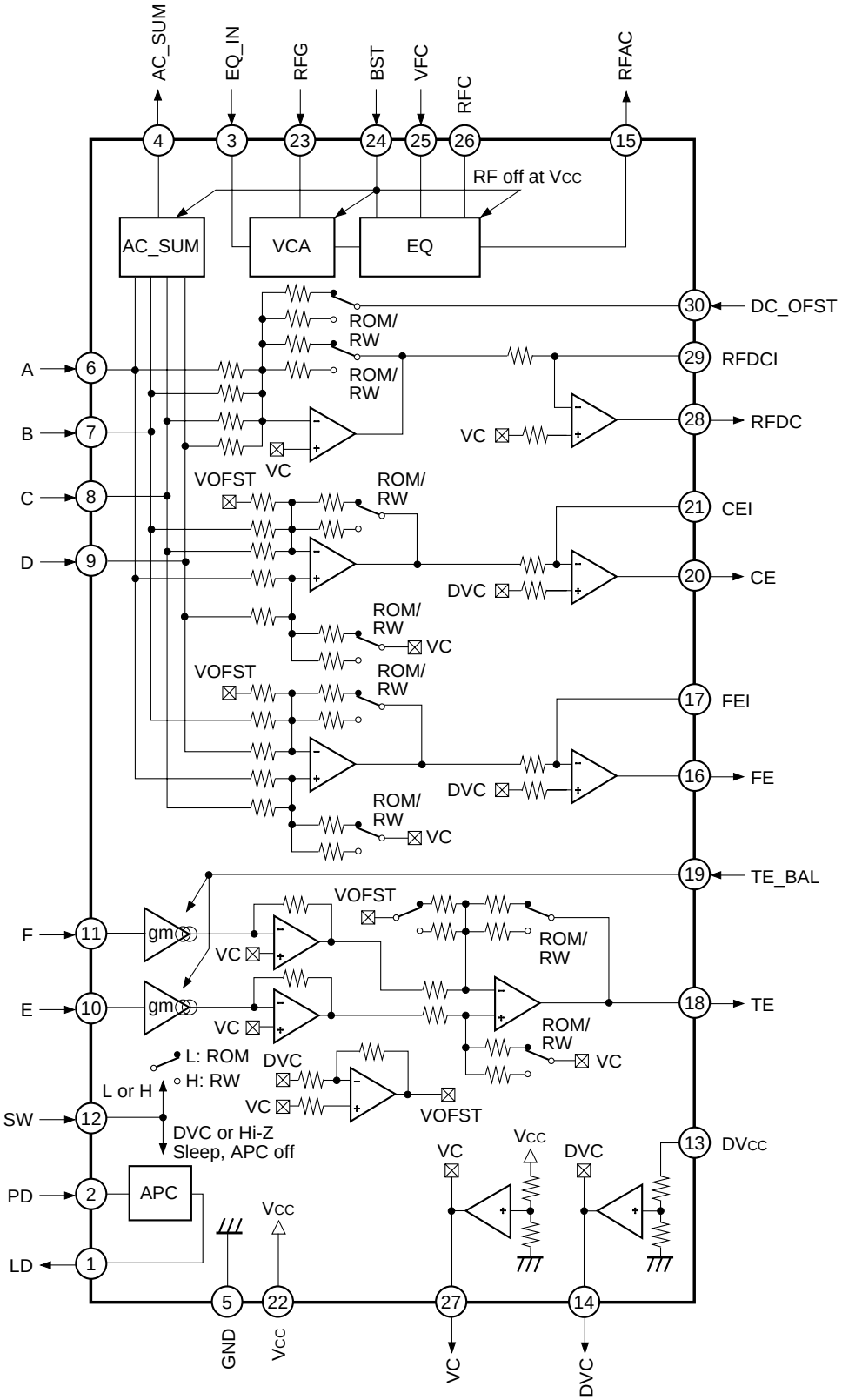
Pin Configuration



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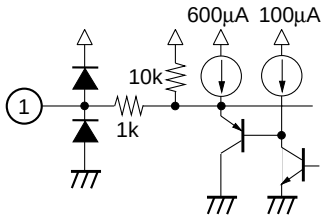
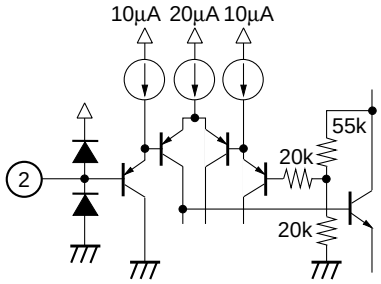
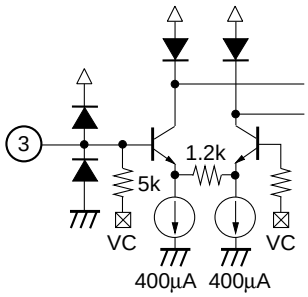
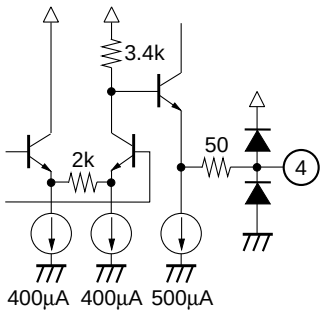
Block Diagram

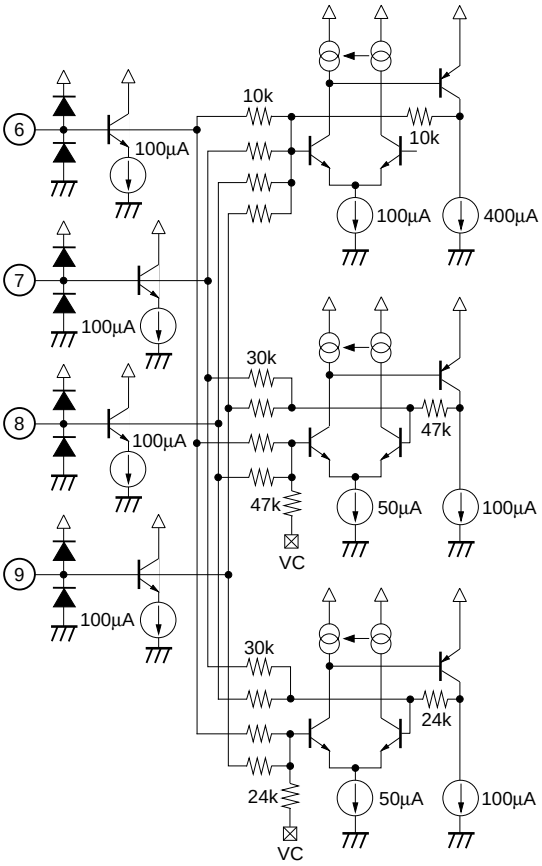
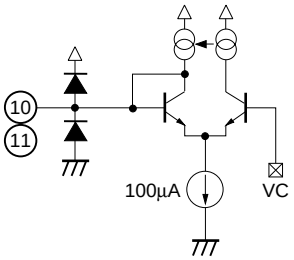
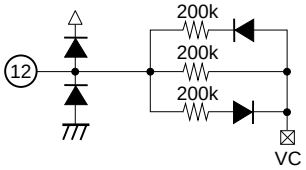
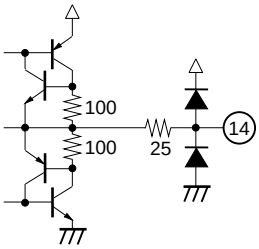


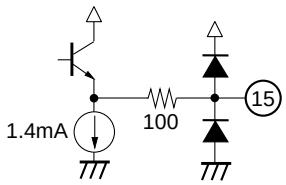
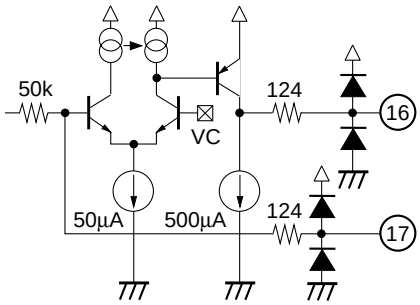
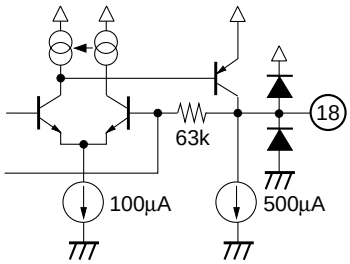
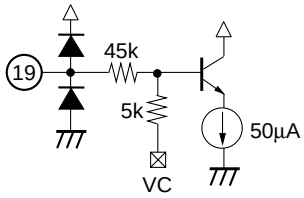
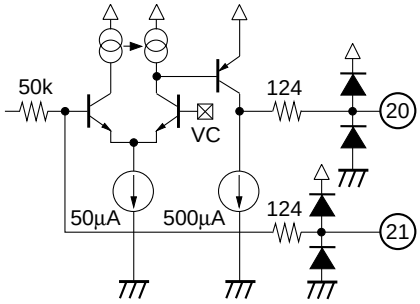
Pin Description

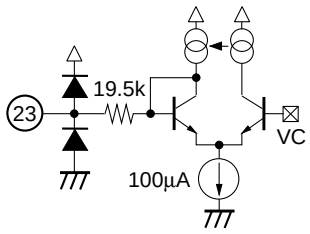
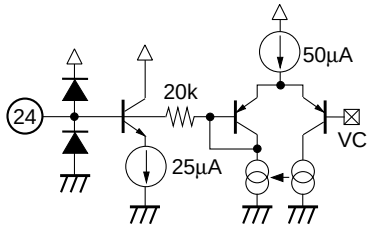
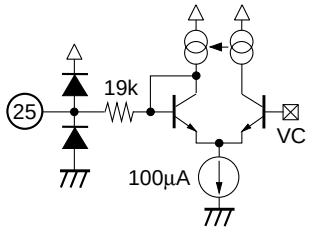
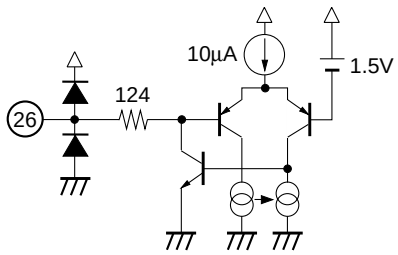
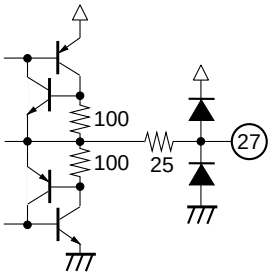
Pin No.	Symbol	I/O	Description
1	LD	O	APC amplifier output.
2	PD	I	APC amplifier input.
3	EQ_IN	I	RFAC system VCA block and EQ block input.
4	AC_SUM	O	RFAC system RF_SUM output.
5	GND	I	GND.
6	A	I	Signal A input.
7	B	I	Signal B input.
8	C	I	Signal C input.
9	D	I	Signal D input.
10	E	I	Signal E input.
11	F	I	Signal F input.
12	SW	I	Mode switching signal input.
13	DV_{CC}	I	DV_{CC}.
14	DVC	O	DVC output.
15	RFAC	O	RFAC signal output.
16	FE	O	Focus error signal output.
17	FEI	I	FE amplifier virtual ground.
18	TE	O	Tracking error signal output.
19	TE_BAL	I	TE balance adjustment.
20	CE	O	Center error signal output.
21	CEI	I	CE amplifier virtual ground.
22	V_{CC}	I	V_{CC}.
23	RFG	I	RFAC system VCA block low frequency gain adjustment.
24	BST	I	EQ boost level adjustment.
25	VFC	I	EQ cut-off frequency adjustment.
26	RFC	I	EQ cut-off frequency adjustment.
27	VC	O	VC voltage output.
28	RFDC	O	RFDC signal output.
29	RFDCI	I	RFDC amplifier virtual ground.
30	DC_OFST	I	RFDC signal output offset adjustment.

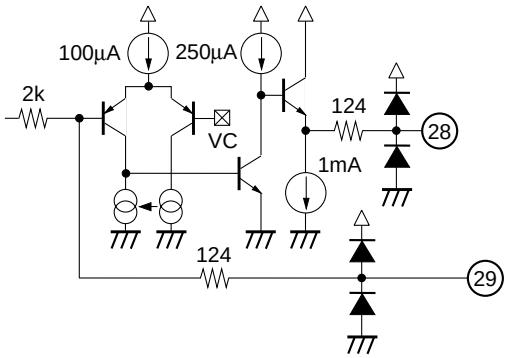
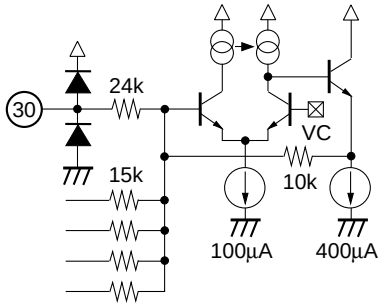
Pin Description

Pin No.	Symbol	I/O	Equivalent circuit	Description
1	LD	O		APC amplifier output.
2	PD	I		APC amplifier input.
3	EQ_IN	I		Equalizer circuit input.
4	AC_SUM	O		RFAC summing amplifier output.
5	GND	—	—	GND.

Pin No.	Symbol	I/O	Equivalent circuit	Description
6	A	I		RFAC summing amplifier, RFDC amplifier, focus error amplifier and center error amplifier input.
7	B	I		
8	C	I		
9	D	I		
10	E	I		Tracking error amplifier input.
11	F	I		
12	SW	I		CD-ROM/SLEEP/CD-RW switching input. ROM when connected to GND, RW when connected to DVCC, SLEEP mode when connected to DVC or Hi-Z.
13	DVCC	—	—	Digital power supply.
14	DVC	O		(DVCC + GND)/2 voltage output.

Pin No.	Symbol	I/O	Equivalent circuit	Description
15	RFAC	O		RFAC amplifier output.
16	FE	O		Focus error amplifier output.
17	FEI	I		Focus error amplifier gain adjustment. The gain is adjusted by the external resistance value connected between this pin and Pin 16.
18	TE	O		Tracking error amplifier output.
19	TE_BAL	I		Input for adjusting the tracking error amplifiers E and F gain balance with the control voltage.
20	CE	O		Center error amplifier output.
21	CEI	I		Center error amplifier gain adjustment. The gain is adjusted by the external resistance value connected between this pin and Pin 20.

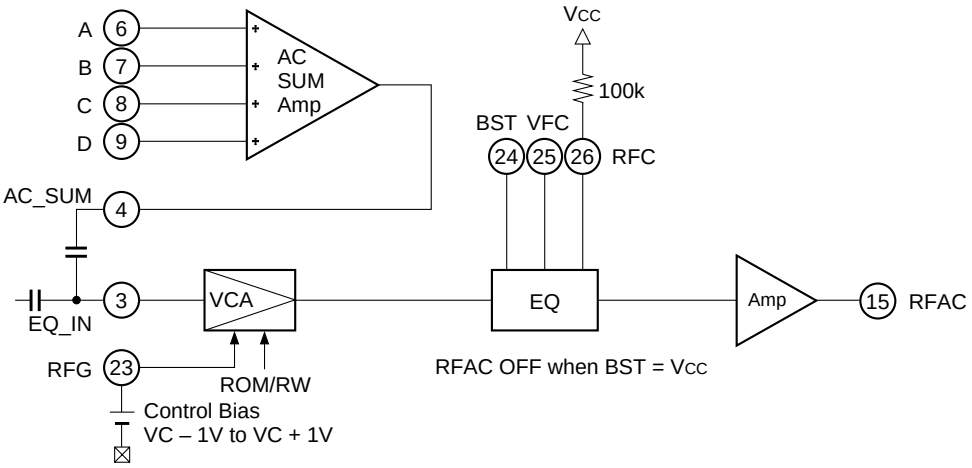
Pin No.	Symbol	I/O	Equivalent circuit	Description
22	V_{CC}	—	—	V_{CC}.
23	RFG	I		Input for setting the RFAC low frequency gain with the control voltage.
24	BST	I		Input for adjusting the equalizer circuit boost level with the control voltage.
25	VFC	I		Input for adjusting the equalizer circuit cut-off frequency with the control voltage.
26	RFC	I		Input for adjusting the equalizer circuit cut-off frequency with the external resistance.
27	VC	O		(V_{CC} + GND)/2 voltage output.

Pin No.	Symbol	I/O	Equivalent circuit	Description
28	RFDC	O		RFDC amplifier output.
29	RFDCI	I		RFDC amplifier gain adjustment. The gain is adjusted by the external resistance value connected between this pin and Pin 28.
30	DC_OFST	I		Input for adjusting RFDC amplifier offset with the control voltage.

Description of Functions

• RFAC

The RF signal input by connecting capacitance to EQ_IN (Pin 3) is equalized, arithmetically amplified and then output from RFAC (Pin 15).

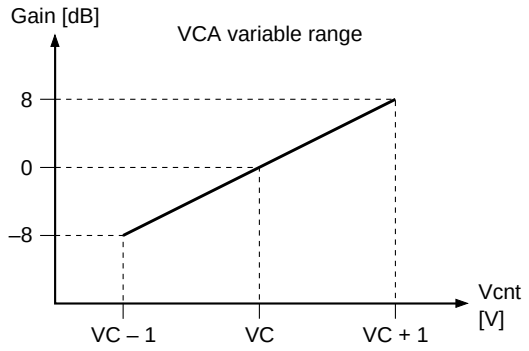


Low frequency gain (100kHz)
AC_SUM (ABCD to AC_SUM) 13dB
RFAC (EQ_IN to RFAC) ROM: 1.5dB
RW: 13.5dB

When BST (Pin 24) is connected to V_{CC}, the RFAC function is turned off and the low consumption mode is entered.

If RF (summing signal) is present at the pickup output pin, input the addition output signal to EQ_IN (Pin 3) coupled by capacitance.
When using a pickup without a summing output function, perform addition with the AC_SUM and then input the signal to EQ_IN (Pin 3) coupled by capacitance.
ROM/RW switching is done by the VCA block, so either input method can be used without problem.
The RW gain is 12dB higher than the ROM gain.

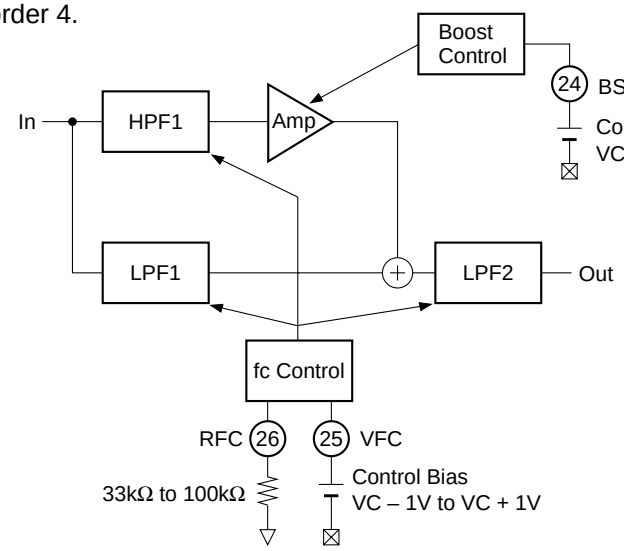
The VCA low frequency gain can be adjusted by the RFG (Pin 23) voltage control.
The control voltage vs. low frequency gain characteristics are shown in the graph to the right.



The RFAC pin (Pin 15) is an NPN transistor emitter follower output.
The maximum drive current is approximately 1.4mA.
If the load capacitance distorts the output waveform, connect resistance between the RFAC pin and GND to increase the drive current.

• **EQ**

The EQ internal block diagram is shown below. The EQ is configured with the filter of the Bessel function of order 4.



$$LPF1 = \frac{79.517fc^2}{S^2 + (17.085fc)\,S + 79.517fc^2}$$

$$HPF1 = \frac{S^2}{S^2 + (17.085fc)\,S + 79.517fc^2}$$

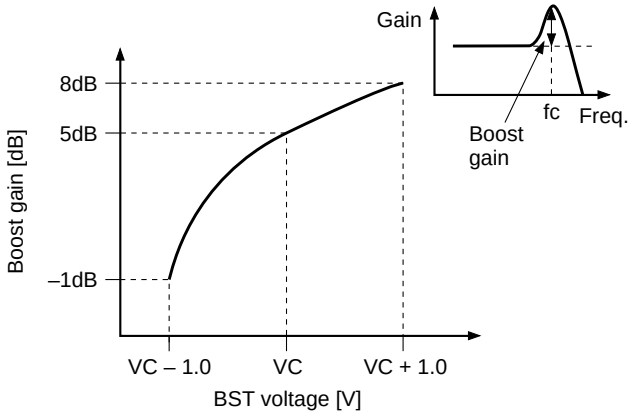
$$LPF2 = \frac{99.963fc^2}{S^2 + (12.412fc)\,S + 99.963fc^2}$$

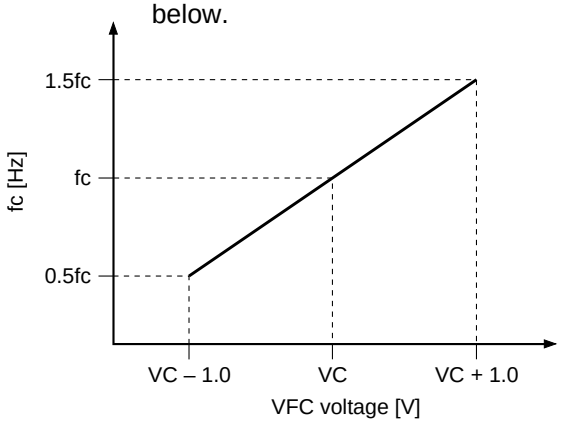
The boost gain can be adjusted by adjusting the HPF1 gain.
The cut-off frequency is adjusted by the RFC external resistance value and the VFC control voltage value.

RFC resistance value: The cut-off frequency fc of each filter is adjusted by the Pin 26 external resistance value.
The VFC voltage can be varied using this fc as the reference.

VFC voltage: fc can be adjusted by the voltage applied to Pin 25. The cut-off frequency control characteristics are shown in the graph below.

The boost gain can be adjusted by the BST (Pin 24) control voltage.
The control characteristics are shown in the graph below.
The boost gain stands for the increased gain from the low frequency gain in the fc frequency.

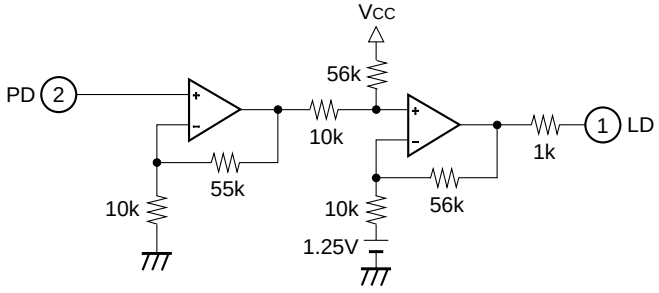




RFC pin external resistor value 100kΩ: fc = 1.6MHz
33kΩ: fc = 4.8MHz

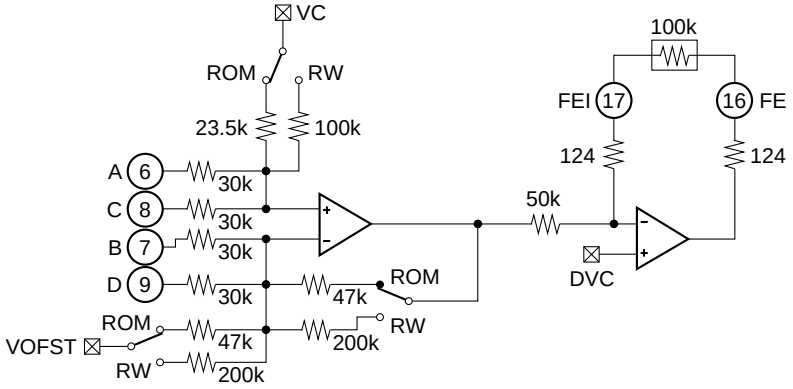
• **APC (Automatic Power Control)**

When the laser diode is driven by a constant current, the optical power output has extremely large negative temperature characteristics. Therefore, the current must be controlled to maintain the monitor photodiode output at a constant level. This control is performed by the APC function.



• **Focus Error**

The signals input to the A and C pins and the B and D pins are arithmetically amplified and the focus error signal is output.
This circuit has ROM/RW switching and offset addition functions.

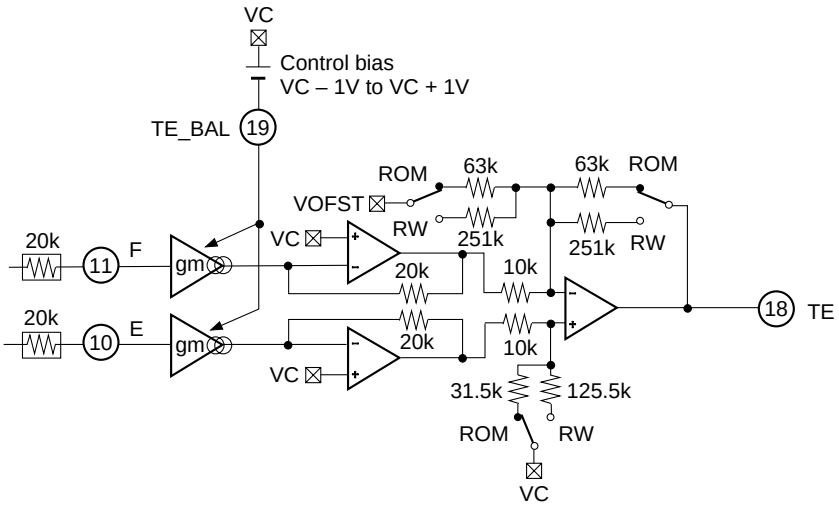


FE = Gain { (B + D) – (A + C) }
Low frequency gain ROM: 15.5dB
RW: 27.5dB

Cut-off frequency fc (typ.) ROM: 400kHz
RW: 300kHz

• **Tracking Error**

The signals input to the E and F pins are arithmetically amplified and the tracking error signal is output.
This circuit has ROM/RW switching and offset addition functions.



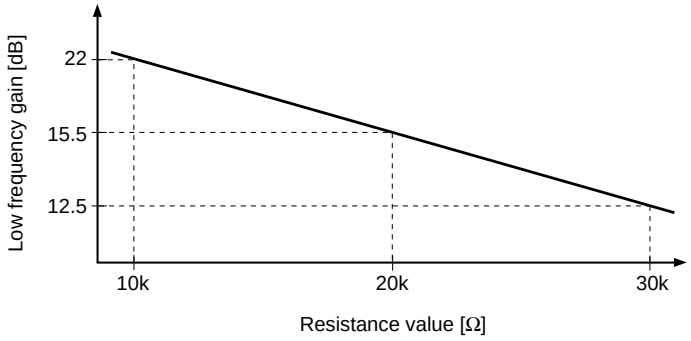
TE = Gain (F – E)

Low frequency gain ROM: 16dB
RW: 28dB

TE balance adjustment
(F – E) low frequency gain = ±6dB

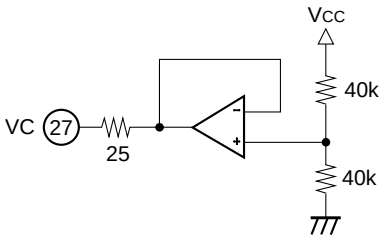
Cut-off frequency fc (typ.)
ROM: 200kHz
RW: 150kHz

External resistance value vs. Low frequency gain for E and F input pins



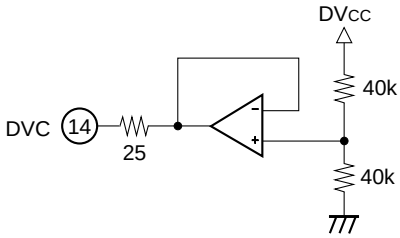
• VC Buffer

This outputs the VC ((1/2) Vcc) voltage.
The maximum output current is approximately ±3mA.
Use this voltage as the analog block VC voltage.



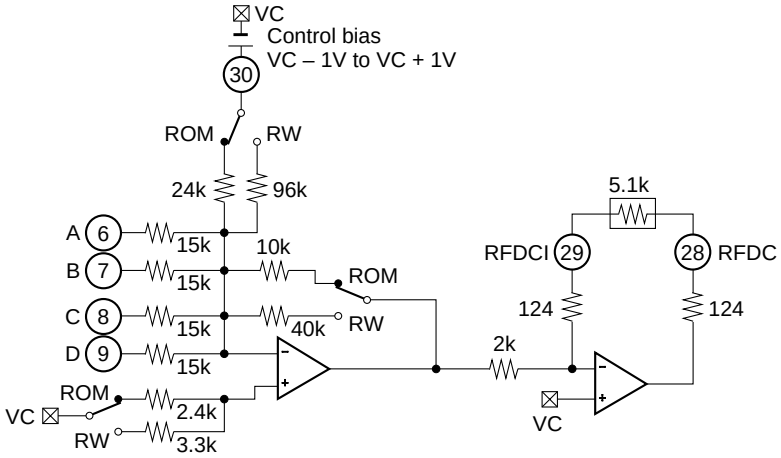
• DVC Buffer

This outputs the DVC ((1/2) DVcc) voltage.
The maximum output current is approximately ±3mA.
Use this voltage as the digital block VC voltage.
The each output DC voltage of FE, TE and CE is level shifted using the DVC voltage as the reference.



• RFDC

The signals input to the A, B, C and D pins are added, amplified and the RFDC signal is output. ROM/RW switching, low frequency gain adjustment and output DC voltage adjustment are possible.



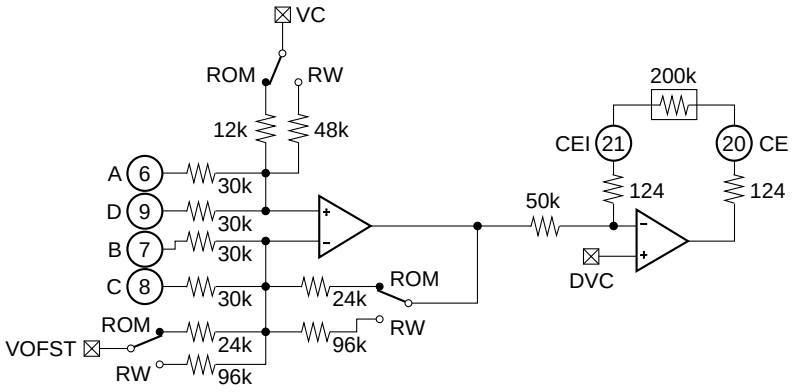
RFDC = Gain (A + B + C + D)
Low frequency gain ROM: 16.5dB
RW: 28.5dB

Cut-off frequency fc (typ.)
ROM : 15MHz
RW : 6MHz

The gain can be adjusted by the external resistance connected between Pins 28 and 29.
The output voltage offset can be adjusted by controlling the Pin 30 voltage.

• Center Error

The signals input to the A and D pins and the B and C pins are arithmetically amplified and the center error signal is output.
ROM/RW switching and offset addition functions are incorporated.

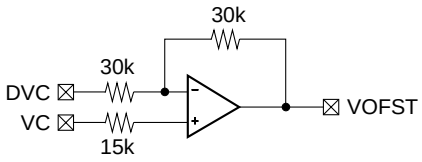


CE = Gain {(B + C) – (A + D)} signal is arithmetically amplified.
Low frequency gain ROM: 15.5dB
RW: 27.5dB

Cut-off frequency fc (typ.)
ROM: 200kHz
RW: 200kHz

• Output DC Level Shift

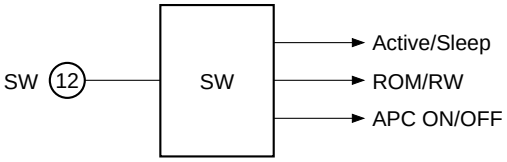
The FE, TE and CE output DC voltages are level shifted to the digital VC voltage (DVC).
The reference voltage of this IC is the VC voltage, and only the output reference voltage changes.
The maximum output voltage of each output signal should be kept to the digital V_{CC} voltage (DV_{CC}) or less in order to protect the DSP IC.



The VC and DVC voltages are arithmetically amplified and output as the VOFST voltage.
The VOFST voltage serves as the level shift reference voltage, and is distributed to each block.
VOFST = 2VC –DVC

• SW

This controls the laser (APC) on/off, active/sleep mode, and ROM/RW mode switching.
Switching is controlled by the voltage applied to the SW pin.



SW low/high condition
Low: GND to DVC – 1.2V
High: DVC + 1.2V to Vcc

Status of Functions on SW Switching

Item / Control voltage	APC	Active/Sleep	ROM/RW
V_{CC}	ON	Active	RW
VC or Hi-Z	OFF	Sleep	—
GND	ON	Active	ROM

The VC buffer is always in active mode even if it enters sleep mode.
In the function block, MODE SW is always set to active mode.

Electrical Characteristics

(V_{CC} = 1.5V, V_{EE} = –1.5V, DV_{CC} = 1.5V, DV_{EE} = –1.5V)

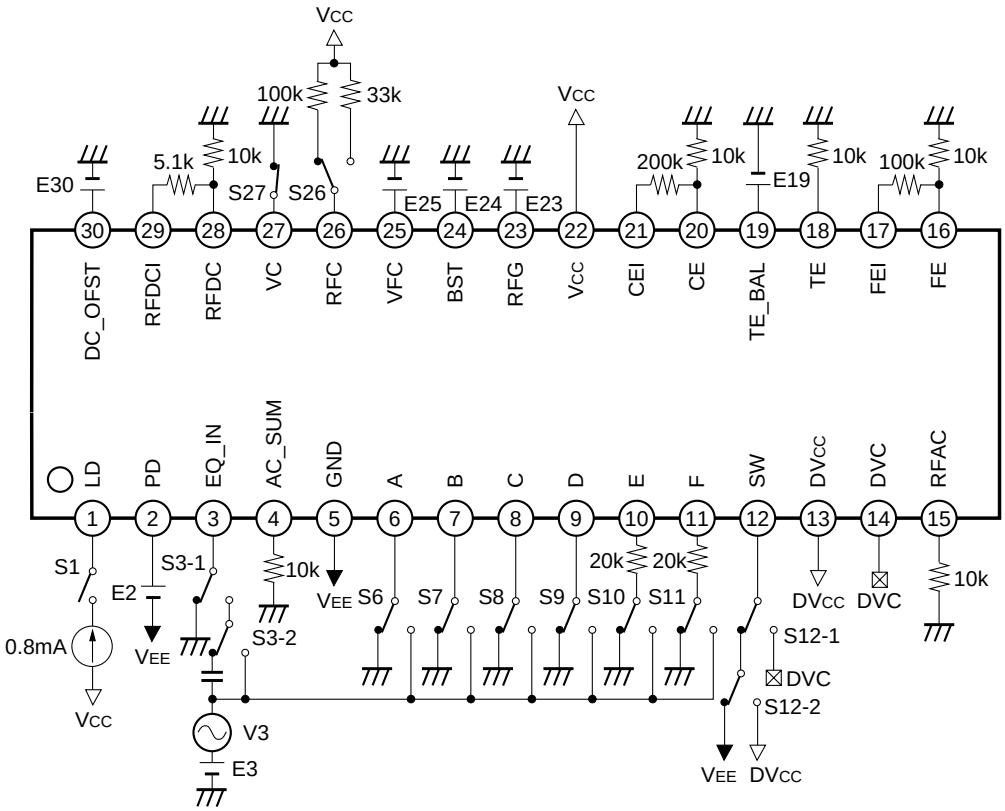
Measurement No.	Function	Measurement item	Symbol	Switch conditions													Bias conditions										Measurement pin	Measurement conditions	Min.	Typ.	Max.	Unit
				S1	S3-1	S3-2	S6	S7	S8	S9	S10	S11	S12-1	S12-2	S26	S27	V3 amplitude	V3 frequency	E2	E3	E19	E23	E24	E25	E30						
1		Current consumption (Active, RF On)	Icc_ARFon																0V	0V	0V	0V	0V	0V	0V	22	Pin current	18	30	42	mA
2		Current consumption (Active, RF Off)	Icc_ARFoff																				1.5V			22	Pin current	7	12	17	mA
3		Current consumption (DV_{CC})	Icc_Dvcc																				0V			13	Pin current	0.2	0.7	1.2	mA
4		Current consumption (Sleep)	Icc_Slp										O													22	Pin current	1.8	3	4.2	mA
5	RFAC SUM	SUM offset voltage	ACSUM_Ofst																							4	Pin voltage	–0.95	–0.55	–0.15	V
6		SUM low frequency gain	Gsum				O	O	O	O							0.1Vp-p	100kHz								4	20 log (Vout/Vin)	11	13	15	dB
7		SUM frequency response	Fsum				O	O	O	O							0.1Vp-p	10MHz		↓						4	20 log (Vout/Vin) – Gsum	–2.5	–0.5	0.5	dB
8		SUM maximum output voltage H	Vsum_H				O	O	O	O										0.35V						4	Pin voltage – ACSUM_Ofst	1.15	1.35	1.55	V
9		SUM maximum output voltage L	Vsum_L				O	O	O	O										–0.15V						4	Pin voltage – ACSUM_Ofst	–0.55	–0.35	–0.15	V
10	RFAC EQ	Offset voltage ROM	AC_OfstROM																	0V						15	Pin voltage	–0.45	–0.05	0.35	V
11		Offset voltage RW	AC_OfstRW											O								↓				15	Pin voltage	–0.45	–0.05	0.35	V
12		Low frequency gain ROM_min	Gac_ROM1		O												1.4Vp-p	100kHz				–1.0V				15	20 log (Vout/Vin) – Gac_ROM2	–10	–8	–6	dB
13		Low frequency gain ROM_cnt	Gac_ROM2		O												0.8Vp-p	100kHz				0V				15	20 log (Vout/Vin)	–2	1.5	5	dB
14		Low frequency gain ROM_max	Gac_ROM3		O												0.3Vp-p	100kHz				1.0V				15	20 log (Vout/Vin) – Gac_ROM2	6	8	10	dB
15		Low frequency gain RW_min	Gac_RW1		O									O			0.35Vp-p	100kHz				–1.0V				15	20 log (Vout/Vin) – Gac_RW2 – Gac_ROM2	–10	–8	–6	dB
16		Low frequency gain RW_cnt	Gac_RW2		O									O			0.2Vp-p	100kHz				0V				15	20 log (Vout/Vin) – Gac_ROM2	10	12	14	dB
17		Low frequency gain RW_max	Gac_RW3		O									O			75mVp-p	100kHz				1.0V		↓		15	20 log (Vout/Vin) – Gac_RW2 – Gac_ROM2	6	8	10	dB
18		Low frequency gain RF_HiFc	Gac_HiFc		O										O		0.8Vp-p	100kHz				0V		1.0V		15	20 log (Vout/Vin)	–2	1.5	5	dB
19		Frequency response Min_L	Fac_MinL		O												0.4Vp-p	800kHz				↓		–1.0V		15	20 log (Vout/Vin) – Gac_ROM2	3	5	7	dB
20		Frequency response Min_H	Fac_MinH		O												0.4Vp-p	2.4MHz						1.0V		15	20 log (Vout/Vin) – Gac_ROM2	3	5	7	dB
21		Frequency response RF_HiFc	Fac_HiFcf		O										O		0.4Vp-p	7.2MHz					↓	1.0V		15	20 log (Vout/Vin) – Gac_HiFc	3	5	7	dB
22		Boost response BST_H	Fac_BSTH		O									O			70mVp-p	1.6MHz					1.0V	0V		15	20 log (Vout/Vin) – Gac_RW2 – Gac_ROM2	6.5	8.5	10.5	dB
23		Boost response BST_L	Fac_BSTL		O									O			0.2Vp-p	1.6MHz		↓			–1.0V			15	20 log (Vout/Vin) – Gac_RW2 – Gac_ROM2	–2.5	–0.5	1.5	dB
24		Maximum output voltage H	Vac_H		O	O														0.85V			0V			15	Pin voltage – AC_OfstROM	0.65	0.85	1.05	V
25		Maximum output voltage L	Vac_L		O	O													↓	–0.85V	↓	↓	↓	↓	↓	15	Pin voltage – AC_OfstROM	–0.95	–0.75	–0.55	V

Measure-ment No.	Func-tion	Measurement item	Symbol	Switch conditions													Bias conditions										Measure-ment pin	Measurement conditions	Min.	Typ.	Max.	Unit
				S1	S3-1	S3-2	S6	S7	S8	S9	S10	S11	S12-1	S12-2	S26	S27	V3 amplitude	V3 frequency	E2	E3	E19	E23	E24	E25	E30							
26	RFDC	Offset voltage ROM	DC_OfstROM																0V	0V	0V	0V	0V	0V	0V	28	Pin voltage	–120	0	120	mV
27		Offset voltage RW	DC_OfstRW											O												28	Pin voltage	–120	0	120	mV
28		Low frequency gain ROM	Gdc_ROM				O	O	O	O							50mVp-p	100kHz								28	20 log (Vout/Vin)	13.5	16.5	19.5	dB
29		Low frequency gain RW	Gdc_RW				O	O	O	O				O			12.5mVp-p	100kHz								28	20 log (Vout/Vin) – Gdc_ROM	11	12	13	dB
30		Frequency response ROM	Fdc_ROM				O	O	O	O							50mVp-p	10MHz								28	20 log (Vout/Vin) – Gdc_ROM	–3	–0.5	0.5	dB
31		Frequency response RW	Fdc_RW				O	O	O	O				O			12.5mVp-p	3MHz		↓						28	20 log (Vout/Vin) – Gdc_RW _Gdc_ROM	–3	–0.5	0.5	dB
32		Maximum output voltage H	Vdc_H				O	O	O	O										0.13V						28	Pin voltage	0.35	0.55	0.75	V
33		Maximum output voltage L	Vdc_L				O	O	O	O										–0.25V					↓	28	Pin voltage	–1.5	–1.3	–1.1	V
34		Offset voltage 1	DC_Ofst1																	0V					–0.5V	28	Pin voltage	–0.67	–0.55	–0.43	V
35	FE	Offset voltage ROM	FE_OfstROM																						0V	16	Pin voltage	–120	0	120	mV
36		Offset voltage RW	FE_OfstRW											O												16	Pin voltage	–120	0	120	mV
37		Low frequency gain ROM1	Gfe_ROM1				O		O								0.1Vp-p	1kHz								16	20 log (Vout/Vin)	12.5	15.5	18.5	dB
38		Low frequency gain ROM2	Gfe_ROM2					O		O							0.1Vp-p	1kHz								16	20 log (Vout/Vin)	12.5	15.5	18.5	dB
39		Low frequency gain RW1	Gfe_RW1				O		O					O			25mVp-p	1kHz								16	20 log (Vout/Vin) – Gfe_ROM1	11	12	13	dB
40		Low frequency gain RW2	Gfe_RW2					O		O				O			25mVp-p	1kHz								16	20 log (Vout/Vin) – Gfe_ROM2	11	12	13	dB
41		Frequency response ROM1	Ffe_ROM1				O		O								0.1Vp-p	200kHz								16	20 log (Vout/Vin) – Gfe_ROM1	–2.5	–0.5	0.5	dB
42		Frequency response ROM2	Ffe_ROM2					O		O							0.1Vp-p	200kHz								16	20 log (Vout/Vin) – Gfe_ROM2	–2.5	–0.5	0.5	dB
43		Frequency response RW1	Ffe_RW1				O		O					O			25mVp-p	100kHz								16	20 log (Vout/Vin) – Gfe–RW1 –Gfe_ROM1	–2.5	–0.5	0.5	dB
44		Frequency response RW2	Ffe_RW2					O		O				O			25mVp-p	100kHz		↓						16	20 log (Vout/Vin) – Gfe_RW2–Gfe_ROM2	–2.5	–0.5	0.5	dB
45		Maximum output voltage H	Vfe_H					O		O										0.18V						16	Pin voltage	0.75	1	1.45	V
46		Maximum output voltage L	Vfe_L				O		O										↓	0.18V	↓	↓	↓	↓	↓	16	Pin voltage	–1.45	–1	–0.75	V

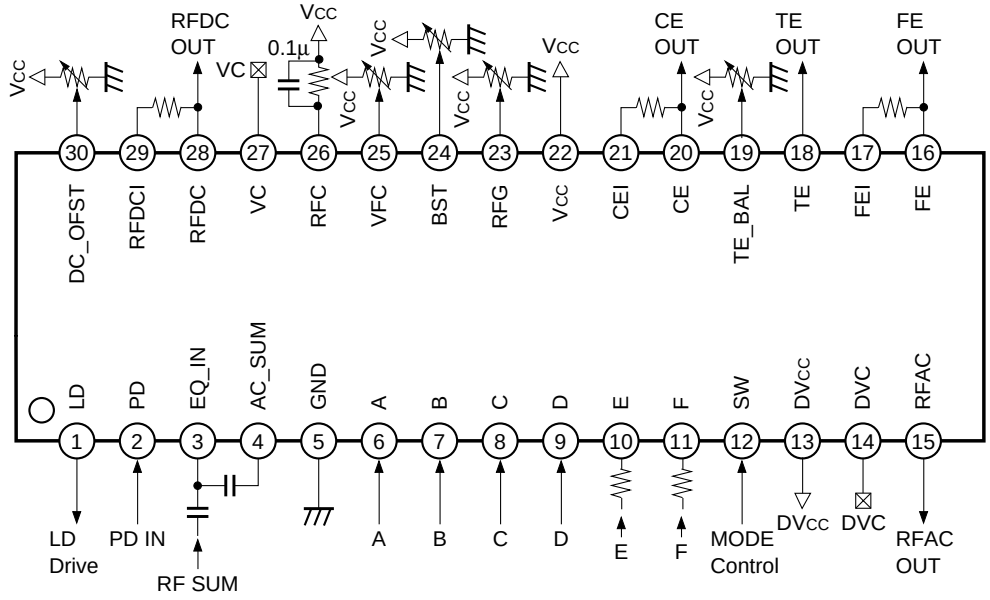
Measurement No.	Function	Measurement item	Symbol	Switch conditions												Bias conditions									Measurement pin	Measurement conditions	Min.	Typ.	Max.	Unit
				S1	S3-1	S3-2	S6	S7	S8	S9	S10	S11	S12-1	S12-2	S26	S27	V3 amplitude	V3 frequency	E2	E3	E19	E23	E24	E25	E30					
47	TE	Offset voltage ROM	TE_OfstROM																0V	0V	0V	0V	0V	0V	0V	18	Pin voltage	–150	0	150	mV
48	TE	Offset voltage RW	TE_OfstRW											O												18	Pin voltage	–350	0	350	mV
49	TE	Low frequency gain ROM1	Gte_ROM1								O						0.1Vp-p	1kHz								18	20 log (Vout/Vin)	13	16	19	dB
50	TE	Low frequency gain ROM2	Gte_ROM2									O					0.1Vp-p	1kHz								18	20 log (Vout/Vin)	13	16	19	dB
51	TE	Low frequency gain RW1	Gte_RW1								O			O			25mVp-p	1kHz								18	20 log (Vout/Vin) – Gte_ROM1	11	12	13	dB
52	TE	Low frequency gain RW2	Gte_RW2									O		O			25mVp-p	1kHz								18	20 log (Vout/Vin) – Gte_ROM2	11	12	13	dB
53	TE	Frequency response ROM1	Fte_ROM1								O						0.1Vp-p	100kHz								18	20 log (Vout/Vin) – Gte_ROM1	–3	–1	0	dB
54	TE	Frequency response ROM2	Fte_ROM2									O					0.1Vp-p	100kHz								18	20 log (Vout/Vin) – Gte_ROM2	–3	–1	0	dB
55	TE	Frequency response RW1	Fte_RW1								O			O			25mVp-p	100kHz								18	20 log (Vout/Vin) – Gte_RW1– Gte_ROM1	–3.5	–1.5	0	dB
56	TE	Frequency response RW2	Fte_RW2									O		O			25mVp-p	100kHz			↓					18	20 log (Vout/Vin) – Gte_RW2– Gte_ROM2	–3.5	–1.5	0	dB
57	TE	Balance gain 1	Gte1								O	O					0.1Vp-p	10kHz			1.0V					18	E, F gain difference	4	6	8	dB
58	TE	Balance gain 2	Gte2								O	O					0.1Vp-p	10kHz			–1.0V					18	E, F gain difference	–8	–6	–4	dB
59	TE	Maximum output voltage H	Vte_H									O								0.18V	0V					18	Pin voltage	0.8	1.2	1.45	V
60	TE	Maximum output voltage L	Vte_L								O									0.18V						18	Pin voltage	–1.45	–1.2	–0.8	V
61	CE	Offset voltage ROM	CE_OfstROM																	0V						20	Pin voltage	–120	0	120	mV
62	CE	Offset voltage RW	CE_OfstRW											O												20	Pin voltage	–120	0	120	mV
63	CE	Low frequency gain ROM1	Gce_ROM1				O			O							0.1Vp-p	1kHz								20	20 log (Vout/Vin)	12.5	15.5	18.5	dB
64	CE	Low frequency gain ROM2	Gce_ROM2					O	O								0.1Vp-p	1kHz								20	20 log (Vout/Vin)	12.5	15.5	18.5	dB
65	CE	Low frequency gain RW1	Gce_RW1				O			O				O			25mVp-p	1kHz								20	20 log (Vout/Vin) – Gce_ROM1	11	12	13	dB
66	CE	Low frequency gain RW2	Gce_RW2					O	O					O			25mVp-p	1kHz								20	20 log (Vout/Vin) – Gce_ROM2	11	12	13	dB
67	CE	Frequency response ROM1	Fce_ROM1				O			O							0.1Vp-p	100kHz								20	20 log (Vout/Vin) – Gce_ROM1	–2.7	–1.2	0.3	dB
68	CE	Frequency response ROM2	Fce_ROM2					O	O								0.1Vp-p	100kHz								20	20 log (Vout/Vin) – Gce_ROM2	–2.7	–1.2	0.3	dB
69	CE	Frequency response RW1	Fce_RW1				O			O				O			25mVp-p	100kHz								20	20 log (Vout/Vin) – Gce_RW1– Gce_ROM1	–2.7	–1.2	0.3	dB
70	CE	Frequency response RW2	Fce_RW2					O	O					O			25mVp-p	100kHz			↓					20	20 log (Vout/Vin) – Gce_RW2– Gce_ROM2	–2.7	–1.2	0.3	dB
71	CE	Maximum output voltage H	Vce_H					O	O											0.18V						20	Pin voltage	0.75	1	1.45	V
72	CE	Maximum output voltage L	Vce_L				O			O									↓	0.18V	↓	↓	↓	↓	↓	20	Pin voltage	–1.45	–1	–0.75	V

Measurement No.	Function	Measurement item	Symbol	Switch conditions															Bias conditions									Measurement pin	Measurement conditions	Min.	Typ.	Max.	Unit
				S1	S3-1	S3-2	S6	S7	S8	S9	S10	S11	S12-1	S12-2	S26	S27	V3 amplitude	V3 frequency	E2	E3	E19	E23	E24	E25	E30						
73	APC	Output voltage 1	Vapc1																adj	0V	0V	0V	0V	0V	0V		1	Input at which output voltage = 0V	50	150	250	mV
74		Output voltage 2	Vapc2																Vapc1 + 20mV								1	Pin voltage	0.5	0.75	1	V
75		Output voltage 3	Vapc3																Vapc1 – 20mV								1	Pin voltage	–1	–0.75	–0.5	V
76		APC OFF voltage	Vapc_off										O						0V								1	Pin voltage	1.25	1.45	1.5	V
77		Maximum output current	Iapc_max	O																							1	Pin voltage	–0.25	0.1	0.45	V
78	AVC	Output voltage	Vavc													O											27	Pin voltage	–50	0	50	mV
79	DVC	Output voltage	Vdvc																								14	Pin voltage	–50	0	50	mV

Electrical Characteristics Measurement Circuit

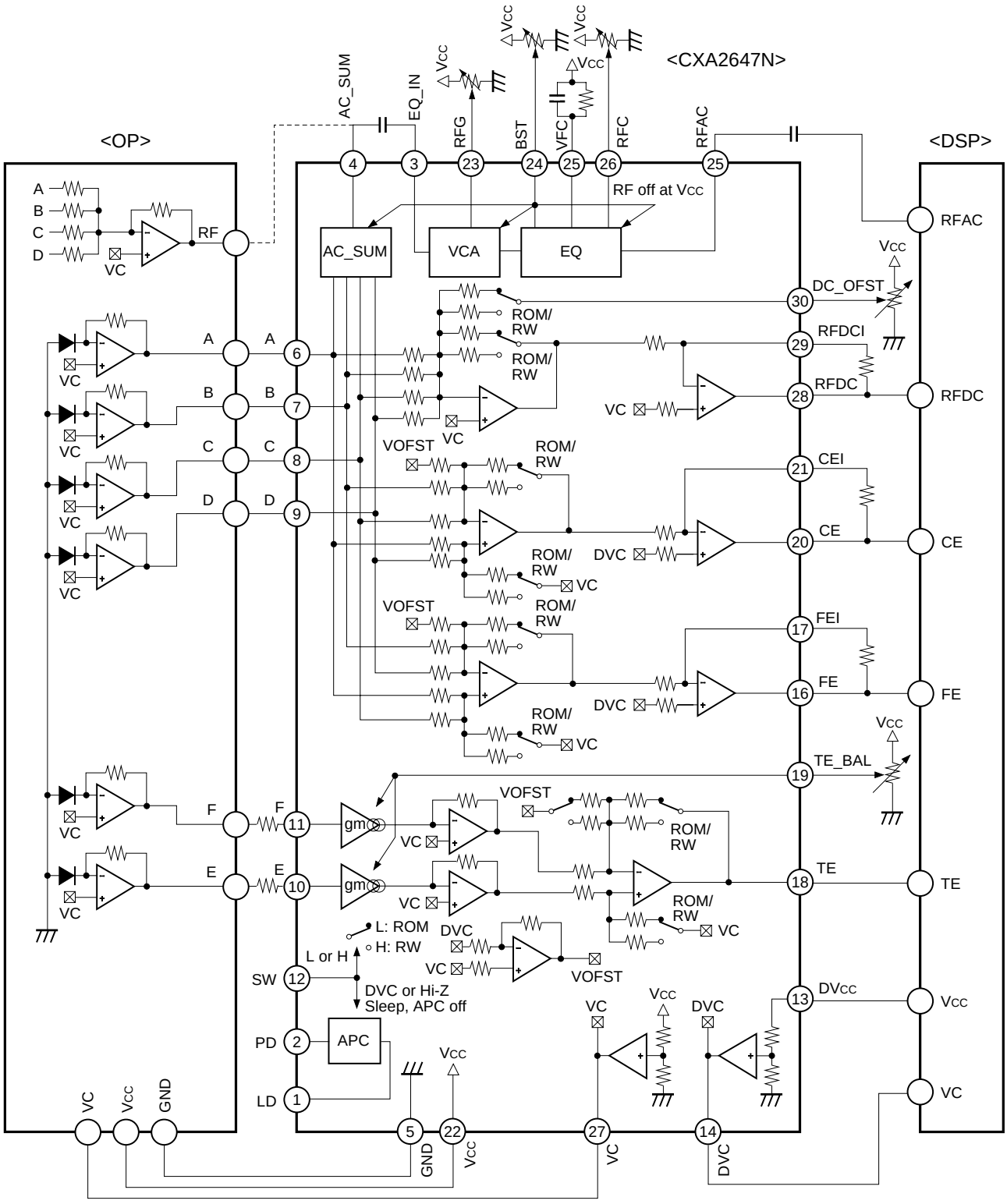


Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Connection Example of DP and DSP

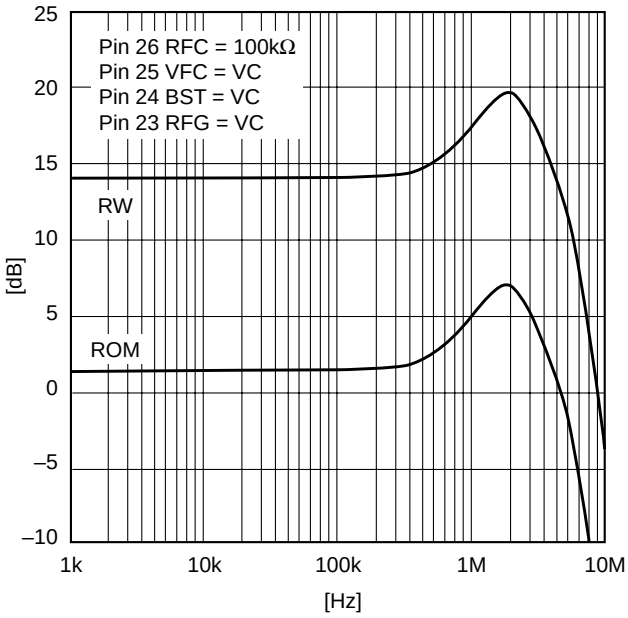


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

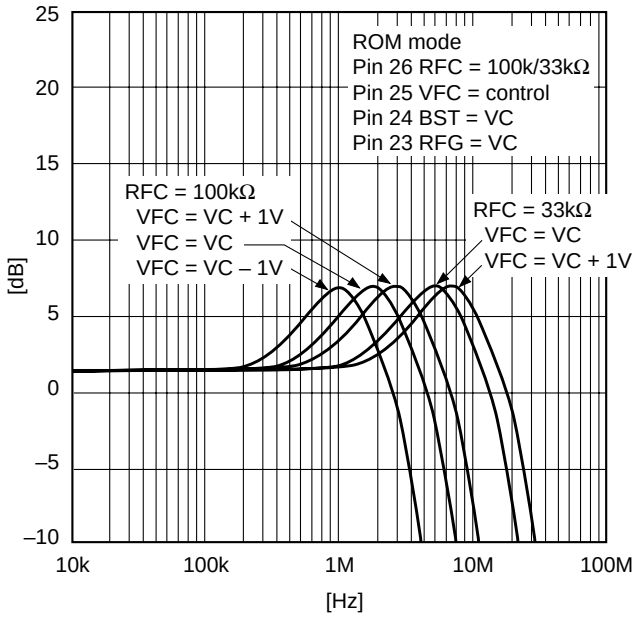
Characteristics Graphs (Vcc = 3.0V, DVcc = 3.0V)

1. EQ characteristics Input: Pin 3 EQ_IN
Output: Pin 15 RFAC

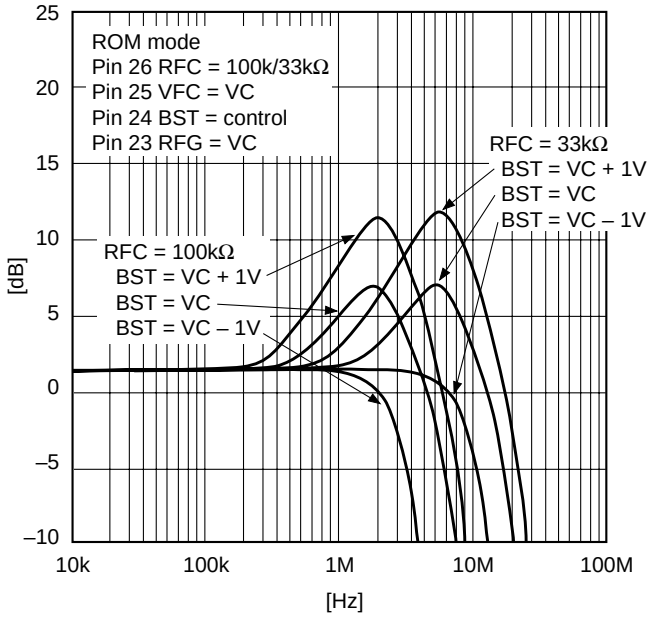
1-1. EQ ROM/RW characteristics



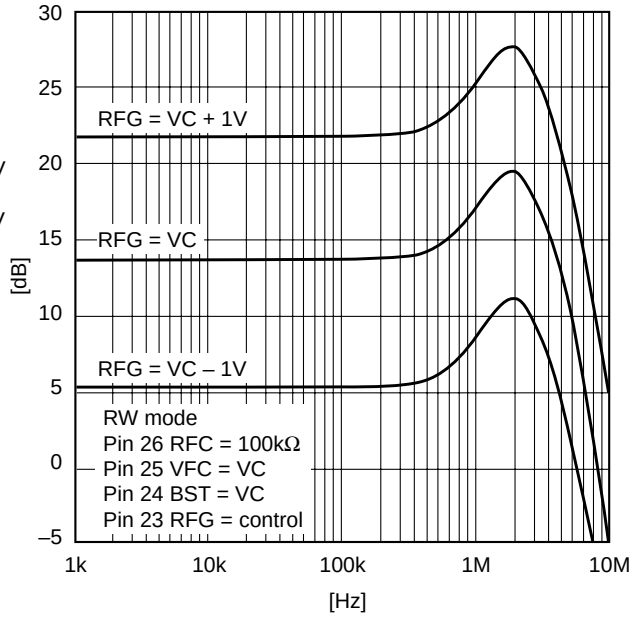
1-2. EQ fc control characteristics



1-3. EQ boost control characteristics



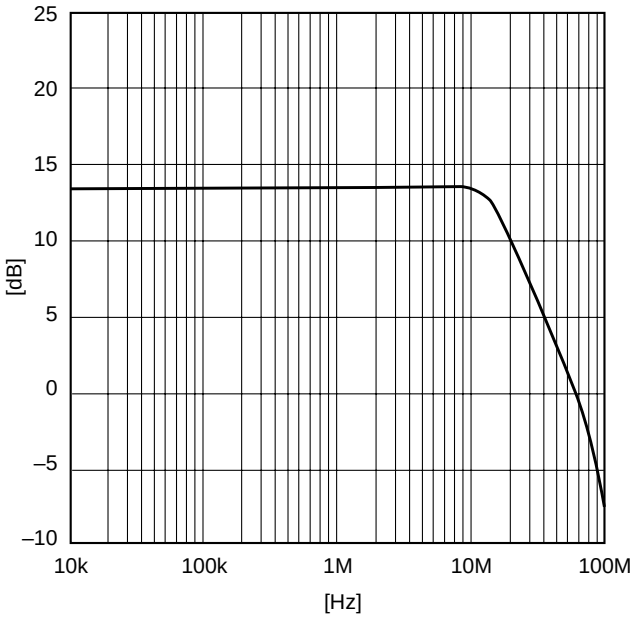
1-4. EQ gain control characteristics



2. AC_SUM characteristics

Input: Pin 6, 7, 8, 9 A, B, C, D

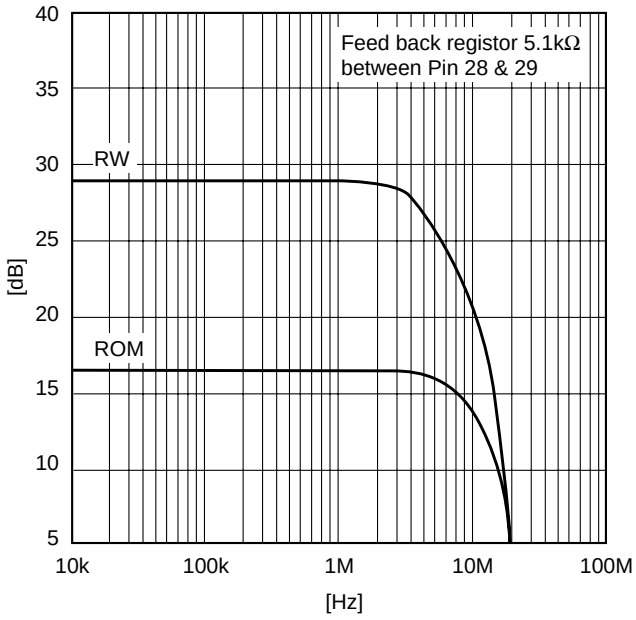
Output: Pin 4 AC_SUM



3. RFDC characteristics

Input: Pin 6, 7, 8, 9 A, B, C, D

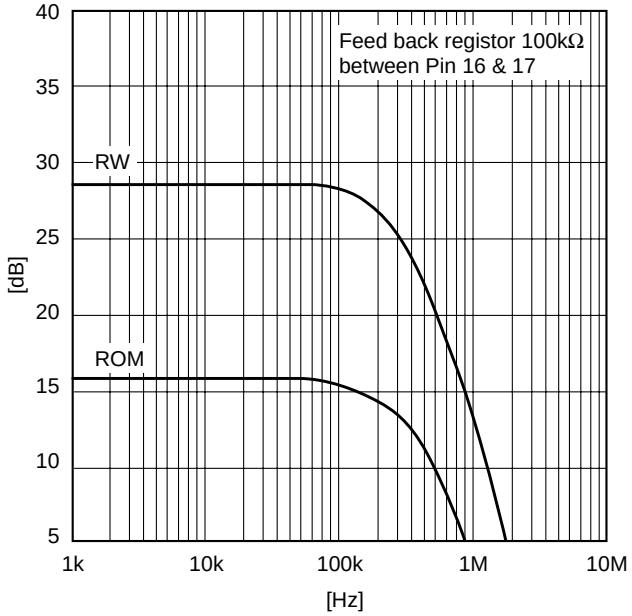
Output: Pin 28 RFDC



3. FE characteristics

Input: Pin 6, 8 A, C

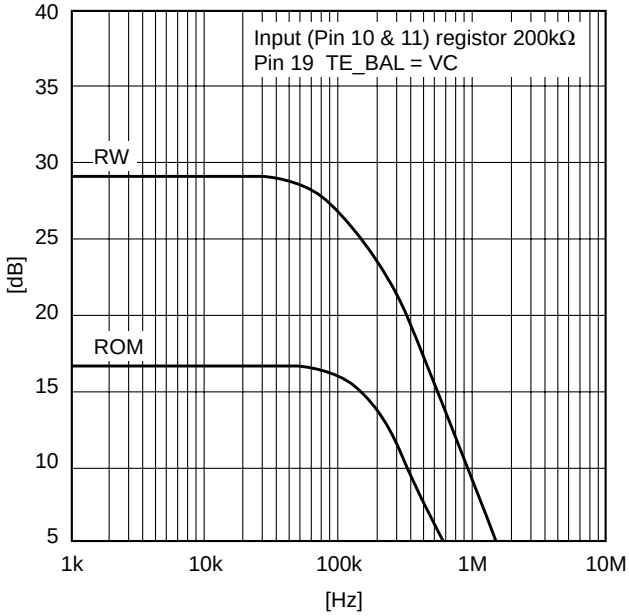
Output: Pin 16 FE



4. TE characteristics

Input: Pin 10 E

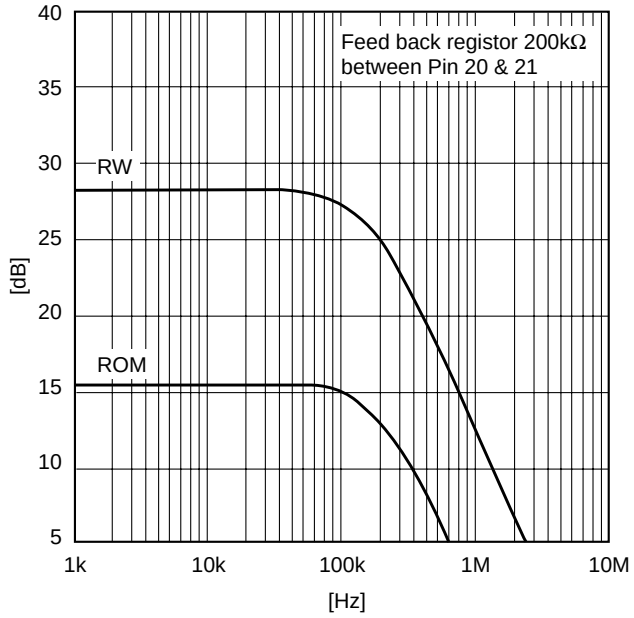
Output: Pin 18 TE



3. CE characteristics

Input: Pin 6, 9 A, D

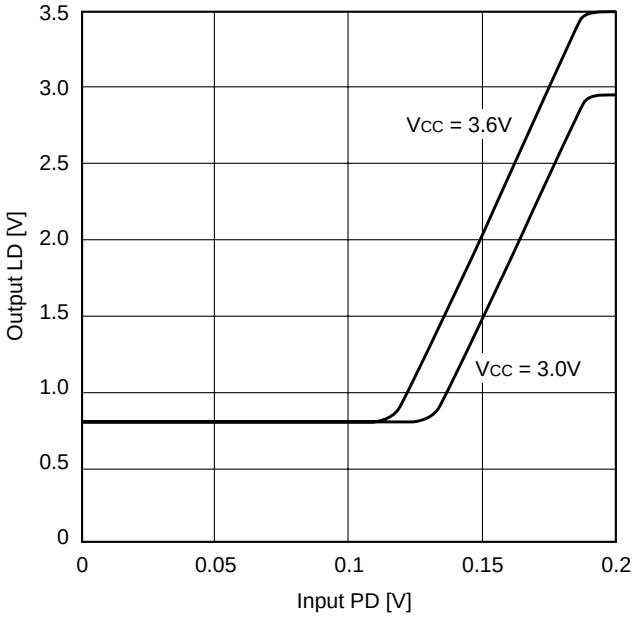
Output: Pin 20 CE



3. APC input/output characteristics

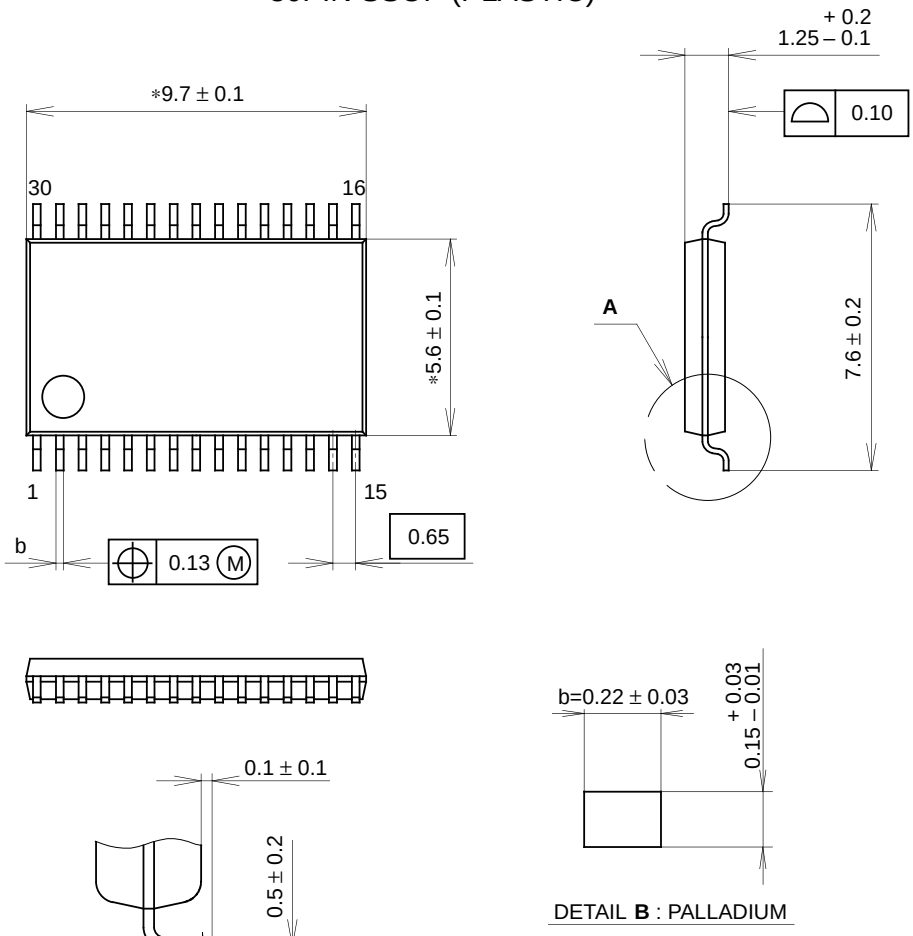
Input: Pin 2 PD

Output: Pin 1 LD



Package Outline Unit: mm

30PIN SSOP (PLASTIC)



DETAIL **B** : PALLADIUM

DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-30P-L01
EIAJ CODE	P-SSOP30-5.6x9.7-0.65
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g