8-Channel VARIABLE GAIN AMPLIFIER

Check for Samples: VCA8617

FEATURES

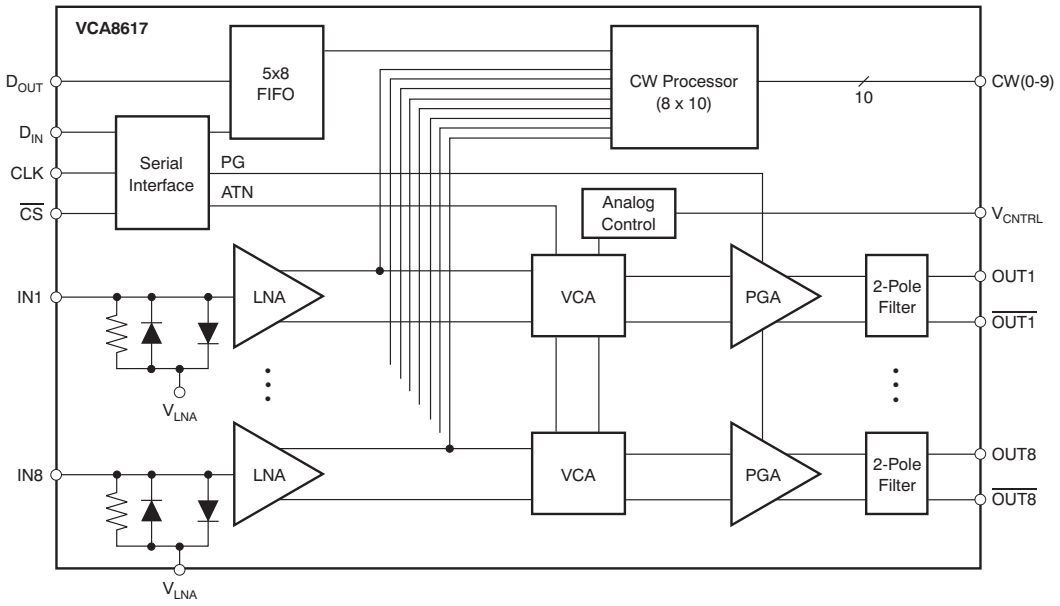
- **3V OPERATION**
- **LOW INPUT NOISE:**
  - **1.05nV/√Hz at f_{IN} = 5MHz**
- **EXTREMELY LOW POWER OPERATION:**
  - **103mW/CHANNEL**
- **INTEGRATED LOW-PASS, ANTI-ALIASING BUTTERWORTH FILTER**
  - **14.5MHz BANDWIDTH**
- **INTEGRATED INPUT CLAMP DIODES**
- **DIFFERENTIAL OUTPUT**
- **INTEGRATED INPUT LNA**
- **READABLE CONTROL REGISTERS**
- **INTEGRATED CONTINUOUS WAVE (CW) PROCESSOR**

DESCRIPTION

The VCA8617 is an 8-channel variable gain amplifier ideally suited to portable ultrasound applications. Excellent dynamic performance enables use in low-power, high-performance portable applications. Each channel consists of a 20dB gain Low-Noise pre-Amplifier (LNA) and a Variable Gain Amplifier (VGA). The differential outputs of the LNA can be switched through the 8x10 cross-point switch, which is programmable through the serial interface input port.

The output of the LNA is fed directly into the VGA stage. The VGA consists of two parts, a Voltage-Controlled Attenuator (VCA) and a Programmable Gain Amplifier (PGA). The gain and gain range of the PGA can be digitally configured separately. The gain of the PGA can vary between four discrete settings of 25dB, 30dB, 35dB, and 40dB. The VCA has four programmable maximum attenuation settings: 29dB, 33dB, 36.5dB, and 40dB. Also, the VCA can be continuously varied by a control voltage from 0dB to a maximum of 29dB, 33dB, 36.5dB, and 40dB.

The output of the PGA feeds directly into an integrated low-pass filter.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VCA8617	TQFP-64	PAG	−40°C to +85°C	VCA8617PAG	VCA8617PAGT	Tape and Reel, 250
					VCA8617PAGR	Tape and Reel, 1500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range unless otherwise noted.

$+AV_{DD}$	+3.6V
Analog Input	−0.3V to $+AV_{DD}$ + 0.3V
Logic Input	−0.3V to $+AV_{DD}$ + 0.3V
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C
Thermal Resistance, Junction-to-Ambient (θ_{JA})	66.6°C/W
Thermal Resistance, Junction-to-Case (θ_{JC})	4.3°C/W

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

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ELECTRICAL CHARACTERISTICS: $AV_{DD} = DV_{DD} = 3V$

At T_A = +25°C, load resistance = 1kΩ on each output to ground, unless otherwise noted. The input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

PARAMETER	CONDITIONS	VCA8617			UNIT
		MIN	TYP	MAX	
Input Voltage Noise (TGC, Full Signal Chain)	f_{IN} = 5MHz		1.05		nV/√Hz
Input Voltage Noise (CW)	f_{IN} = 5MHz		1.15		nV/√Hz
PREAMPLIFIER (LNA)					
Input Resistance			4.5		kΩ
Input Capacitance			52		pF
Input Bias Current			1		nA
Maximum Input Voltage(1)			200		mV_{PP}
Output Swing (Differential)			2		V_{PP}
Bandwidth			100		MHz
Gain			20		dB
Input Common-Mode Voltage			1.4		V
ACCURACY					
Gain Slope	0.2V − 1.7V, V_{CNTRL}		18		dB/V
Gain Error	0.2V − 1.7V, V_{CNTRL}			1.7	dB
Output Offset Voltage	Differential		0.65		mV
GAIN CONTROL INTERFACE					
Input Voltage (VCA_{CNTRL}) Range			0 to 2.0		V
Input Resistance			1		MΩ
Response Time	40dB Gain Change, PG = 11		0.2		µs
POWER SUPPLY					
Specified Operating Range		2.85	3.0	3.15	V
Power-Down Delay			5		µs
Power-Up Delay			100		µs
Power Dissipation (TGC Mode)	Operating All Channels		825	950	mW
Power-Down			9		mW
PROGRAMMABLE VGA AND LOW-PASS FILTER					
−3dB Cutoff (low-pass)			14.5		MHz
−3dB Cutoff (high-pass)			400		kHz
Slew Rate			300		V/µs
Output Impedance			10		Ω
Crosstalk			49		dB
Output Common-Mode Voltage			1.5		V
Output Swing (Differential)(2)				2	V_{PP}
3rd-Harmonic Distortion			–65	–50	dB
2nd-Harmonic Distortion			–60	–50	dB
Group Delay Variation			±3		ns
CONTINUOUS WAVE PROCESSOR					
V/I Converter Transconductance		17	20	23	mA/V
Output Common-Mode Voltage			1.4		V
Maximum Output Swing			3.4		mA_{PP}

(1) Under conditions when input signal is within linear range of LNA.
(2) Under conditions when signal is within linear range of output amplifier.

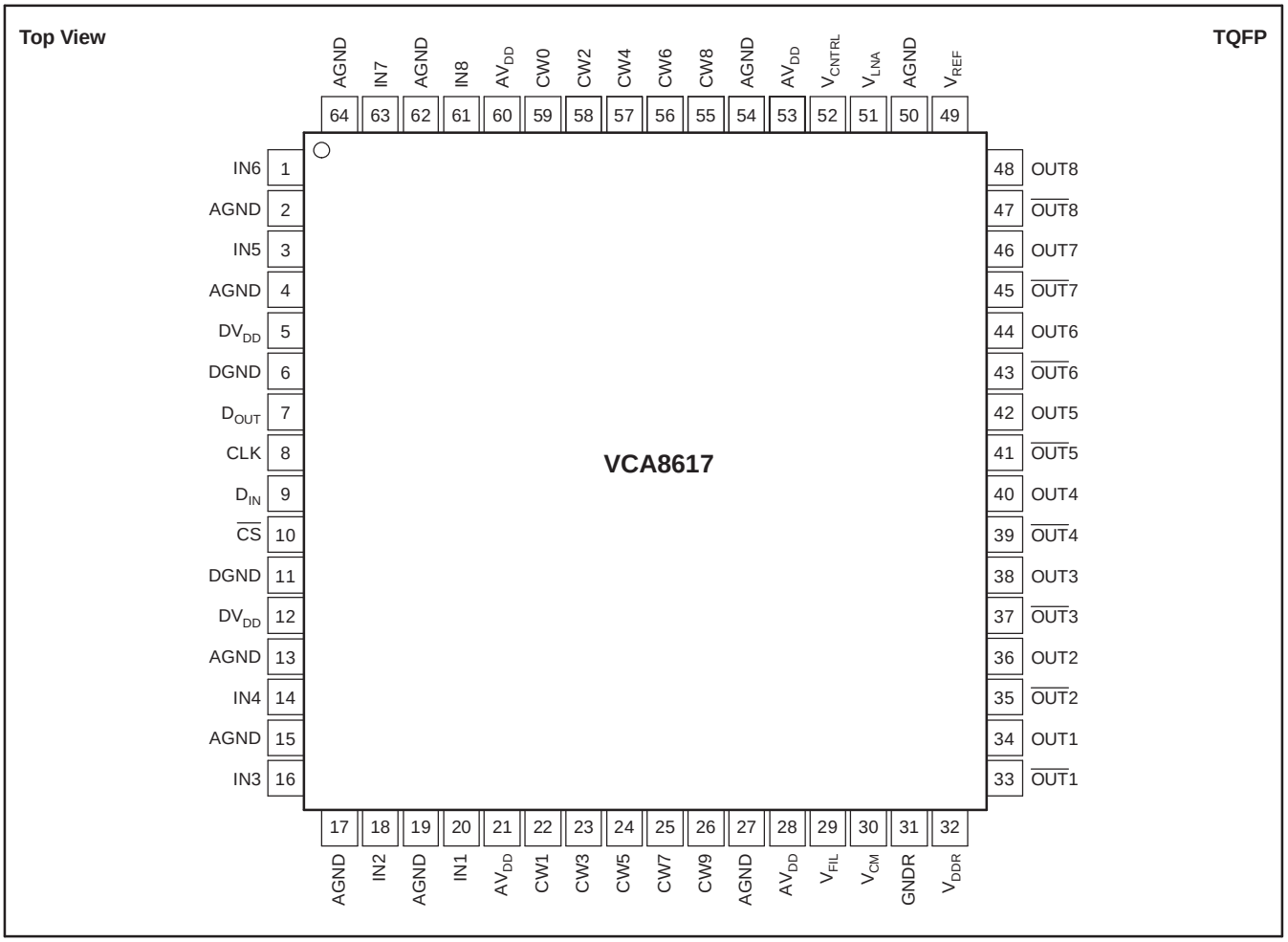
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ELECTRICAL CHARACTERISTICS: $AV_{DD} = DV_{DD} = 3V$ (continued)

At T_A = +25°C, load resistance = 1kΩ on each output to ground, unless otherwise noted. The input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

PARAMETER	CONDITIONS	VCA8617			UNIT
		MIN	TYP	MAX	
LOGIC INPUTS					
V_{IN} LOW (input low voltage)		0		0.6	V
V_{IN} HIGH (input high voltage)		2.1		DV_{DD}	V
Input Current				±1	µA
Input Pin Capacitance			5		pF
Clock Input Frequency		10k		25M	Hz

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PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
5, 12	DV_{DD}	Digital Supplies
2, 4, 13, 15, 17, 19, 27, 50, 54, 62, 64	AGND	Analog Ground
1, 3, 14, 16, 18, 20, 61, 63	IN(1−8)	Single-Ended LNA Inputs
22−26, 55−59	CW(0−9)	Continuous Wave Outputs
51	V_{LNA}	Reference Voltage for LNA−internally generated; requires external bypass cap.
29	V_{FIL}	Reference Voltage for Output Filter−internally generated; requires external bypass cap.
30	V_{CM}	Common-Mode Voltage−internally generated; requires external bypass cap.
34, 36, 38, 40, 42, 44, 46, 48	OUT(1−8)	Positive Polarity PGA Outputs
33, 35, 37, 39, 41, 43, 45, 47	$\overline{OUT}$(1−8)	Negative Polarity PGA Outputs
52	V_{CNTRL}	Attenuator Control Input
9	D_{IN}	Serial Data Input Pin
10	$\overline{CS}$	Serial Data Chip Select
8	CLK	Serial Data Input Clock
7	D_{OUT}	Serial Data Output Pin
21, 28, 53, 60	AV_{DD}	Analog Supplies
6, 11	DGND	Digital Ground
49	V_{REF}	Reference Voltage for Attenuator−internally generated; requires external bypass cap.
32	V_{DDR}	Reference Power Supply
31	GNDR	Reference Ground

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INPUT REGISTER BIT MAPS

Table 1. Byte 1—Control Byte Register Map

BIT #	NAME	DESCRIPTION
LSB	1	Start bit; always a '1'—40-bit countdown starts upon first '1' after chip select.
1	$\overline{W}$/R	1 = Write, 0 = Read—Read prevents latching of DATA only—Control register remains latched with existing data.
2	P_{WR}	Power-Down control bit (all channels); 1 = Power-Down Mode Enabled (default), 0 = Normal Operation.
3	A0	Attenuator control bit (ATN).
4	A1	Attenuator control bit (ATN).
5	Mode	1 = TGC Control mode (CW powered down), 0 = Doppler mode (TGC powered down)
6	PG0	LSB of PGA Gain Control
MSB	PG1	MSB of PGA Gain Control

Table 2. Byte 2—First Data Byte

BIT #	NAME	DESCRIPTION
LSB	Data 1:0	Channel 1, LSB of Matrix Control
1	Data 1:1	Channel 1, Matrix Control
2	Data 1:2	Channel 1, Matrix Control
3	Data 1:3	Channel 1, MSB of Matrix Control
4	Data 2:0	Channel 2, LSB of Matrix Control
5	Data 2:1	Channel 2, Matrix Control
6	Data 2:2	Channel 2, Matrix Control
MSB	Data 2:3	Channel 2, MSB of Matrix Control

Table 3. Byte 3—Second Data Byte

BIT #	NAME	DESCRIPTION
LSB	Data 3:0	Channel 3, LSB of Matrix Control
1	Data 3:1	Channel 3, Matrix Control
2	Data 3:2	Channel 3, Matrix Control
3	Data 3:3	Channel 3, MSB of Matrix Control
4	Data 4:0	Channel 4, LSB of Matrix Control
5	Data 4:1	Channel 4, Matrix Control
6	Data 4:2	Channel 4, Matrix Control
MSB	Data 4:3	Channel 4, MSB of Matrix Control

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Table 4. Byte 4—Third Data Byte

BIT #	NAME	DESCRIPTION
LSB	Data 5:0	Channel 5, LSB of Matrix Control
1	Data 5:1	Channel 5, Matrix Control
2	Data 5:2	Channel 5, Matrix Control
3	Data 5:3	Channel 5, MSB of Matrix Control
4	Data 6:0	Channel 6, LSB of Matrix Control
5	Data 6:1	Channel 6, Matrix Control
6	Data 6:2	Channel 6, Matrix Control
MSB	Data 6:3	Channel 6, MSB of Matrix Control

Table 5. Byte 5—Fourth Data Byte

BIT #	NAME	DESCRIPTION
LSB	Data 7:0	Channel 7, LSB of Matrix Control
1	Data 7:1	Channel 7, Matrix Control
2	Data 7:2	Channel 7, Matrix Control
3	Data 7:3	Channel 7, MSB of Matrix Control
4	Data 8:0	Channel 8, LSB of Matrix Control
5	Data 8:1	Channel 8, Matrix Control
6	Data 8:2	Channel 8, Matrix Control
MSB	Data 8:3	Channel 8, MSB of Matrix Control

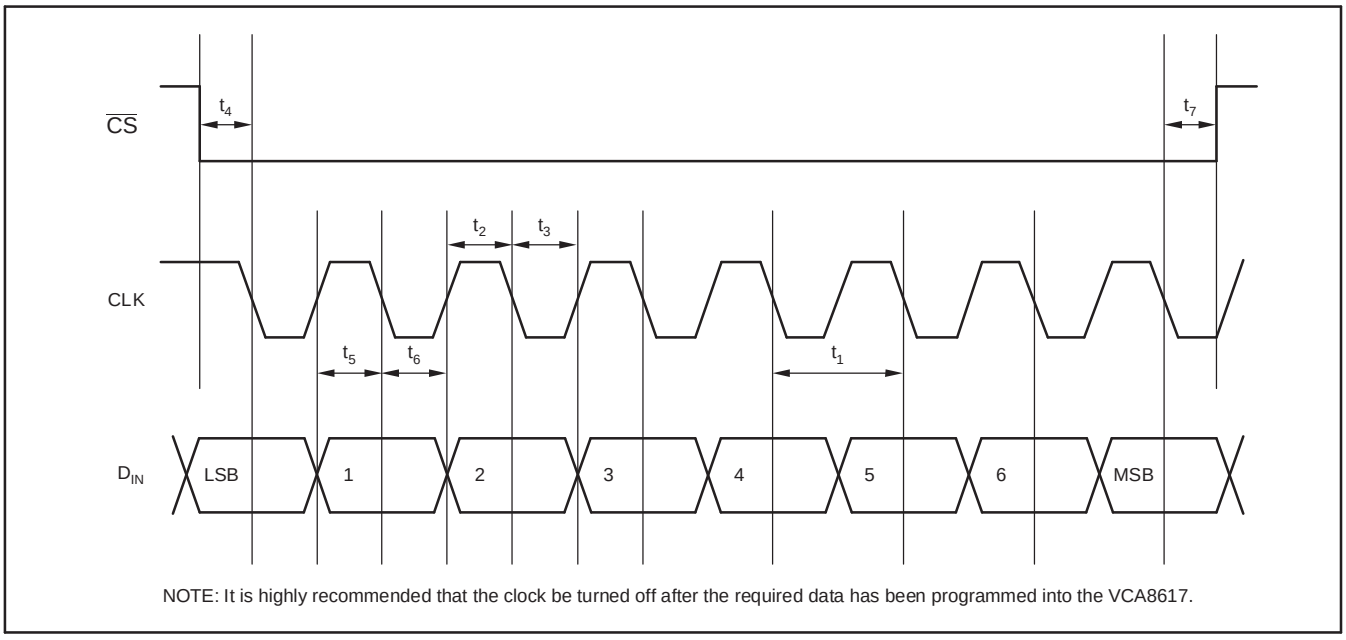
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WRITE/READ TIMING

Generally follows SPI Timing Specification:

- All writes and reads are 40 bits at a time. Each byte consists of 8 bits;
- Separate write and read data lines;
- Reads will follow the same bit stream pattern seen in the write cycle;
- Reads will extract data from the FIFO, not the latched register;
- D_{OUT} data is continuously available and need not be enabled with a read cycle. Selecting a read cycle in the control register only prevents latching of data. The control register remains latched.

WRITE CYCLE TIMING



NOTE: It is highly recommended that the clock be turned off after the required data has been programmed into the VCA8617.

SERIAL PORT TIMING TABLE

Chip Select ($\overline{CS}$) must be held low (active LOW) during transfer. $\overline{CS}$ can be held permanently low.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Serial CLK Period	40			ns
t_2	Serial CLK HIGH Time	20			ns
t_3	Serial CLK LOW Time	20			ns
t_4	$\overline{CS}$ Falling Edge to Serial CLK Falling Edge	10			ns
t_5	Data Setup Time	5			ns
t_6	Data Hold Time	5			ns
t_7	Serial CLK Falling Edge to $\overline{CS}$ Rising Edge	10			ns

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DATA SHIFT SEQUENCE

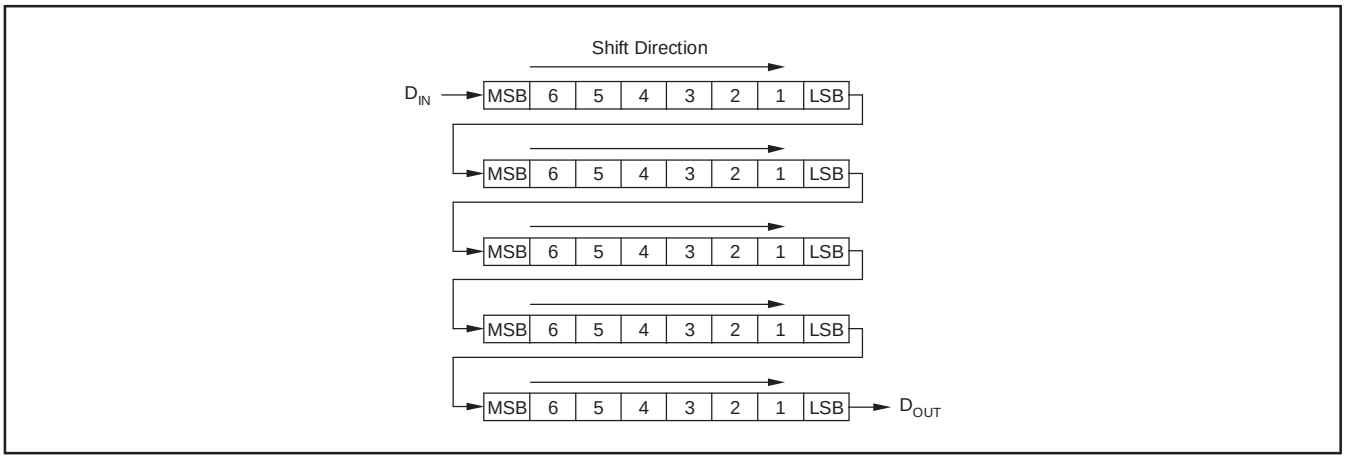


Table 6. Maximum Attenuation

A1, A0	MAXIMUM ATTENUATION
0, 0	29dB
0, 1	33dB
1, 0	36.5dB
1, 1	40dB

Table 7. PGA Gain Settings

PG1, PG0	PGA GAIN
0, 0	25dB
0, 1	30dB
1, 0	35dB
1, 1	40dB

Table 8. CW Coding for Each Channel

CHANNEL	CW CODING (MSB, LSB)	CHANNEL DIRECTED TO:
0	0000	Output 0
1	0001	Output 1
2	0010	Output 2
3	0011	Output 3
4	0100	Output 4
5	0101	Output 5
6	0110	Output 6
7	0111	Output 7
8	1000	Output 8
9	1001	Output 9
10	1010	Channel tied to +V (internal)
11	1011	Channel tied to +V (internal)
12	1100	Channel tied to +V (internal)
13	1101	Channel tied to +V (internal)
14	1110	Channel tied to +V (internal)
15	1111	Channel tied to +V (internal)
Applies to bytes 2 through 5.		

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TYPICAL CHARACTERISTICS: $AV_{DD} = DV_{DD} = 3V$

At T_A = +25°C, load resistance = 1kΩ on each output to ground; the input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

GAIN vs V_{CNTRL} (PG = 00, 25dB)

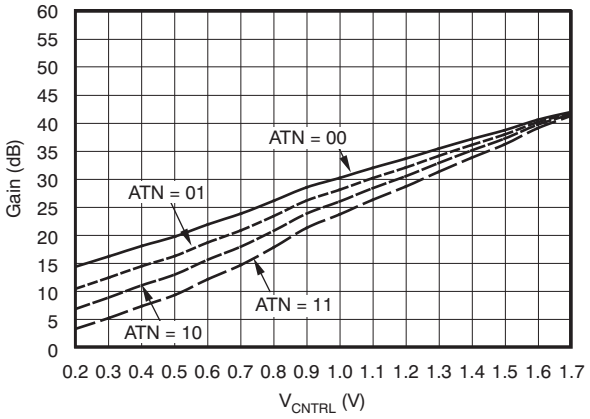


Figure 1.

GAIN vs V_{CNTRL} (PG = 01, 30dB)

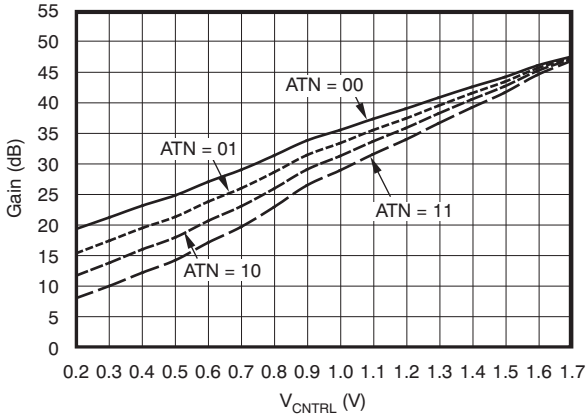


Figure 2.

GAIN vs V_{CNTRL} (PG = 10, 35dB)

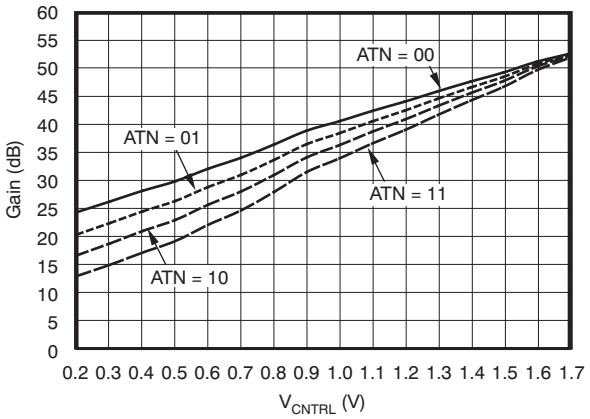


Figure 3.

GAIN vs V_{CNTRL} (PG = 11, 40dB)

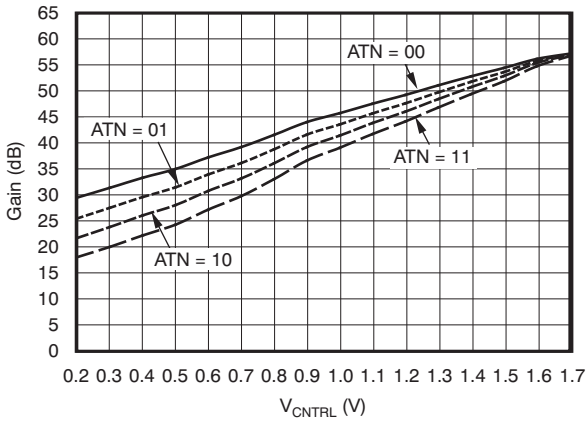


Figure 4.

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TYPICAL CHARACTERISTICS: AV_{DD} = DV_{DD} = 3V (continued)

At T_A = +25°C, load resistance = 1kΩ on each output to ground; the input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

GAIN ERROR vs V_{CNTRL} (PG = 00)

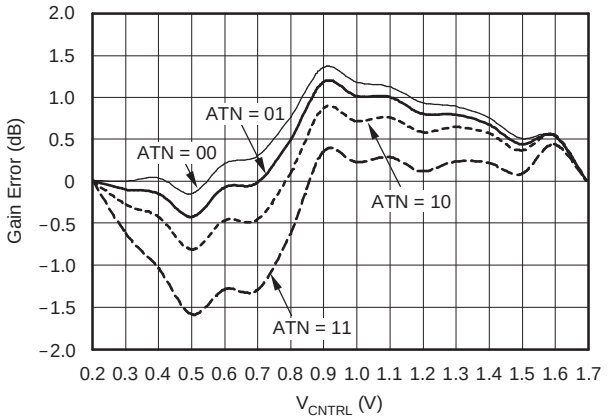


Figure 5.

GAIN ERROR vs V_{CNTRL} (PG = 01)

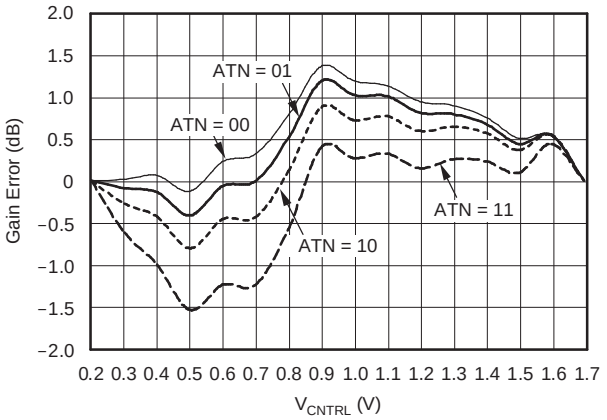


Figure 6.

GAIN ERROR vs V_{CNTRL} (PG = 10)

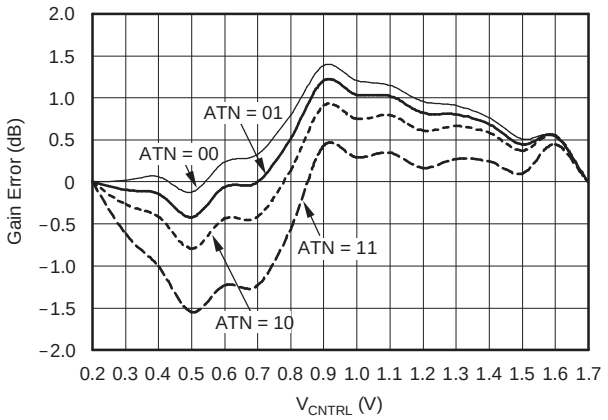


Figure 7.

GAIN ERROR vs V_{CNTRL} (PG = 11)

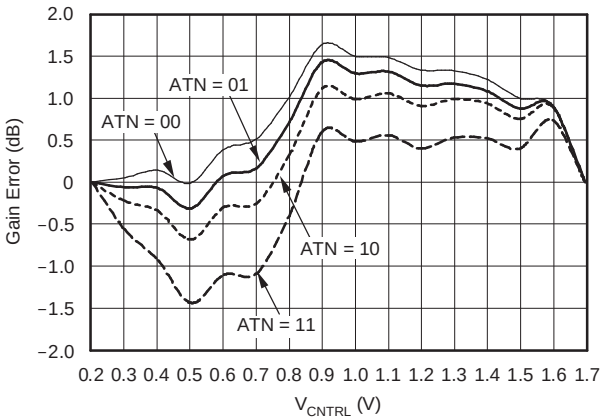


Figure 8.

GAIN ERROR vs V_{CNTRL} vs FREQUENCY

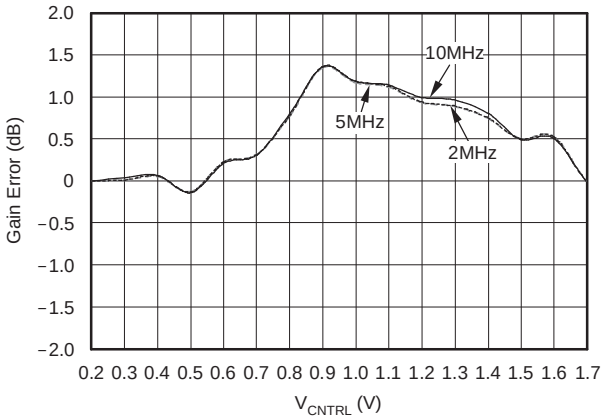


Figure 9.

GAIN ERROR vs V_{CNTRL} vs TEMPERATURE

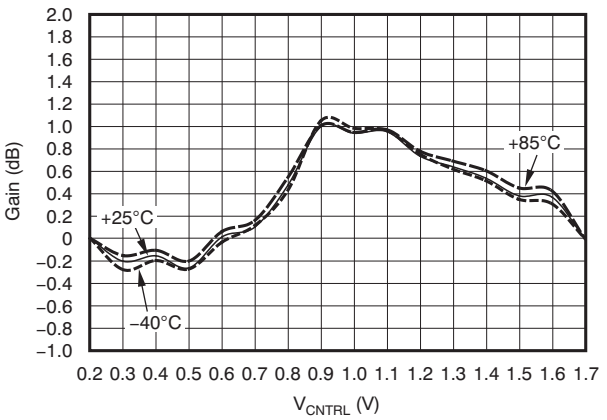


Figure 10.

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TYPICAL CHARACTERISTICS: AV_{DD} = DV_{DD} = 3V (continued)

At T_A = +25°C, load resistance = 1kΩ on each output to ground; the input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

TIME GAIN CONTROL (TGC) CURRENT vs TEMPERATURE

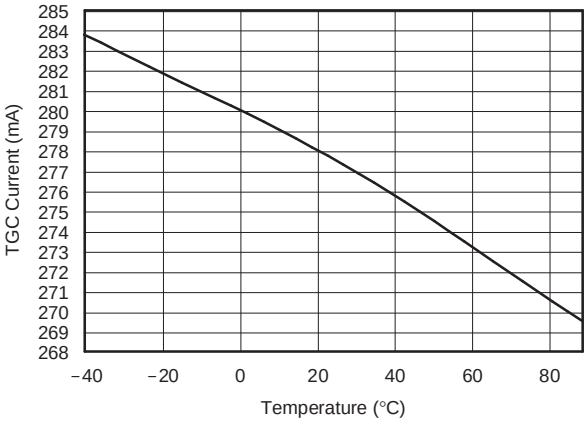


Figure 11.

CONTINUOUS WAVE (CW) CURRENT vs TEMPERATURE

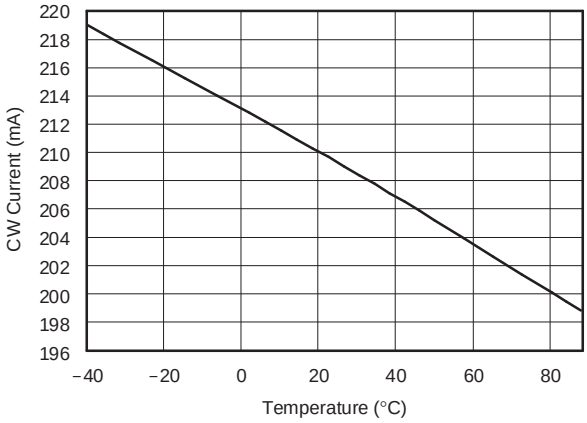


Figure 12.

GAIN MATCH (V_{CNTRL} = 0.2V)

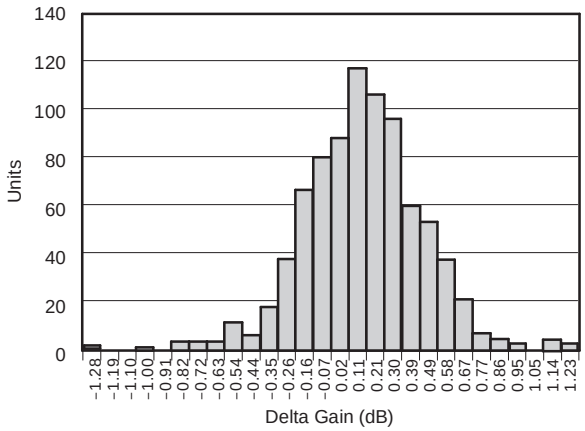


Figure 13.

GAIN MATCH (V_{CNTRL} = 1.7V)

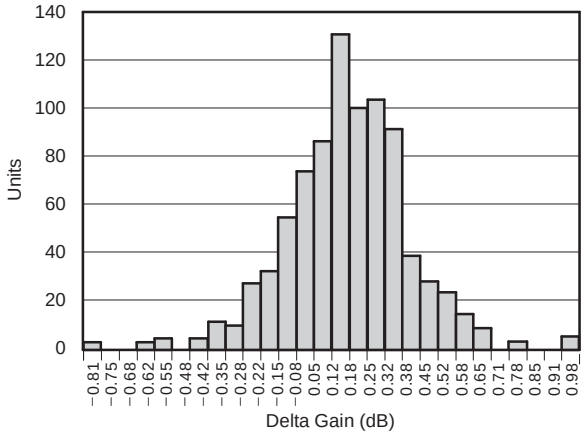


Figure 14.

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TYPICAL CHARACTERISTICS: AV_{DD} = DV_{DD} = 3V (continued)

At T_A = +25°C, load resistance = 1kΩ on each output to ground; the input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

CW ACCURACY

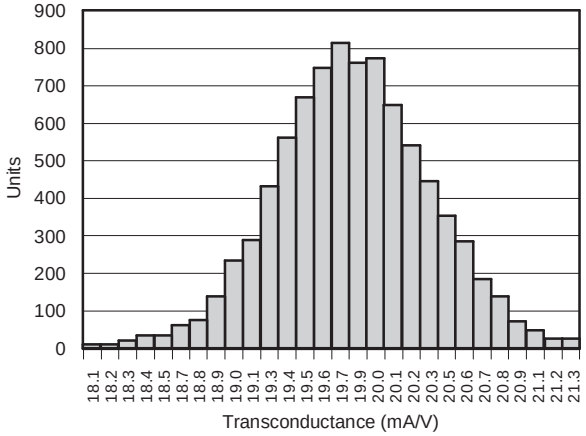


Figure 15.

GAIN vs FREQUENCY (ATN = 00, V_{CNTRL} = 0.2V)

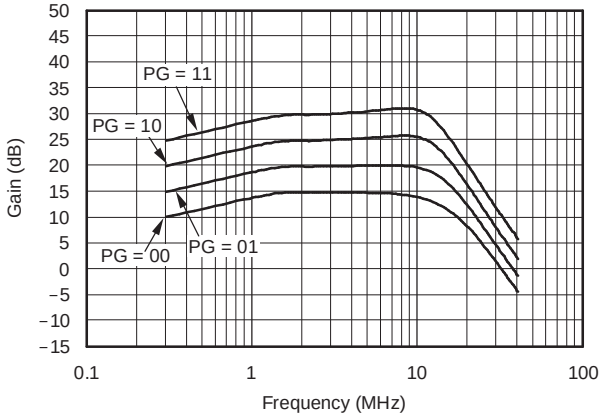


Figure 16.

GAIN vs FREQUENCY (ATN = 00, V_{CNTRL} = 1.7V)

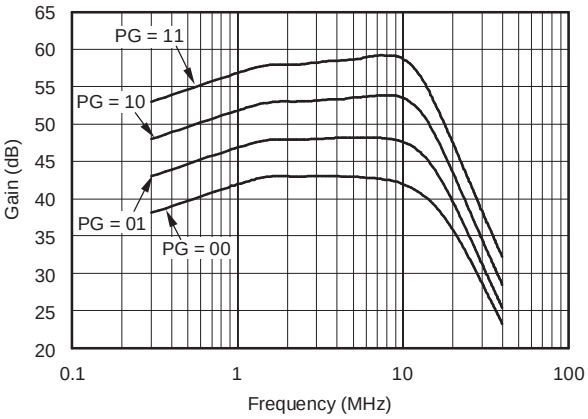


Figure 17.

OUTPUT-REFERRED NOISE vs V_{CNTRL} (ATN = 00, f_{IN} = 2MHz)

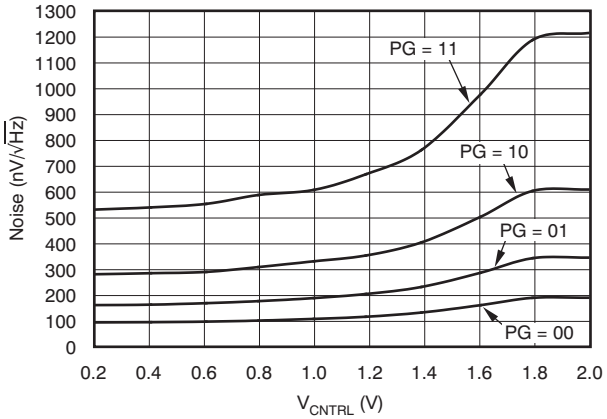


Figure 18.

TYPICAL CHARACTERISTICS: $AV_{DD} = DV_{DD} = 3V$ (continued)

At T_A = +25°C, load resistance = 1kΩ on each output to ground; the input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

OUTPUT-REFERRED NOISE vs V_{CNTRL} (ATN = 00, f_{IN} = 5MHz)

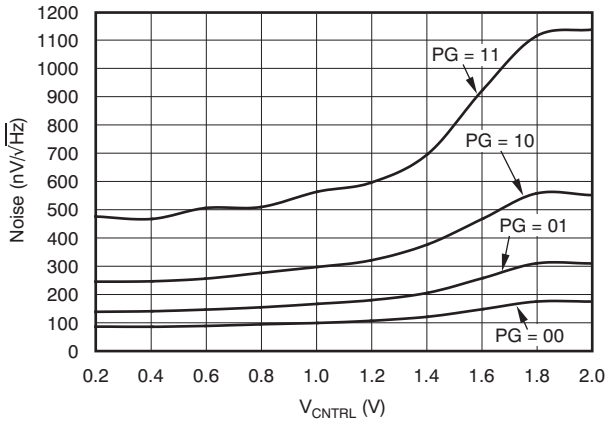


Figure 19.

INPUT-REFERRED NOISE vs V_{CNTRL} (ATN = 00, f_{IN} = 2MHz)

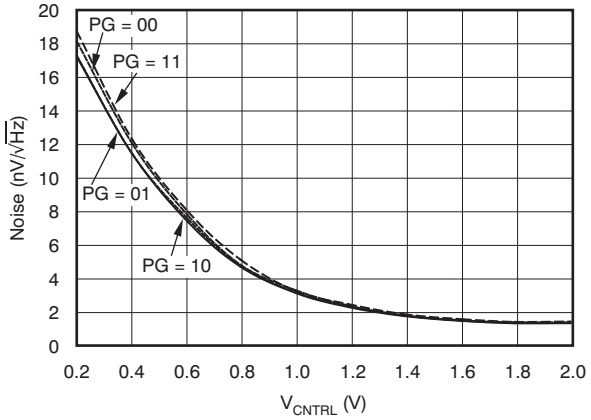


Figure 20.

INPUT-REFERRED NOISE vs V_{CNTRL} (ATN = 00, f_{IN} = 5MHz)

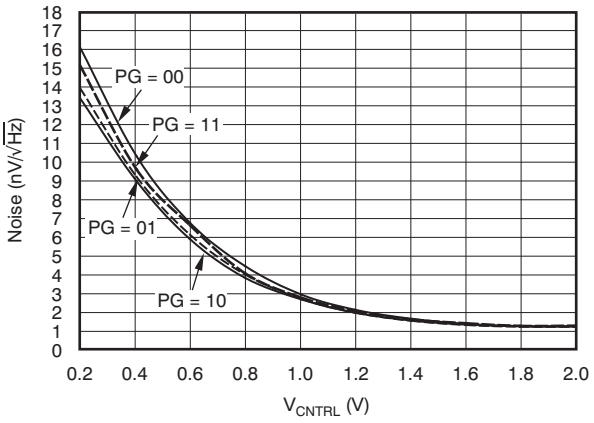


Figure 21.

NOISE FIGURE vs V_{CNTRL} (ATN = 00, f_{IN} = 2MHz)

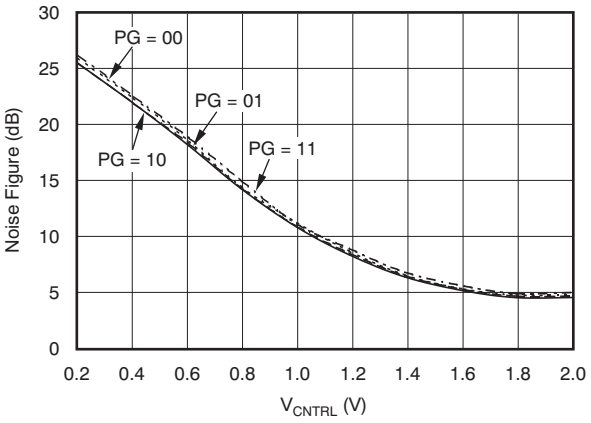


Figure 22.

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TYPICAL CHARACTERISTICS: AV_{DD} = DV_{DD} = 3V (continued)

At T_A = +25°C, load resistance = 1kΩ on each output to ground; the input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

NOISE FIGURE vs V_{CNTRL} (ATN = 00, f_{IN} = 5MHz)

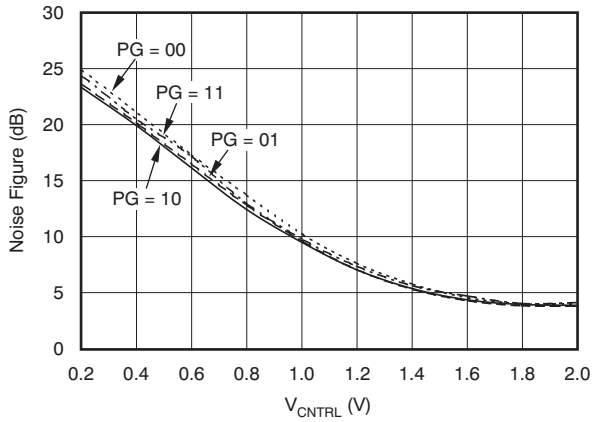


Figure 23.

OUTPUT-REFERRED NOISE vs V_{CNTRL} (ATN = 11, f_{IN} = 2MHz)

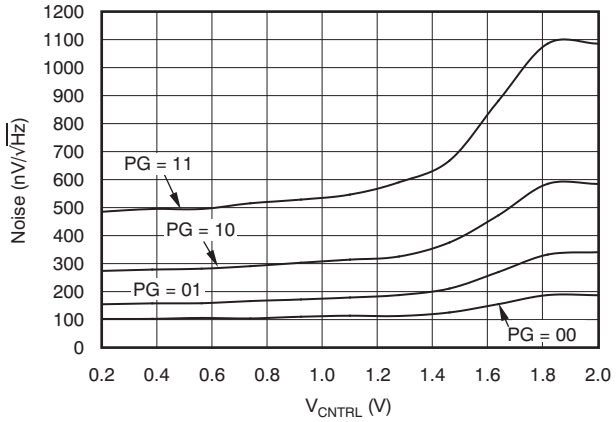


Figure 24.

OUTPUT-REFERRED NOISE vs V_{CNTRL} (ATN = 11, f_{IN} = 5MHz)

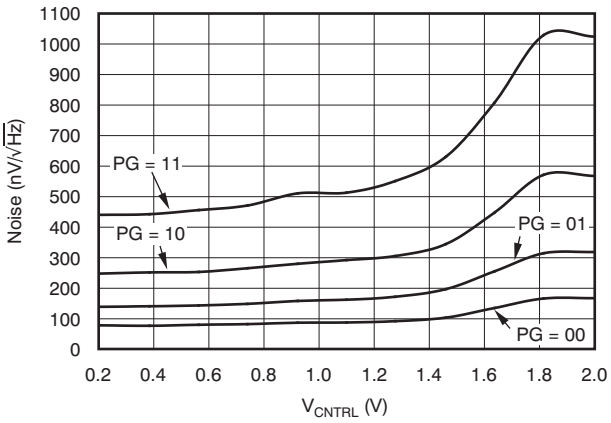


Figure 25.

INPUT-REFERRED NOISE vs V_{CNTRL} (ATN = 11, f_{IN} = 2MHz)

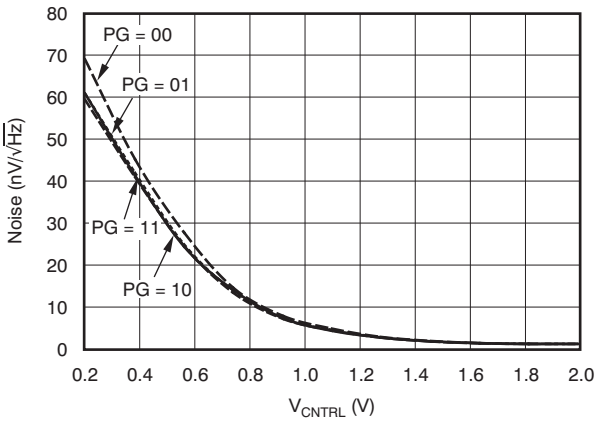


Figure 26.

TYPICAL CHARACTERISTICS: AV_{DD} = DV_{DD} = 3V (continued)

At T_A = +25°C, load resistance = 1kΩ on each output to ground; the input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

INPUT-REFERRED NOISE vs V_{CNTRL} (ATN = 11, f_{IN} = 5MHz)

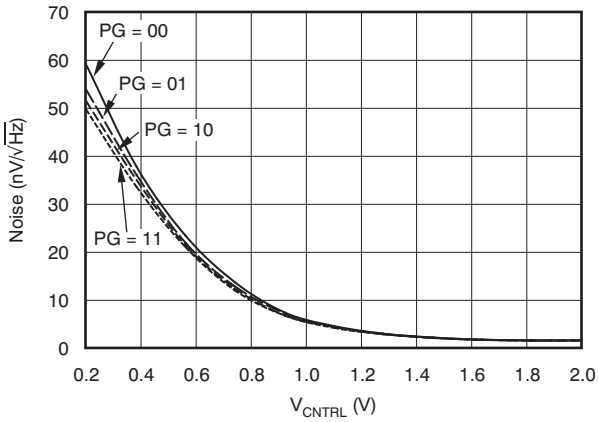


Figure 27.

NOISE FIGURE vs V_{CNTRL} (ATN = 11, f_{IN} = 2MHz)

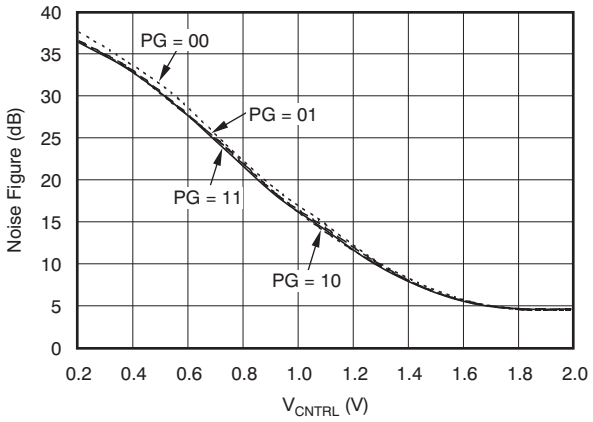


Figure 28.

NOISE FIGURE vs V_{CNTRL} (ATN = 11, f_{IN} = 5MHz)

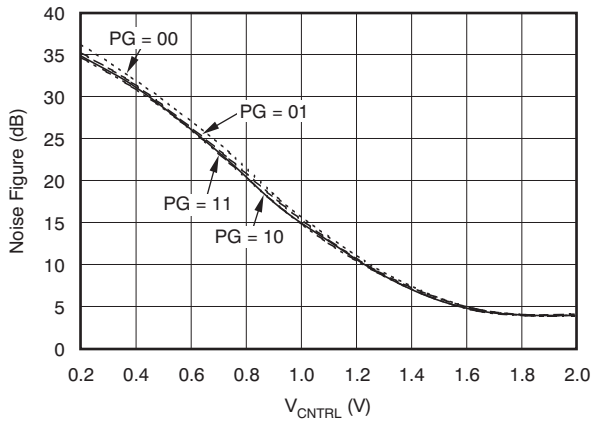


Figure 29.

INPUT-REFERRED NOISE (2MHz, 2V V_{CNTRL})

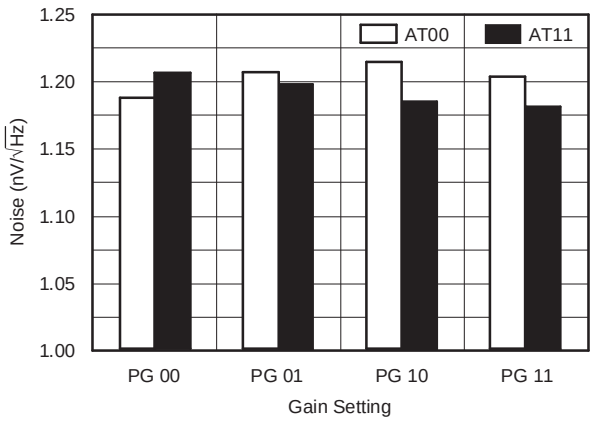


Figure 30.

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TYPICAL CHARACTERISTICS: AV_{DD} = DV_{DD} = 3V (continued)

At T_A = +25°C, load resistance = 1kΩ on each output to ground; the input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

INPUT-REFERRED NOISE (5MHz, 2V V_{CNTRL})

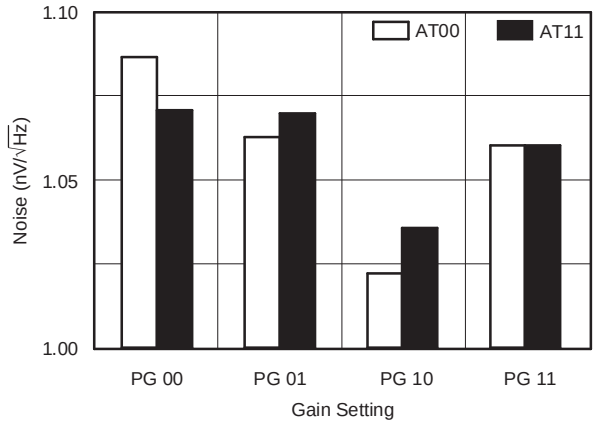


Figure 31.

INPUT-REFERRED NOISE (CW Output)

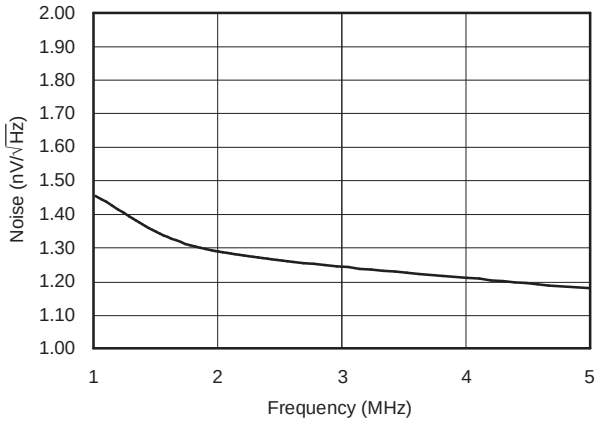


Figure 32.

DISTORTION vs FREQUENCY (ATN = 00, PG = 00, V_{CNTL} = 2.0V)

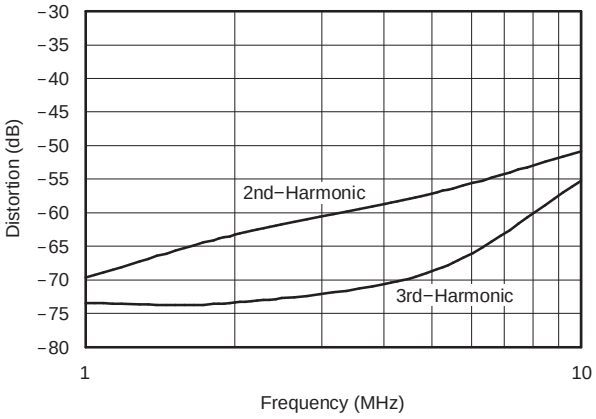


Figure 33.

DISTORTION vs FREQUENCY (ATN = 00, PG = 01, V_{CNTL} = 2.0V)

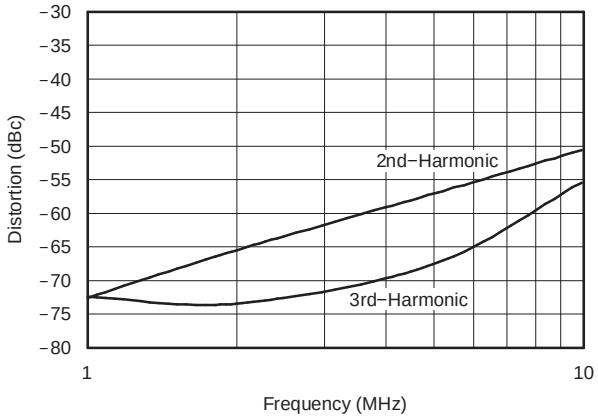


Figure 34.

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TYPICAL CHARACTERISTICS: AV_{DD} = DV_{DD} = 3V (continued)

At T_A = +25°C, load resistance = 1kΩ on each output to ground; the input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

DISTORTION vs FREQUENCY
(ATN = 00, PG = 10, V_{CNTL} = 2.0V)

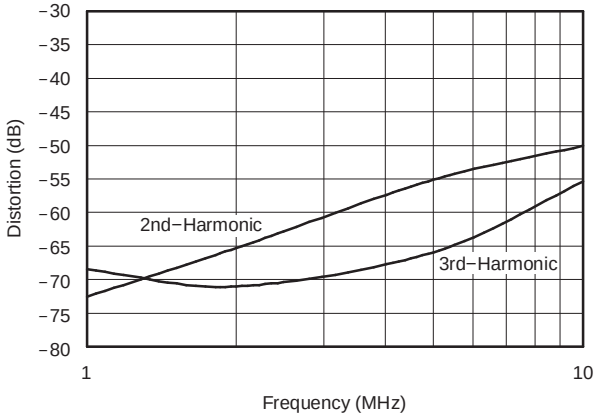


Figure 35.

DISTORTION vs FREQUENCY
(ATN = 00, PG = 11, V_{CNTL} = 2.0V)

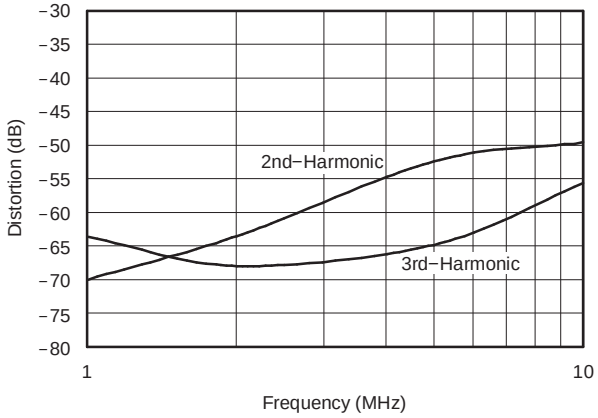


Figure 36.

DISTORTION vs V_{CNTRL}
(ATN = 00, PG = 10, f_{IN} = 2MHz, 750mV_{PP})

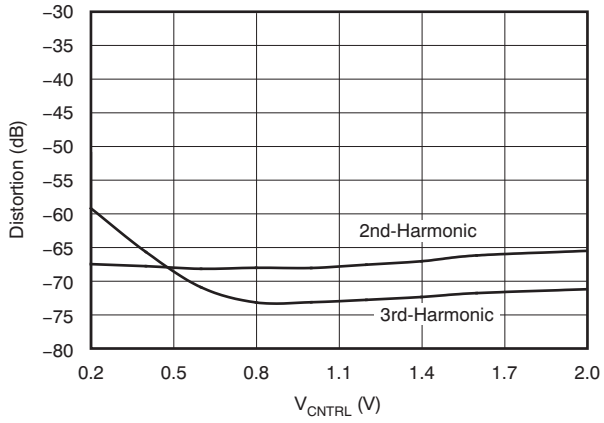


Figure 37.

DISTORTION vs V_{CNTRL}
(ATN = 01, PG = 10, f_{IN} = 2MHz, 750mV_{PP})

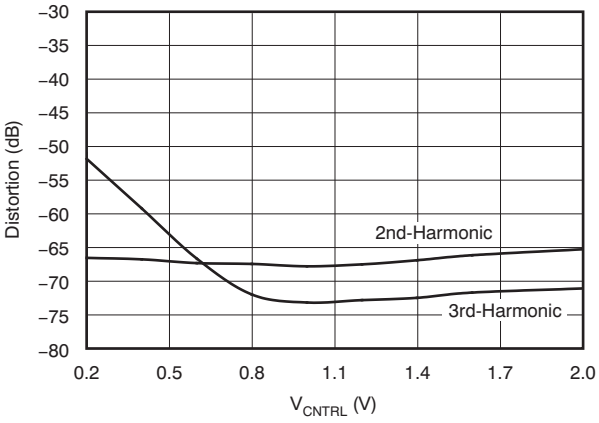


Figure 38.

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TYPICAL CHARACTERISTICS: AV_{DD} = DV_{DD} = 3V (continued)

At T_A = +25°C, load resistance = 1kΩ on each output to ground; the input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

DISTORTION vs V_{CNTRL}
(ATN = 10, PG = 10, f_{IN} = 2MHz, 750mV_{PP})

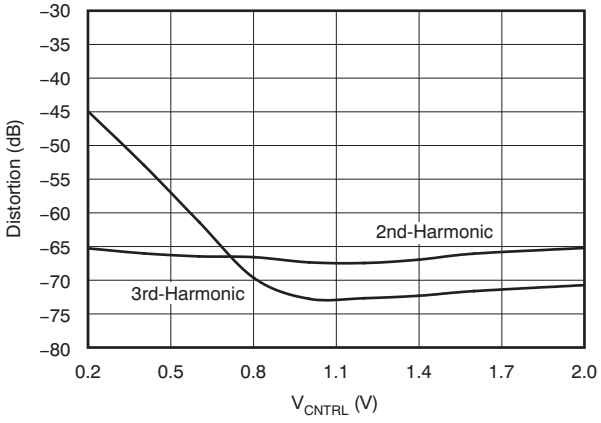


Figure 39.

DISTORTION vs V_{CNTRL}
(ATN = 11, PG = 10, f_{IN} = 2MHz, 750mV_{PP})

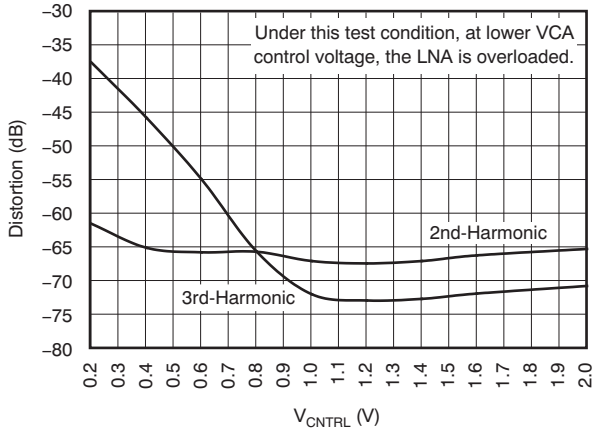


Figure 40.

DISTORTION vs V_{CNTRL}
(ATN = 00, PG = 00, 500mV_{PP}, 2nd-Harmonic)

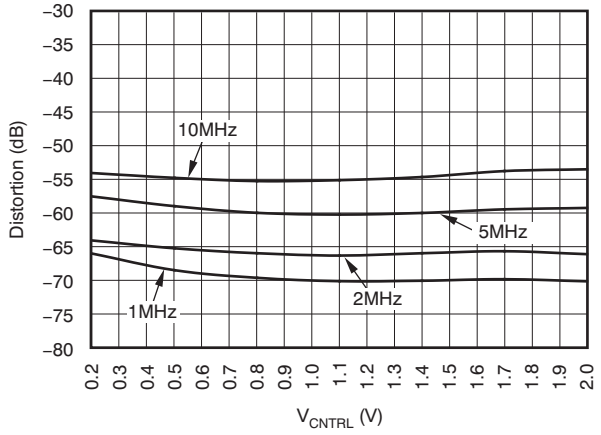


Figure 41.

DISTORTION vs V_{CNTRL}
(ATN = 00, PG = 01, 500mV_{PP}, 2nd-Harmonic)

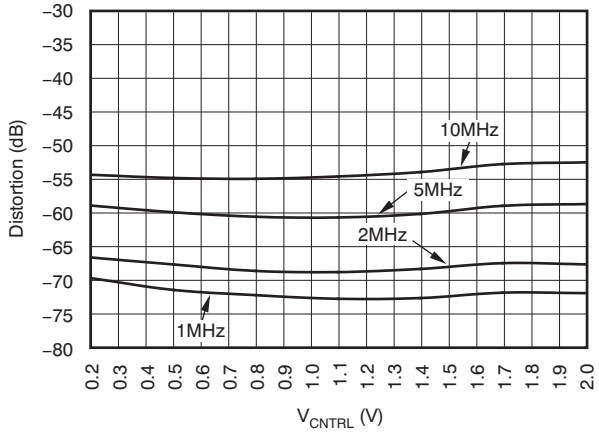


Figure 42.

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TYPICAL CHARACTERISTICS: AV_{DD} = DV_{DD} = 3V (continued)

At T_A = +25°C, load resistance = 1kΩ on each output to ground; the input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

DISTORTION vs V_{CNTRL}
(ATN = 00, PG = 10, 500mV_{PP}, 2nd-Harmonic)

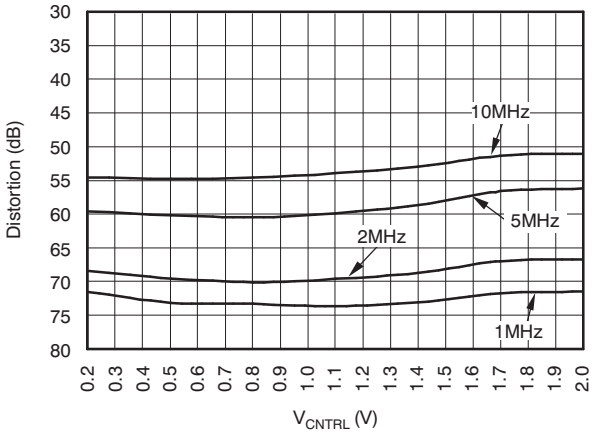


Figure 43.

DISTORTION vs V_{CNTRL}
(ATN = 00, PG = 10, 500mV_{PP}, 2nd-Harmonic)

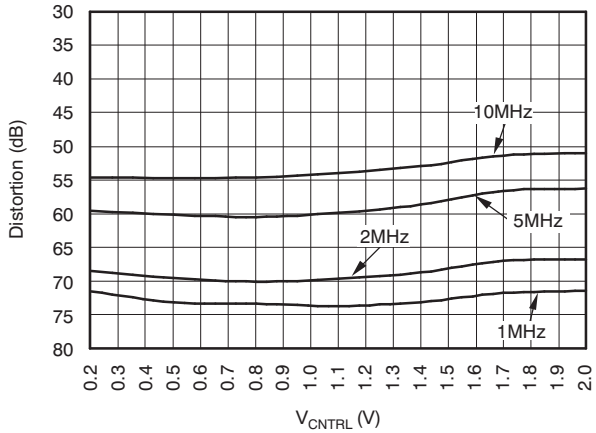


Figure 44.

DISTORTION vs V_{CNTRL}
(ATN = 00, PG = 00, 500mV_{PP}, 3rd-Harmonic)

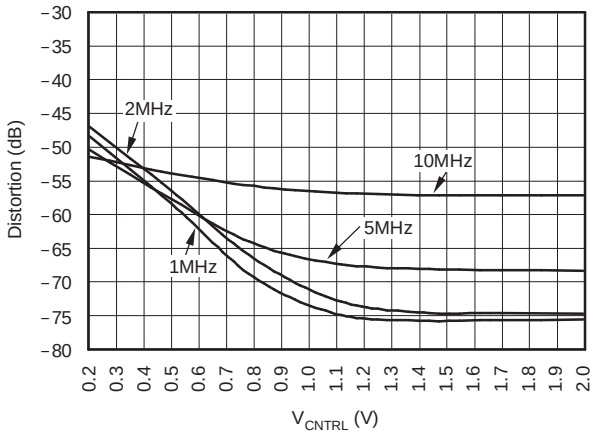


Figure 45.

DISTORTION vs V_{CNTRL}
(ATN = 00, PG = 01, 500mV_{PP}, 3rd-Harmonic)

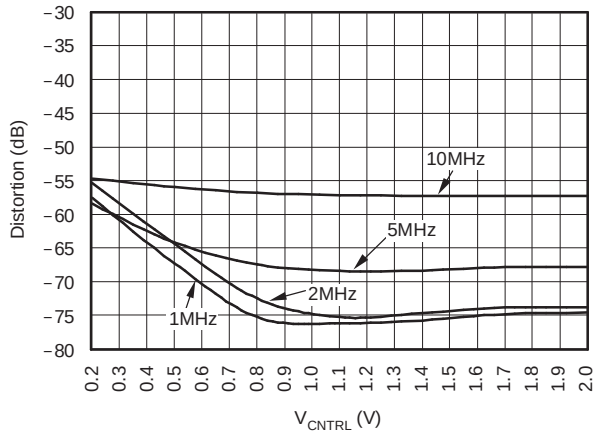


Figure 46.

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TYPICAL CHARACTERISTICS: AV_{DD} = DV_{DD} = 3V (continued)

At T_A = +25°C, load resistance = 1kΩ on each output to ground; the input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

DISTORTION vs V_{CNTRL}
(ATN = 00, PG = 10, 500mV_{PP}, 3rd-Harmonic)

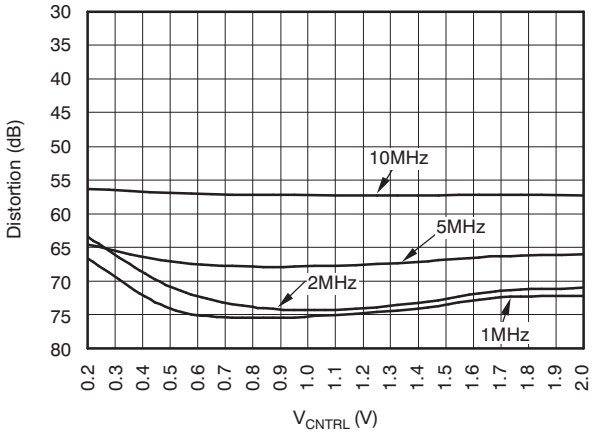


Figure 47.

DISTORTION vs V_{CNTRL}
(ATN = 00, PG = 11, 500mV_{PP}, 3rd-Harmonic)

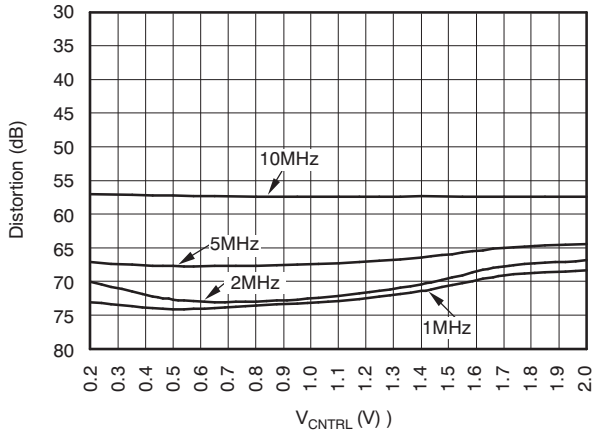


Figure 48.

CROSSTALK vs V_{CNTRL}
(ATN = 00, f_{IN} = 2MHz, CH4 to CH5)

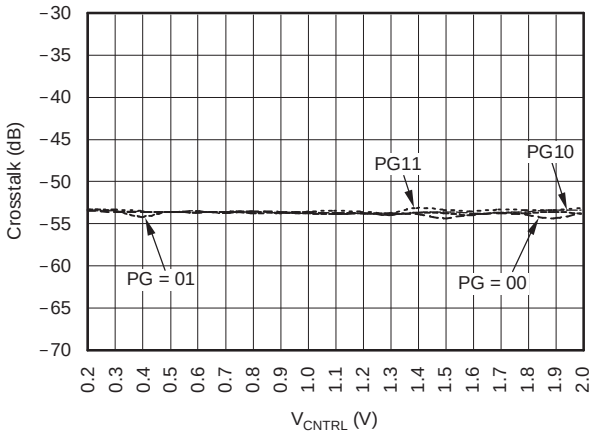


Figure 49.

CROSSTALK vs V_{CNTRL}
(ATN = 00, f_{IN} = 5MHz, CH4 to CH5)

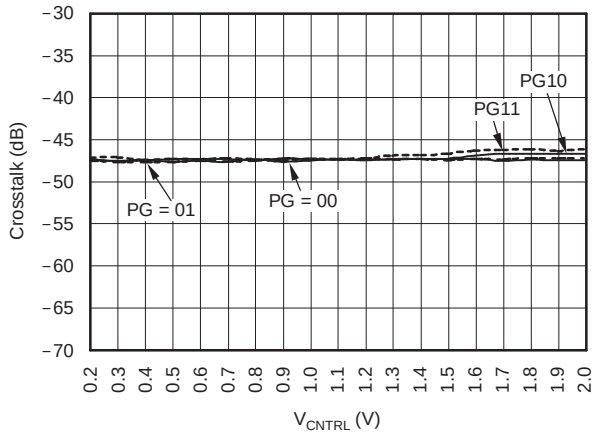


Figure 50.

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TYPICAL CHARACTERISTICS: AV_{DD} = DV_{DD} = 3V (continued)

At T_A = +25°C, load resistance = 1kΩ on each output to ground; the input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

CROSSTALK vs V_{CNTRL} (ATN = 00, f_{IN} = 10MHz, CH4 to CH5)

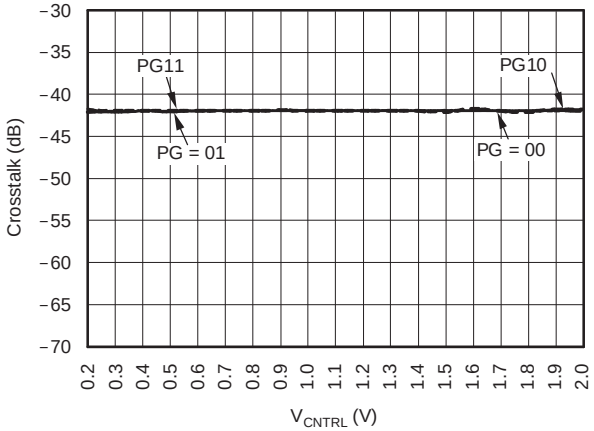


Figure 51.

CROSSTALK to V_{CNTRL} (ATN = 11, PG = 11, CH4 to CH5)

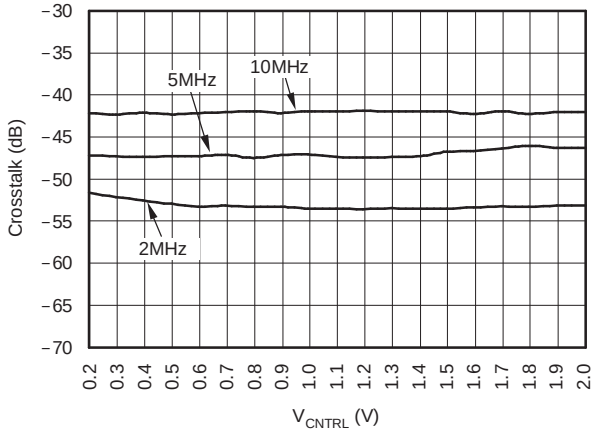


Figure 52.

CROSSTALK to V_{CNTRL}; CH1 vs CHn (at 5MHz, AT = 00, PG = 00)

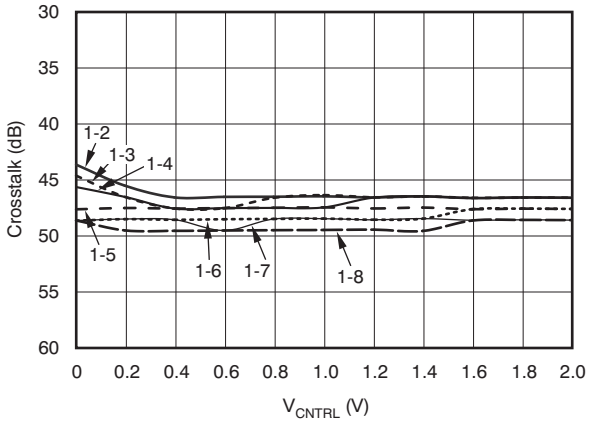


Figure 53.

CROSSTALK to V_{CNTRL}; CH1 vs CHn (at 5MHz, AT = 11, PG = 00)

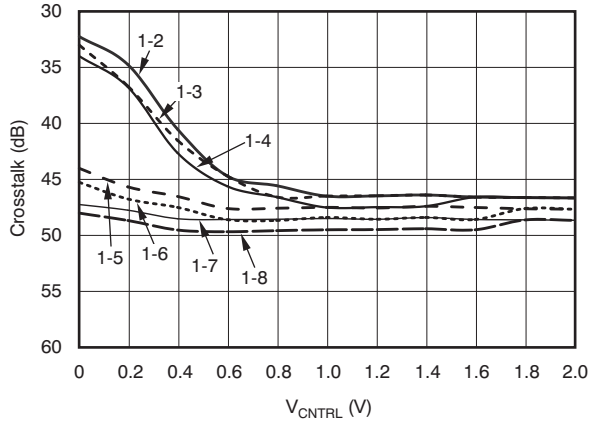


Figure 54.

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TYPICAL CHARACTERISTICS: $AV_{DD} = DV_{DD} = 3V$ (continued)

At T_A = +25°C, load resistance = 1kΩ on each output to ground; the input to the preamp (LNA) is single-ended; pre-amp gain is fixed at +20dB, f_{IN} = 2MHz, PG = 01, ATN = 00, and the output from the VCA is differential, unless otherwise noted.

CROSSTALK to V_{CNTRL}; CH1 vs CHn (at 5MHz, AT = 00, PG = 11)

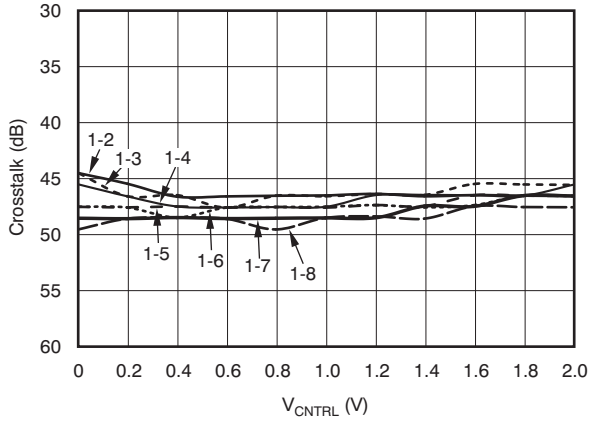


Figure 55.

CROSSTALK to V_{CNTRL}; CH1 vs CHn (at 5MHz, AT = 11, PG = 11)

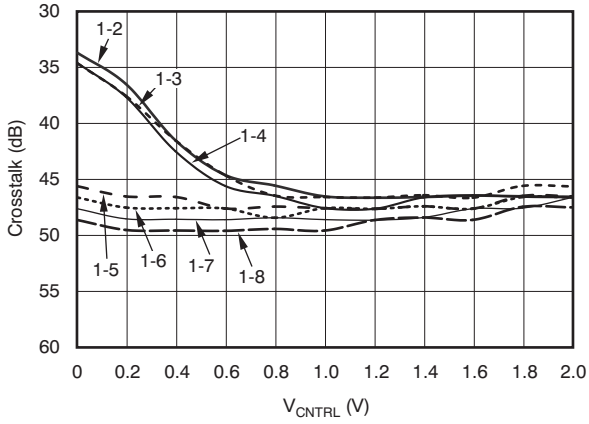


Figure 56.

INPUT IMPEDANCE

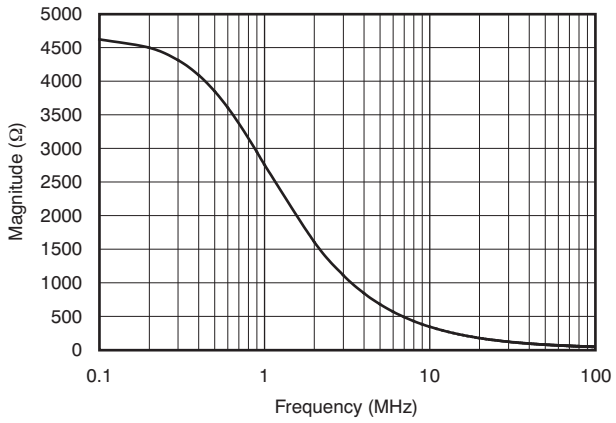


Figure 57.

INPUT IMPEDANCE

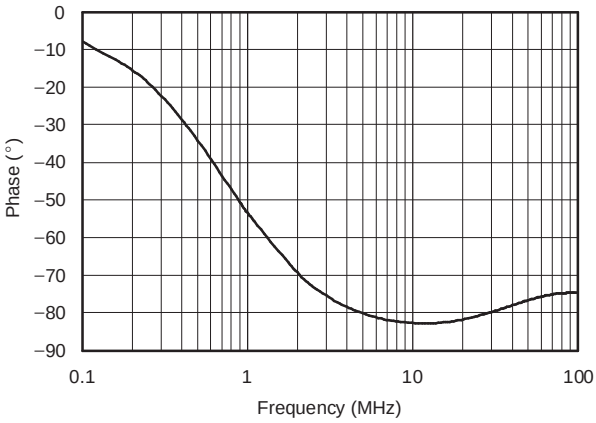


Figure 58.

OVERLOAD RECOVERY vs TIME (ATN = 00, PG = 00, V_{CNTRL} = 1V)

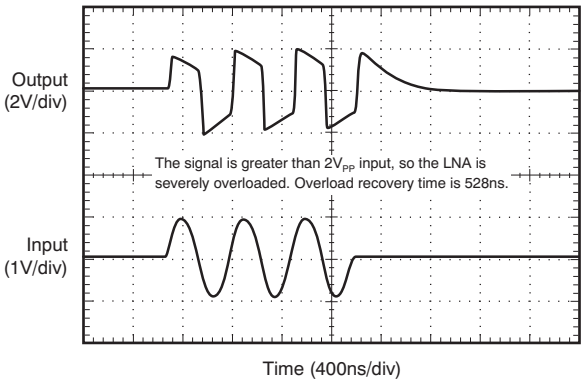


Figure 59.

OVERLOAD RECOVERY vs TIME (ATN = 00, PG = 01, V_{CNTRL} = 2V)

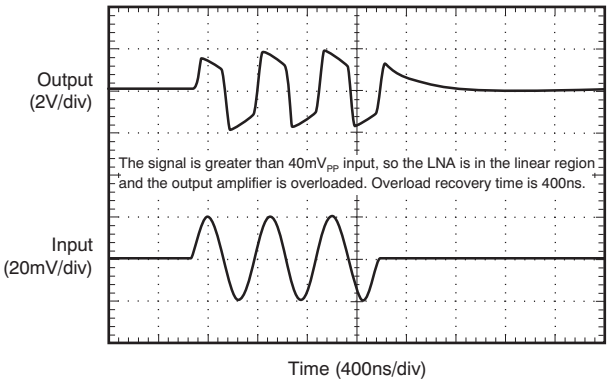


Figure 60.

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APPLICATION INFORMATION

NOTE: For current users of the VCA8613 who are switching to the VCA8617, pin 32 of the VCA8617 is a V_{DD} reference pin and requires a minimum 0.1µF bypass capacitor to ground.

INPUT CIRCUIT

The input of the VCA8617 integrates several commonly-used elements. Before reaching the input of the LNA, the receive signal should be coupled with a capacitor of at least 10nF (preferably more). When this ac-coupling element is inserted, the LNA input bias point is held to a common-mode value of 1.4V by an integrated 4.5kΩ resistor. This common-mode value changes with temperature and may also vary from chip to chip, but for each chip, it will be held constant. Two back-to-back clipping diodes are in parallel with this resistor. These diodes prevent excessive input voltages from passing through to the LNA input, preventing deep saturation effects in the LNA itself. These integrated diodes are designed to handle a dc-current of up to about 10mA. If the application requires improved overload protection, external Schottky diodes, such as the BAS40 series by Infineon, should be considered.

LOW-NOISE PRE-AMPLIFIER (LNA)

The VCA8617 integrates a low-noise pre-amplifier. Because of the high level of integration in the system, noise performance was traded for power consumption, resulting in an extremely low-power pre-amplifier, with 0.8nV/√Hz noise performance at 5MHz. The LNA is configured as a fixed-gain 20dB amplifier. Of this total gain, 6dB results from the single-ended to differential conversion accomplished within the LNA itself. The output of the LNA is limited to a little over $2V_{PP}$ differential swing. This implies a maximum input voltage swing of approximately $200mV_{PP}$ to be operating in the linear range at 5MHz. Larger input signals can be accepted by the LNA, but distortion performance will degrade with larger input signals.

CW DOPPLER PROCESSOR

The VCA8617 integrates many of the elements necessary to allow for the implementation of a simple CW Doppler processing circuit. One circuit that was integrated was a V/I converter following the LNA, as shown in Figure 61. The V/I converter converts the differential LNA voltage output to a current, which is then passed through an 8x10 switch matrix (see Figure 62). Within this switch matrix, any of the eight LNA outputs can be connected to any of 10 CW output pins. This example is a simple current-summing circuit, such that each CW output can represent the sum of any or all the channel currents. The transconductance of the V/I converter is approximately 20mA/V relative to the LNA input. For proper operation of the CW Doppler Processor, it is mandatory to have a bias voltage on the output/outputs that are selected (see Figure 63).

The CW output common-mode is 1.4V.

The CW outputs are typically routed to a passive delay line, allowing coherent summing of the signals. After summing, IQ separation and down conversion to baseband precedes a pair of high-resolution, low sample rate ADCs.

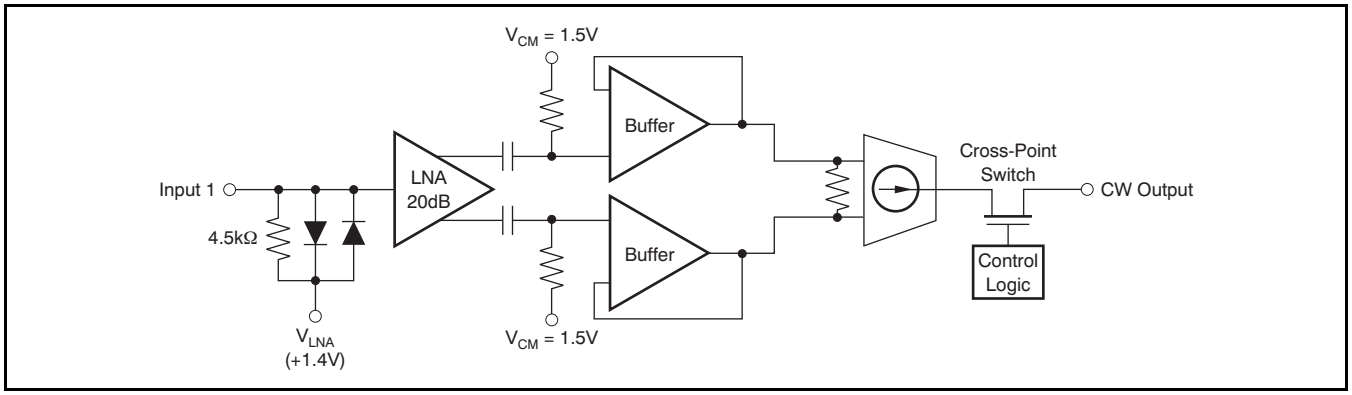


Figure 61. Basic CW Processing Block Diagram

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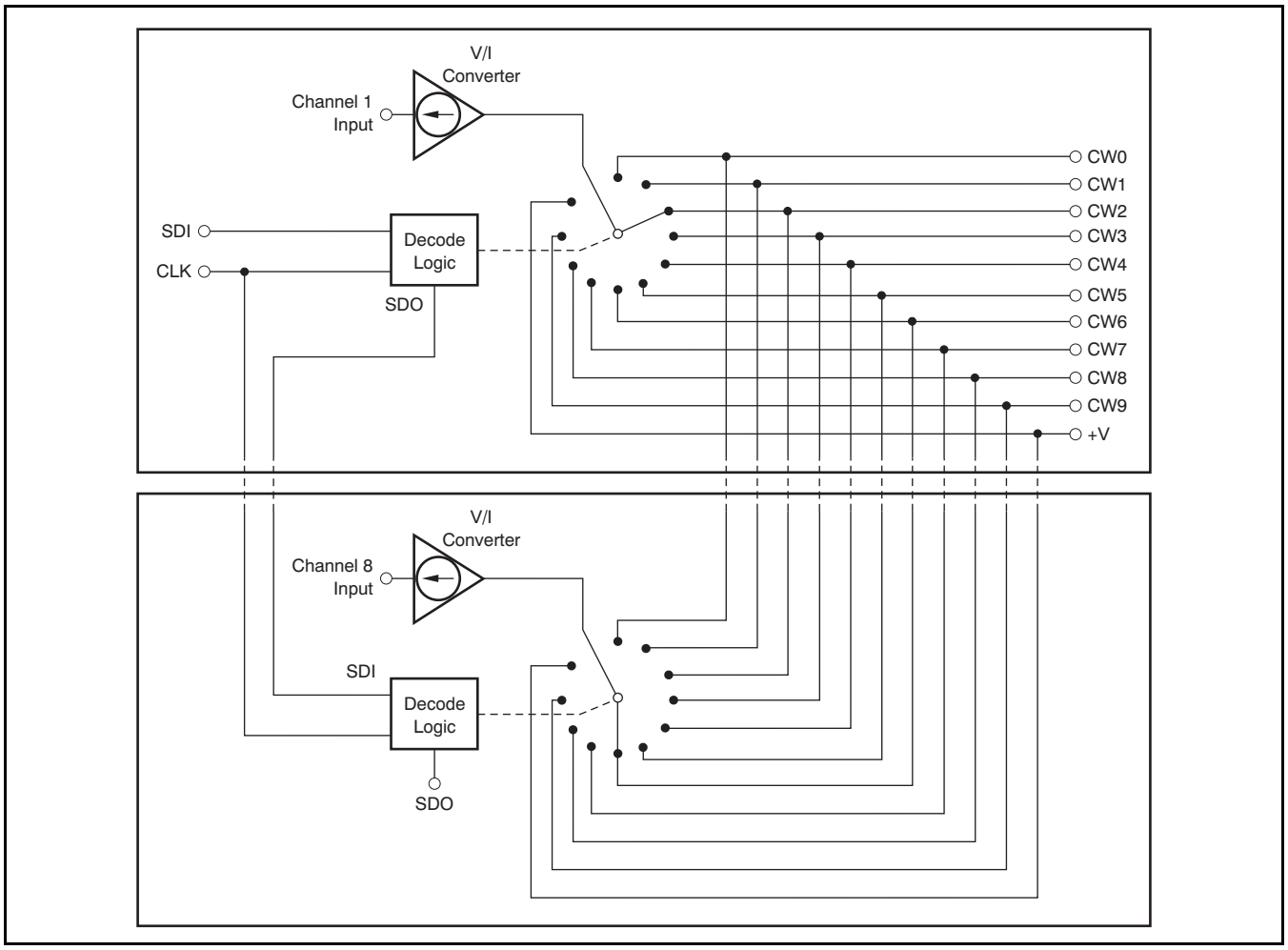


Figure 62. Basic CW Cross-Point Switch Matrix for All Eight Channels

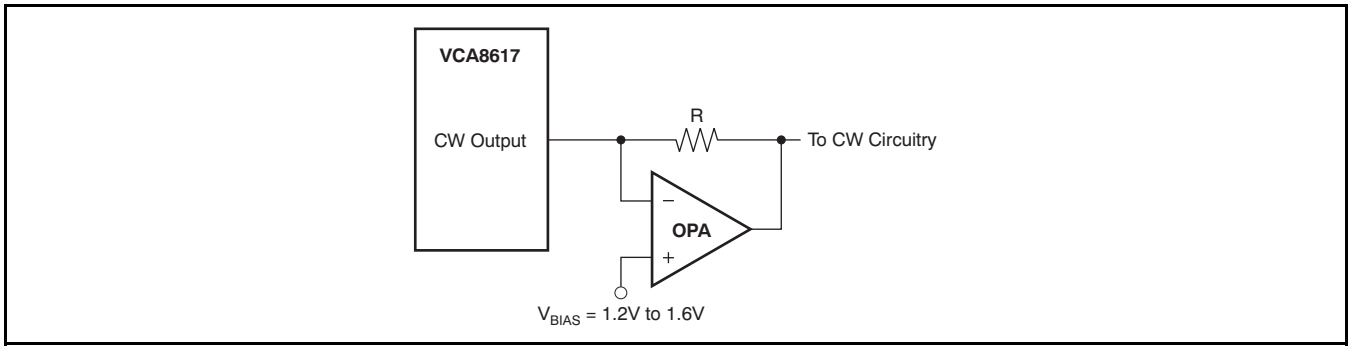


Figure 63. Operational Amplifier

VOLTAGE-CONTROLLED ATTENUATOR (VCA)—DETAIL

The VCA is designed to have a dB-linear attenuation characteristic; that is, the gain loss in dB is constant for each equal increment of the V_{CNTRL} control voltage. Figure 64 shows a block diagram of the VCA. The attenuator is essentially a variable voltage divider consisting of one series input resistor, R_S, and 10 identical shunt FETs, placed in parallel and controlled by sequentially-activated clipping amplifiers. Each clipping amplifier can be thought of as a specialized voltage comparator with a soft transfer characteristic and well-controlled output limit voltages. The reference voltages V1 through V10 are equally spaced over the 0V to 2.0V control voltage range. As the control voltage rises through the input range of each clipping amplifier, the amplifier output will rise from 0V (FET completely ON) to $V_{CM} – V_T$ (FET nearly OFF), where V_{CM} is the common source voltage and V_T is the threshold voltage of the FET. As each FET approaches its OFF state and the control voltage continues to rise, the next clipping amplifier/FET combination takes over for the next portion of the piecewise-linear attenuation characteristic. Thus, low control voltages have most of the FETs turned ON, while high control voltages have most turned OFF. Each FET acts to decrease the shunt resistance of the voltage divider formed by R_S and the parallel FET network.

The attenuator is comprised of two sections, with five parallel clipping amplifier/FET combinations in each. Special reference circuitry is provided so that the $(V_{CM} − V_T)$ limit voltage will track temperature and IC process variations, minimizing the effects on the attenuator control characteristic.

In addition to the analog VCA_{CNTRL} gain setting input, the attenuator architecture provides digitally-programmable adjustment in four steps, via the two attenuation bits. These bits adjust the maximum achievable gain (corresponding to minimum attenuation in the VCA, with V_{CNTRL} = 2.0V) in 5dB increments. This function is accomplished by providing multiple FET sub-elements for each of the Q_1 to Q_{10} FET shunt elements (see Figure 65). In the simplified diagram of Figure 64, each shunt FET is shown as two sub-elements, Q_{NA} and Q_{NB}. Selector switches, driven by the MGS bits, activate either or both of the sub-element FETs to adjust the maximum R_{ON} and thus achieve the stepped attenuation options.

The VCA can be used to process either differential or single-ended signals. Fully differential operation will reduce 2nd-harmonic distortion by about 10dB for full-scale signals.

Input impedance of the VCA varies with gain setting, because of the changing resistances of the programmable voltage divider structure. At large attenuation factors (that is, low gain settings), the impedance will approach the series resistor value of approximately 120Ω.

As with the LNA stage, the VCA output is ac-coupled into the PGA. This ac-coupling means that the attenuation-dependent dc common-mode voltage will not propagate into the PGA, and so the PGA dc output level will remain constant.

Finally, note that the VCA_{CNTRL} input consists of FET gate inputs. This architecture provides very high impedance and ensures that multiple VCA8617 devices may be connected in parallel with no significant loading effects. The nominal voltage range for the V_{CNTRL} input spans from 0V to 2.0V. Overdriving this input (greater than 3V) does not affect the performance.

PGA POST-AMPLIFIER

See Figure 66 for a simplified circuit diagram of the PGA. PGA gain is programmed through the serial port, and can be configured to 24 different gain settings of 25dB, 30dB, 35dB, and 40dB, as shown in Table 9. A patented circuit has been implemented in the PGA that allows for exceptional overload signal recovery.

Table 9. PGA Gain Settings

PG1, PG0	GAIN
0, 0	25dB
0, 1	30dB
1, 0	35dB
1, 1	40dB

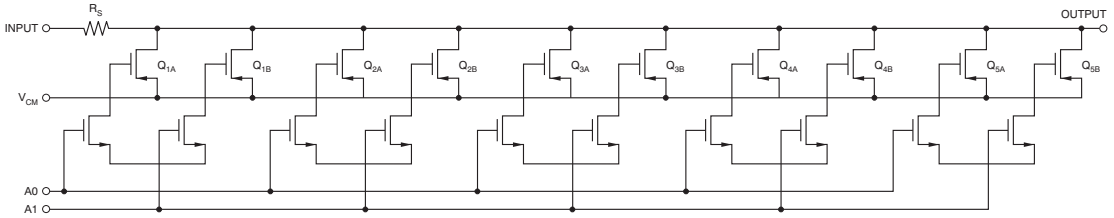


Figure 64. Programmable Attenuator Section

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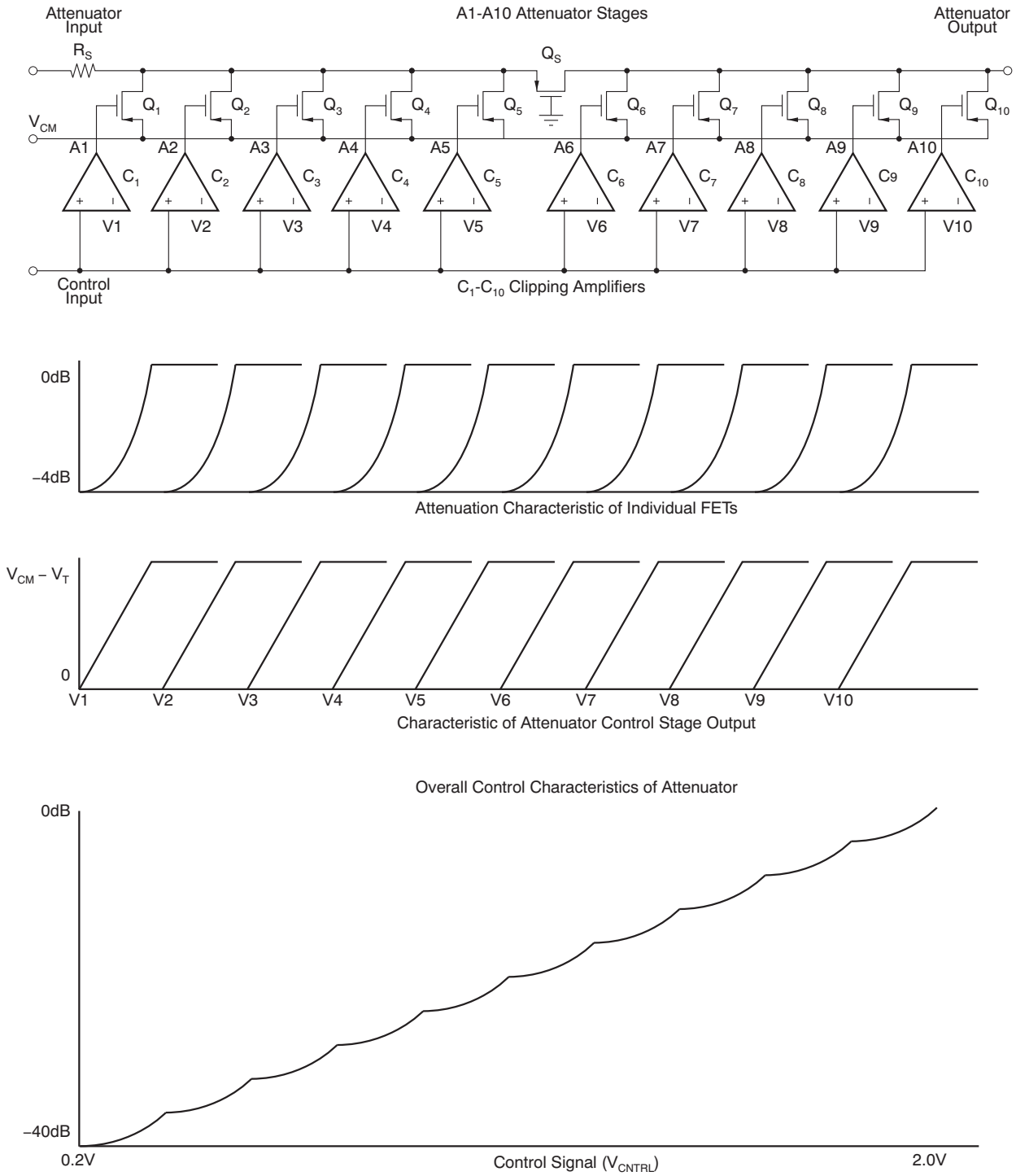


Figure 65. Piecewise Approximation to Logarithmic Control Characteristics

OUTPUT FILTER

The VCA8617 integrates an almost three-pole, 15MHz low-pass Butterworth filter in the output stage. The cutoff frequency is implemented with passive semiconductor elements and as such, the cutoff frequency will not be precise. The output pins of the VCA8617, as shown in Figure 66, nominally sit at approximately $1.5V_{DC}$. However, this dc voltage varies slightly over PG gain settings as well as from chip to chip as a result of process variations. For users who cannot tolerate this slight variation, an ac coupling capacitor is recommended between the VCA outputs and the ADC inputs. The smaller the value of this capacitor, the better, because it reduces the pulse signal settling time. For the typical performance charts in this data sheet, a 560pF capacitor was used.

SERIAL INTERFACE

The serial interface of the VCA8617 allows flexibility in the use of the part. The following parameters are set from the serial control registers:

- Mode
  - TGC mode
  - CW mode
- Attenuation range
- PGA gain
- Power-down (this is the default state in which the VCA8617 initializes)
- CW output selection for each input channel

The serial interface uses an SPI™ style of interface format. The Input Register Bit Maps show the functionality of each control register.

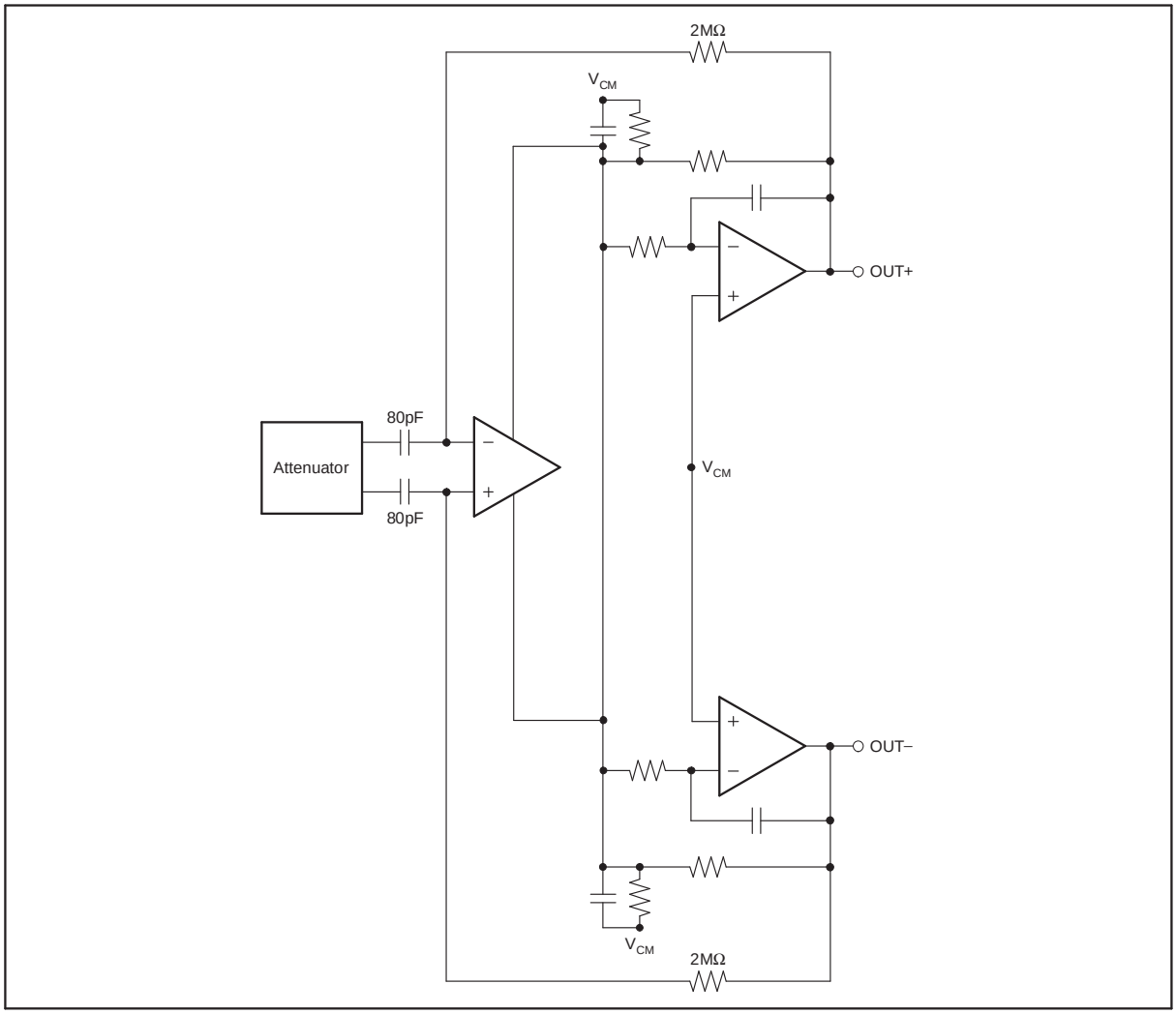


Figure 66. Simplified PGA and Output Filter Circuit

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LAYOUT CONSIDERATIONS

The VCA8617 is a multi-channel amplifier with integrated digital controls, capable of high gains. Layout of the VCA8617 is fairly straightforward. By connecting all of the grounds (including the digital grounds) to the analog ground, noise performance can be maintained.

The analog ground should be a solid plane. Power-supply decoupling and decoupling of the control voltage (V_{CNTRL}) pin are essential in order to ensure that the noise performance be maintained. For further help in determining basic values, refer to Figure 67.

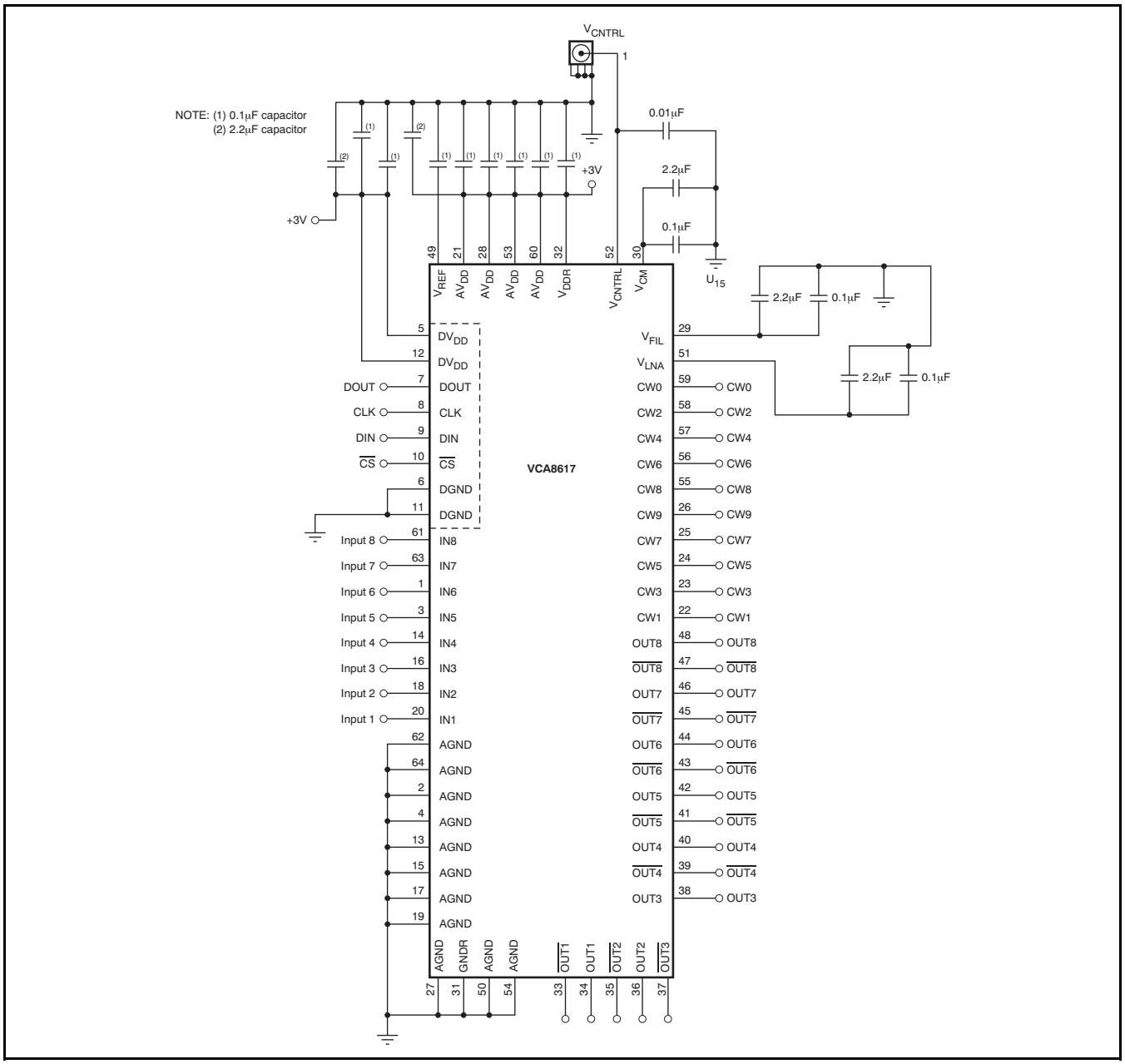


Figure 67. Basic Connection Diagram

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (November, 2007) to Revision F **Page**

- Corrected y-axis labels for Figure 59 23
- Corrected y-axis labels for Figure 60 23

Changes from Revision D (May, 2005) to Revision E **Page**

- Changed "100mW/channel" feature to "103mW/channel" 1
- Changed Electrical Characteristics measured voltage; included DV_{DD} 3
- Added Input Common-Mode Voltage specification 3
- Changed Input Voltage Range typical specification from 20V to 2.0V 3
- Changed Electrical Characteristics measured voltage; included DV_{DD} 4
- Replaced Figure 22 14
- Replaced Figure 23 15
- Replaced Figure 28 16
- Replaced Figure 29 16
- Replaced Figure 43 20
- Replaced Figure 44 20
- Replaced Figure 47 21
- Replaced Figure 48 21
- Revised Application Information Section 24

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VCA8617PAGR	ACTIVE	TQFP	PAG	64	1500	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	VCA8617	Samples
VCA8617PAGT	ACTIVE	TQFP	PAG	64	250	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	VCA8617	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

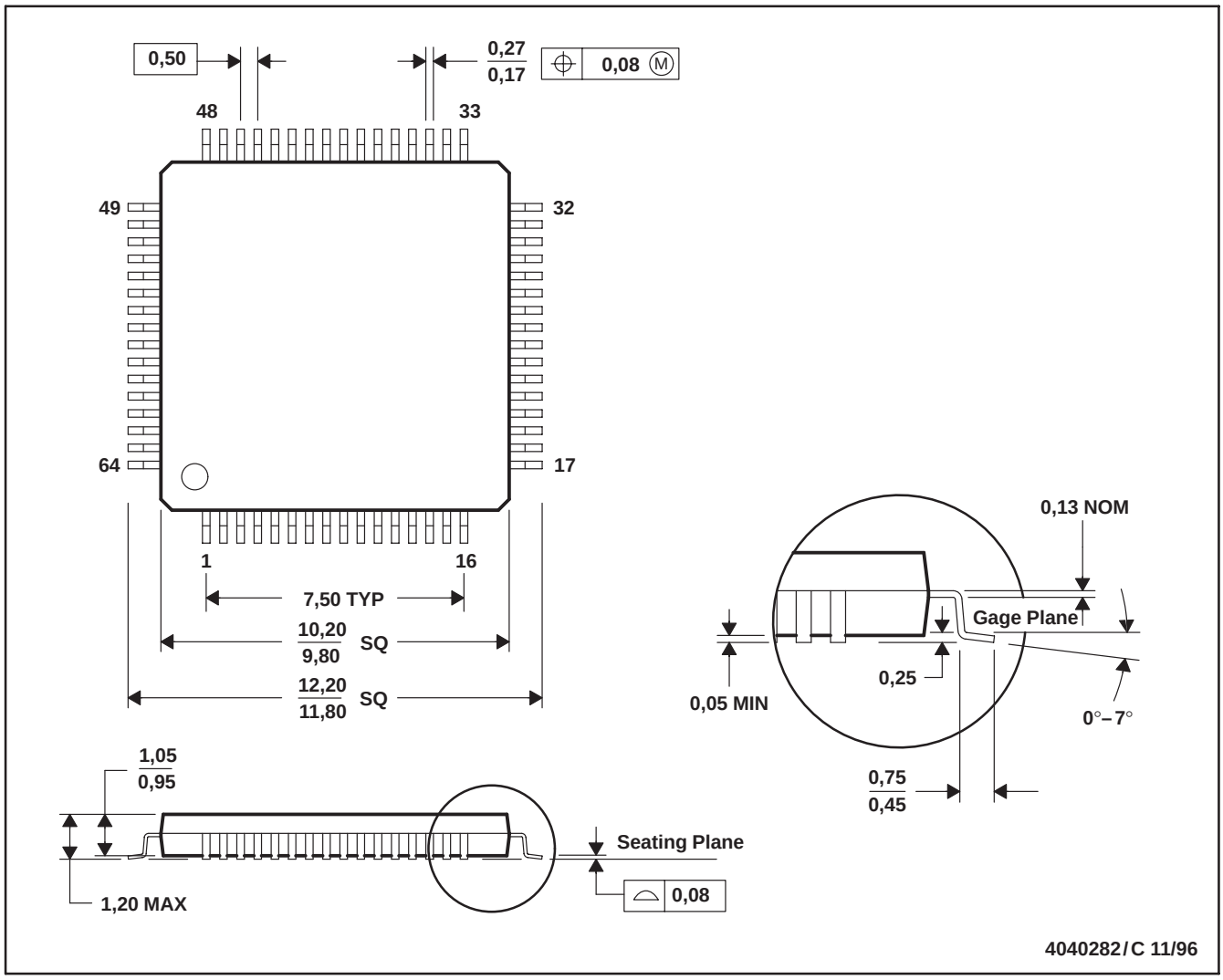
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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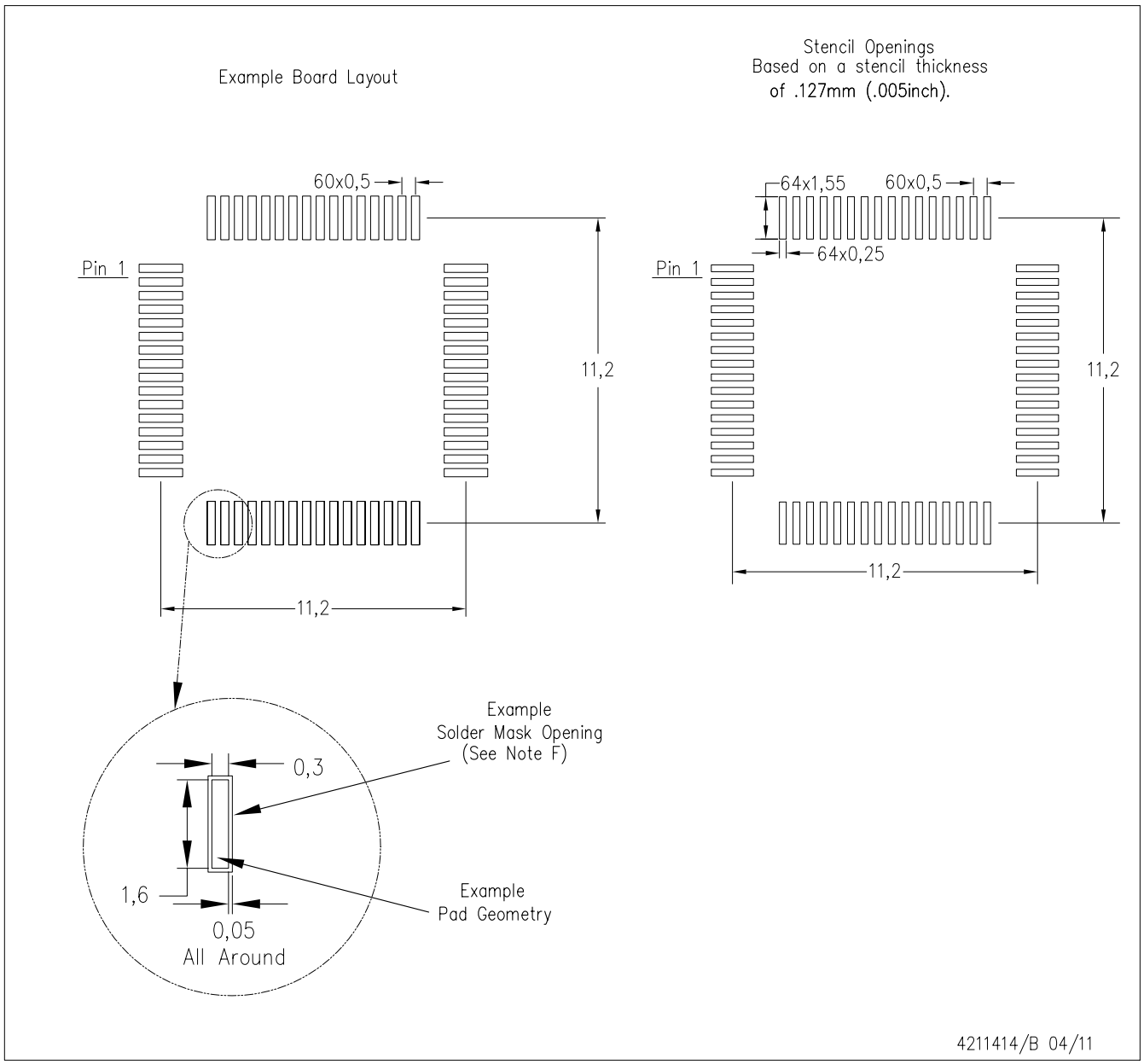
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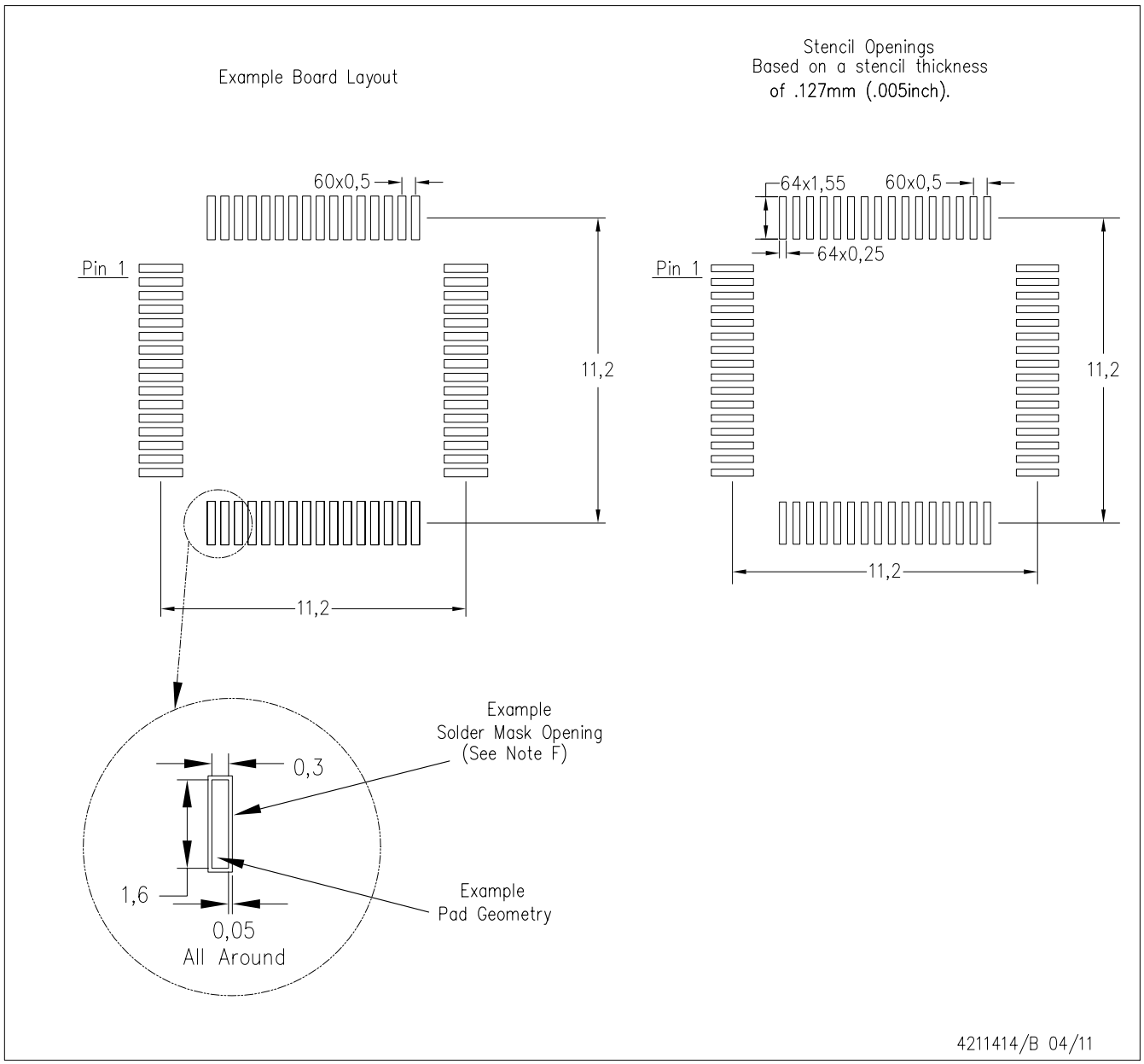
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D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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