FAIRCHILD SEMICONDUCTOR®

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100ELT23
5V Dual Differential PECL to TTL Translator (Preliminary)

General Description

The 100ELT23 is a dual differential PECL to TTL translator operating from a single +5V supply.

The dual gate design of the 100ELT23 makes it ideal for applications which require the translation of a clock and a data signal.

The 100 series is temperature compensated.

Features

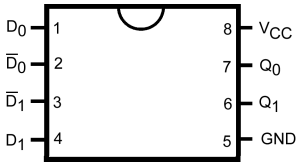
- Typical propagation delay of 3.5 ns
- TTL output drive: I_{OH} = 24 mA; I_{OL} = –3 mA
- Flow through pinout
- Q Output will default to a LOW with the inputs left Open
- Internal pull-down resistors on inputs
- Fairchild MSOP-8 package is a drop-in replacement to ON TSSOP-8
- Typical I_{CCH} of 23 mA, I_{CCL} of 26 mA
- Meets or exceeds JEDEC specification EIA/JESD78 IC latch-up test
- Moisture Sensitivity Level TBD
- ESD Performance:
  Human Body Model > TBD
  Machine Model > TBD

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description
100ELT23M	M08A	KLT23	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
100ELT23M8 (Preliminary)	MA08D	KT23	8-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide

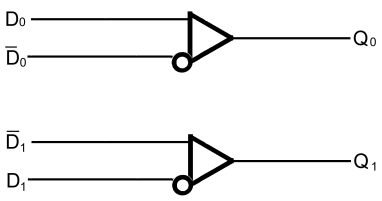
Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Top View

Logic Diagram



Pin Descriptions

Pin Name	Description
D_0, $\overline{D}_0$, D_1, $\overline{D}_1$	PECL Differential Inputs
Q_0, Q_1	TTL Outputs
V_{CC}	Positive Supply
GND	Ground

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Absolute Maximum Ratings(Note 1)

PECL Supply Voltage (V_{CC})	0.0V to +7V
Input Voltage (V_I) $V_I \le V_{CC}$	0.0V to + 6V
Storage Temperature (T_{STG})	−65°C to + 150°C

Thermal Resistance

Junction to Ambient (θ_{JA})	SOIC	0LFPM	TBD
		500LFPM	TBD
Junction to Case (θ_{JC})	SOIC	std bd	TBD
Junction to Ambient (θ_{JA})	MSOP	0LFPM	TBD
		500LFPM	TBD
Junction to Case (θ_{JC})	MSOP	std bd	TBD

Recommended Operating Conditions

Power Supply Operating	V_{CC} = 4.75V to 5.25V
ECL Input Voltage	0.0V to V_{CC}
Free Air Operating Temperature (T_A)	−40°C to +85°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

PECL DC Electrical Characteristics V_{CC} = 5.0V; GND = 0.0V (Note 2)

Symbol	Parameter	−40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	2.2		5.0	2.2		5.0	2.2		5.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

Note 2: V_{IH} and V_{IL} values vary 1 to 1 with V_{CC}. V_{CC} can vary ±0.25V.

Note 3: V_{IHCMR} minimum varies 1 to 1 with GND. V_{IHCMR} maximum varies 1 to 1 with V_{CC}.

Note: Devices are designed to meet the DC specifications after thermal equilibrium has been established. Circuit is tested with air flow greater than 500LFPM maintained.

TTL DC Electrical Characteristics V_{CC} = 5.0V; GND = 0.0V (Note 4)

Symbol	Parameter	T_A = −40°C to 85°C			Units	Condition
		Min	Typ	Max		
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −3.0 mA
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 24 mA
I_{CCH}	Power Supply Current (Outputs set to HIGH)		23	33	mA	
I_{CCL}	Power Supply Current (Outputs set to LOW)		26	36	mA	
I_{OS}	Output Short Circuit Current (Note 5)	−150		−60	mA	

Note 4: V_{CC} can vary ±0.25V.

Note 5: For I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Note: Devices are designed to meet the DC specifications after thermal equilibrium has been established. Circuit is tested with air flow greater than 500LFPM maintained.

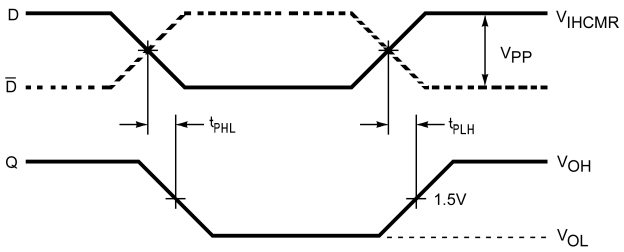
AC Electrical Characteristics V_{CC} = 5.0V; GND = 0.0V (Note 6)(Note 7)

Symbol	Parameter	−40°C			25°C			85°C			Units	Figure Number
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		MHz	
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps	
t_{PLH}, t_{PHL}	Propagation Delay to Output	2.0		5.5	2.0		5.5	2.0		5.5	ns	Figure 1
V_{PP}	Input Swing	200		1000	200		1000	200		1000	mV	Figure 1
t_r, t_f	Output Rise Time (10% to 90%)					1.6					ns	Figure 2
	Output Fall Time (10% to 90%)					1.1						

Note 6: V_{CC} can vary ±0.25V.

Note 7: All Loading with 500Ω to GND, C_L = 20 pF.

Switching Waveforms



Note: V_M varies 1:1 with V_{EE}

FIGURE 1. Differential PECL to TTL Output Propagation Delay

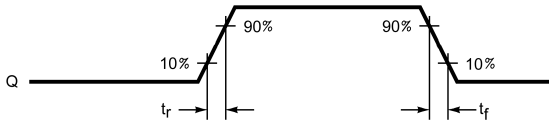
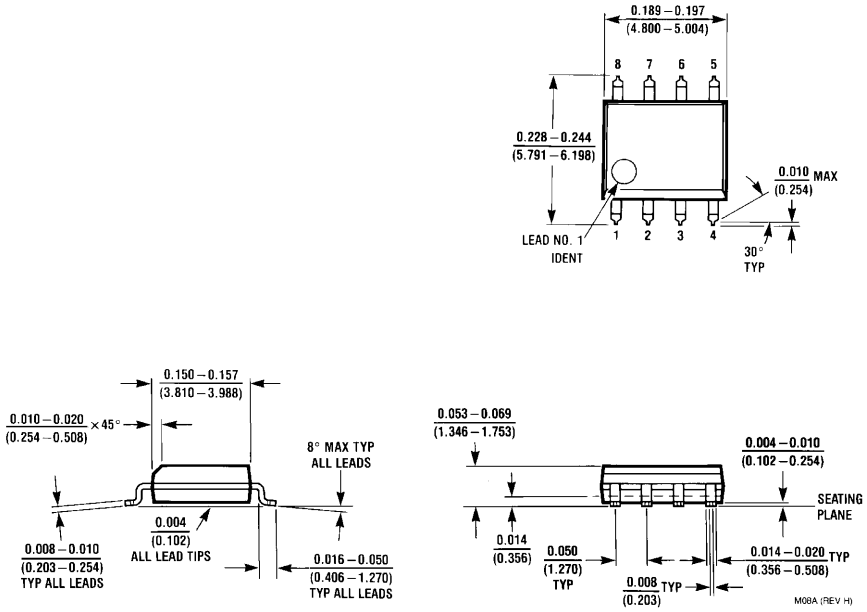


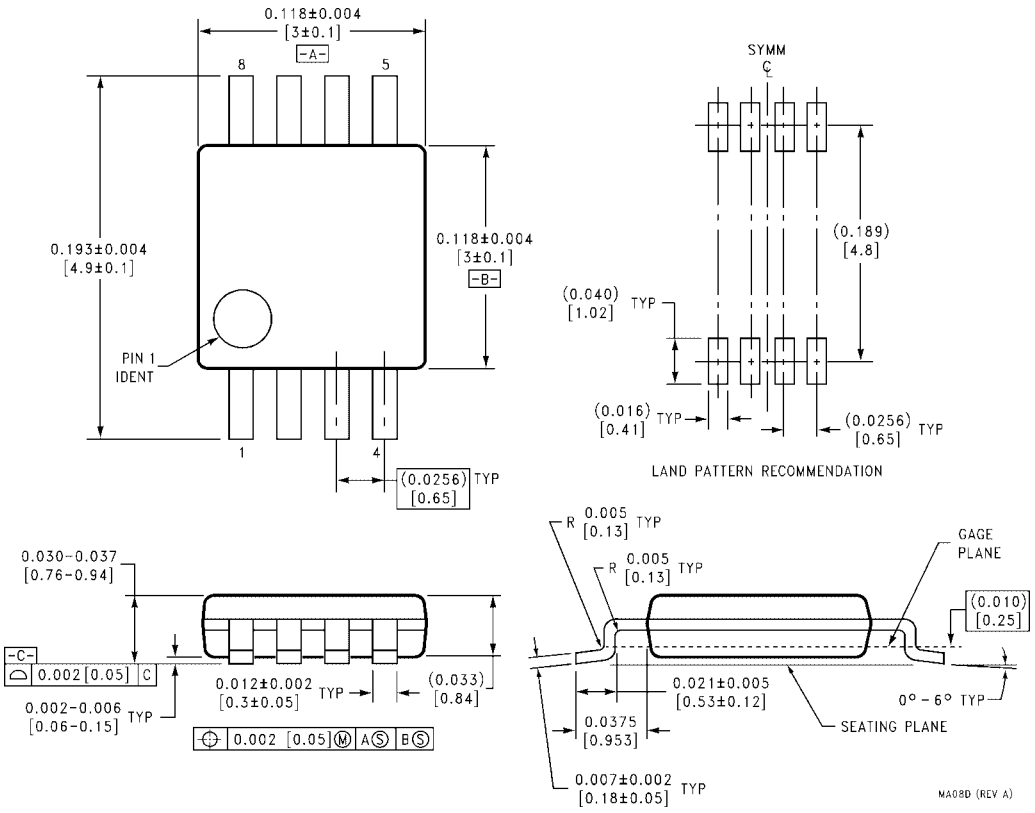
FIGURE 2. TTL Output Edge Rates

Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide
Package Number MA08D

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