

带有自动方向感测的 2 位双向电压电平转换器

查询样品: [TXB0302](#)

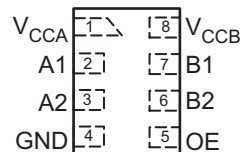
特性

- 完全对称电源电压
A 端口上 **0.9V 至 3.6V** 和 **0.9V 至 3.6V**
- **V_{CC}** 隔离特性—如果任何一个 **V_{CC}** 输入在接地 (**GND**) 上, 所有输出在高阻抗状态
- 以 **V_{CCA}** 为基准的输出使能 (**OE**) 输入电路
- 低功耗, 最大值 **5μA I_{CC}**
- **I_{off}** 支持部分断电模式运行
- 锁断性能超过 **100mA** (符合 **JESD 78 Class II** 规范的要求)
- 静电放电 (**ESD**) 保护性能超过 **JESD 22** 规范要求
 - **4000V** 人体模型 (**A114-A**)
 - **1000V** 充电器件模型 (**C101**)

说明

这个 2 位非反向转换器使用两个独立的可配置电源轨。A 端口被设计用于跟踪 **V_{CCA}**。V_{CCA} 接受从 0.9V 至 3.6V 间的任一电源电压值。B 端口设计用于跟踪 **V_{CCB}**。V_{CCB} 接受从 0.9V 至 3.6V 间的任一电源电压值。这可实现 1V, 1.2V, 1.5V, 1.8V, 2.5V 和 3.3V 电压节点间的低压双向转换。对于 TXB0302, 当输出使能端 (**OE**) 输入为低电平时, 所有输出均被置于高阻抗状态。为了确保加电或断电期间的高阻抗状态, **OE** 应该通过一个下拉电阻器接在 **GND** 上; 此电阻器的最小值由驱动器电流供源能力决定。TXB0302 被设计用于实现 **V_{CCA}** 对 **OE** 输入电路供电。该器件完全符合使用 **I_{关闭}** 的部分断电应用的规范要求。**I_{关闭}** 电路禁用输出, 从而可防止其断电时破坏性电流从该器件回流。

DQM 封装
(顶视图)



- 不需要在逻辑 I/O 的两侧都安装上拉电阻器。
- 如果需要上拉电阻器或者下拉电阻器的话, 电阻器的值必须超过 20kΩ。
- 20kΩ 是建议的安全值, 如果用户能够接受更高 **V_{ol}** 或者更低 **V_{oh}** 的话, 也允许使用电阻值更小的上拉或者下拉电阻器, 粗略的估算值为 **V_{ol}=V_{ccout} x 1.5k/(1.5k+R_{pu})**, 而 **V_{oh}=V_{ccout} x R_{dw}/(1.5k+R_{dw})**。
- 如果需要上拉电阻器, 请参考 **TXS0102** 或者与 **TI** 联系。
- 更多信息, 请参考应用注释 (文献号: [SCEA043](#))。

订购信息⁽¹⁾

T _A	封装 ⁽²⁾	可订购部件号	正面标记
-40°C 至 85°C	DQM – 微型四方扁平无引线 (MicroQFN)	TXB0302DQMR	77A

- (1) 要获得最新的封装和订货信息, 请参阅本文档末尾的封装选项附录, 或者登录 TI 的网站 [www.ti.com](#)。
- (2) 封装图样、热数据和符号可登录 [www.ti.com/packaging](#) 获取。



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TXB0302

ZHCS822B –MARCH 2012–REVISED OCTOBER 2012

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
DQM	TXB0302	
1	VCCA	A-port supply voltage $0.9\text{ V} \leq V_{CCA} \leq 3.6\text{ V}$
2	A1	Input/output 1. Referenced to V_{CCA} .
3	A2	Input/output 2. Referenced to V_{CCA} .
4	GND	Ground
5	OE	3-state output-mode enable. Pull OE (TXB0302) low to place all outputs in 3-state mode.
6	B2	Input/output 2. Referenced to V_{CCB} .
7	B1	Input/output 1. Referenced to V_{CCB} .
8	VCCB	B-port supply voltage $0.9\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	4.6	V
V_{CCB}			–0.5	4.6	
V_I	Input voltage range	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high or low state ⁽²⁾	A port	–0.5	$V_{CCA} + 0.5$	V
		B port	–0.5	$V_{CCB} + 0.5$	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through VCCA, VCCB, or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE RATINGS⁽¹⁾⁽²⁾

THERMAL METRIC		TXB0302	UNIT
		DQM	
		8 PINS	
θ_{JA}	Package thermal impedance	259	°C/W

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.
(2) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			VCCA	VCCB	MIN	MAX	UNIT
VCCA	Supply voltage				0.9	3.6	V
VCCB					0.9	3.6	
VIH	High-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	$V_{CCI}^{(2)} \times 0.65$	$V_{CCI}^{(2)}$	V
		OE	0.9 V to 3.6 V	0.9 V to 3.6 V	$V_{CCA} \times 0.65$	3.6	
VIL	Low-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	0	$V_{CCI}^{(2)} \times 0.35$	V
		OE	0.9 V to 3.6 V	0.9 V to 3.6 V	0	$V_{CCA} \times 0.35$	
VO	Voltage range applied to any output in the high-impedance or power-off state	A-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	3.6	V
		B-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	3.6	
$\Delta t/\Delta v$	Input transition rise or fall rate	A-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V		40	ns/V
		B-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V		40	
TA	Operating free-air temperature				–40	85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at VCCI or both at GND.

(2) VCCI is the supply voltage associated with the input port.

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VCCA	VCCB	TA = 25°C			–40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
VOHA	I _{OH} = –20 µA	0.9 V to 3.6 V				0.9 × VCCA			V
VOA	I _{OL} = 20 µA	0.9 V to 3.6 V					0.2		V
VOHB	I _{OH} = –20 µA		0.9 V to 3.6 V			0.9 × VCCB			V
VOB	I _{OL} = 20 µA	0.9 V to 3.6 V					0.2		V
II	OE	VI = VCCI or GND	0.9 V to 3.6 V	0.9 V to 3.6 V		±1		±2	µA
Ioff	A port	VI or VO = 0 to 3.6 V	0 V	0 V to 3.6 V		±1		±2	µA
	B port	VI or VO = 0 to 3.6 V	0 V	0 V to 3.6 V		±1		±2	
IOZ	A or B port	OE = GND	0.9 V to 3.6 V	0.9 V to 3.6 V		±1		±2	µA
ICCA	VI = VCCI or GND, IO = 0	0.9 V to 3.6 V	0.9 V to 3.6 V					5	µA
ICCB	VI = VCCI or GND, IO = 0	0.9 V to 3.6 V	0.9 V to 3.6 V					5	µA
ICCA + ICCB	VI = VCCI or GND, IO = 0	0.9 V to 3.6 V	0.9 V to 3.6 V					10	µA
ICCA	VI = VCCI or GND, IO = 0, OE = GND	0.9 V to 3.6 V	0.9 V to 3.6 V					5	µA
ICCA	VI = VCCI or GND, IO = 0, OE = GND	0.9 V to 3.6 V	0.9 V to 3.6 V					5	µA
CI	OE	0.9 V to 3.6 V	0.9 V to 3.6 V		3				pF
Cio	A port	0.9 V to 3.6 V	0.9 V to 3.6 V		9				pF
	B port				12				

TIMING REQUIREMENTS

		VCCA	VCCB	MIN	MAX	UNIT
Data rate	CL = 15 pF	0.9 to 3.6 V	0.9 to 3.6 V		40	Mbps
	CL = 15 pF	1.2 to 3.6 V	1.2 to 3.6 V		100	Mbps
	CL = 15 pF	1.8 to 3.6 V	1.8 to 3.6 V		140	Mbps
	CL = 30 pF	0.9 to 3.6 V	0.9 to 3.6 V		40	Mbps
	CL = 30 pF	1.2 to 3.6 V	1.2 to 3.6 V		90	Mbps
	CL = 30 pF	1.8 to 3.6 V	1.8 to 3.6 V		120	Mbps
	CL = 50 pF	1.2 to 3.6 V	1.2 to 3.6 V		70	Mbps
	CL = 50 pF	1.8 to 3.6 V	1.8 to 3.6 V		100	Mbps

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		VCCA	VCCB	MIN	TYP T _A = 25°C	MAX	UNIT
t _{pd}	A	B	C _L = 15	0.9-3.6	0.9-3.6		18.9	62.5	ns
	A	B	C _L = 15	1.2-3.6	1.2-3.6		7.5	15.5	
	A	B	C _L = 15	1.8-3.6	1.8-3.6		3.7	5.8	
	A	B	C _L = 30	0.9-3.6	0.9-3.6		19.5	64.5	
	A	B	C _L = 30	1.2-3.6	1.2-3.6		7.8	16.1	
	A	B	C _L = 30	1.8-3.6	1.8-3.6		3.8	6.1	
	A	B	C _L = 50	1.2-3.6	1.2-3.6		8	16.8	
	A	B	C _L = 50	1.8-3.6	1.8-3.6		4	6.5	ns
	B	A	C _L = 15	0.9-3.6	0.9-3.6		18.9	62.6	
	B	A	C _L = 15	1.2-3.6	1.2-3.6		7.5	15.4	
	B	A	C _L = 15	1.8-3.6	1.8-3.6		3.7	5.8	
	B	A	C _L = 30	0.9-3.6	0.9-3.6		19.5	64.5	
	B	A	C _L = 30	1.2-3.6	1.2-3.6		7.8	16.1	
	B	A	C _L = 30	1.8-3.6	1.8-3.6		3.8	5.2	
	B	A	C _L = 50	1.2-3.6	1.2-3.6		8	16.9	
	B	A	C _L = 50	1.8-3.6	1.8-3.6		4	6.6	
t _{en}	OE	A	C _L = 15	0.9-3.6	0.9-3.6			504	ns
		B	C _L = 15	0.9-3.6	0.9-3.6			356	
t _{dis}	OE	A	C _L = 15	0.9-3.6	0.9-3.6			200	ns
		B	C _L = 15	0.9-3.6	0.9-3.6			200	ns
t _{FB} , t _{FB}	B-port rise and fall times		C _L = 15	0.9-3.6	0.9-3.6		2.95		ns
t _S , t _S	A-port rise and fall times		C _L = 15	0.9-3.6	0.9-3.6		3.1		ns
t _{SK(O)}	Channel-to-channel skew		C _L = 15	0.9-3.6	0.9-3.6			0.5	ns

OPERATING CHARACTERISTICS

 T_A = 25°C

PARAMETER		TEST CONDITIONS	VCCA, VCCB 0.9 V to 3.6 V	UNIT
			TYP	
C _{pdA}	A-port input, B-port output	C _L = 0, f = 10 MHz, t _r = t _f = 1 ns, OE = V _{CCA} (outputs enabled)	40	pF
	B-port input, A-port output		40	
C _{pdB}	A-port input, B-port output		40	pF
	B-port input, A-port output		40	
C _{pdA}	A-port input, B-port output	C _L = 0, f = 10 MHz, t _r = t _f = 1 ns, OE = GND (outputs disabled)	0.01	pF
	B-port input, A-port output		0.01	
C _{pdB}	A-port input, B-port output		0.01	pF
	B-port input, A-port output		0.01	

PRINCIPLES OF OPERATION

Applications

The TXB0302 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

Architecture

The TXB0302 architecture (see [Figure 1](#)) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0302 can maintain a high or low, but are designed to be weak, so that they can be over driven by an external driver when data on the bus starts flowing the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 35 Ω at $V_{CCO} = 0.9$ V to 1.1 V, 25 Ω at $V_{CCO} = 1.2$ V to 3.3 V.

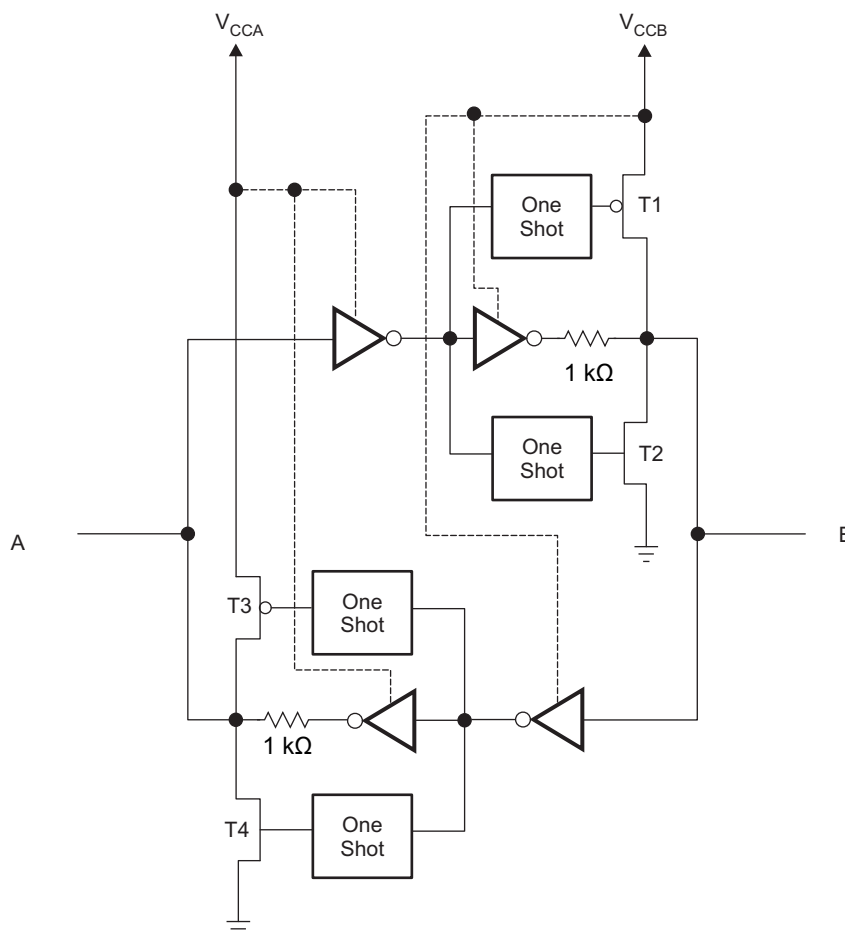
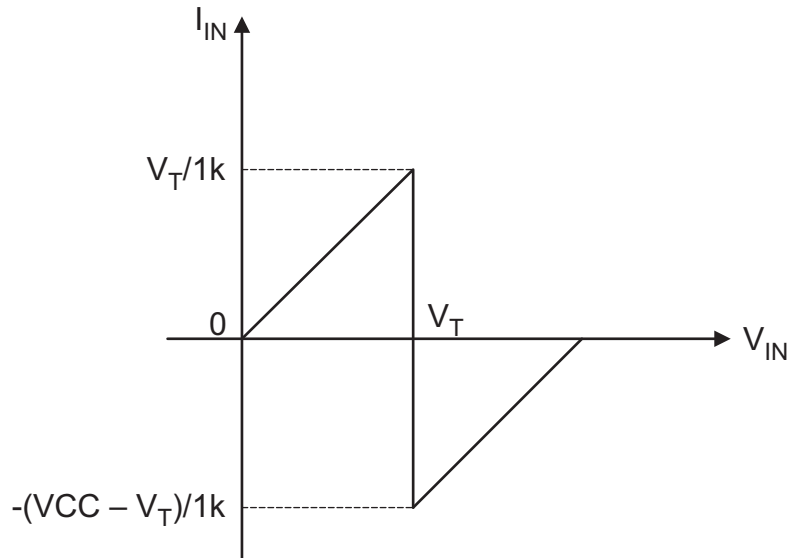


Figure 1. Architecture of TXB0302 I/O Cell

Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0302 are shown in [Figure 2](#). For proper operation, the device driving the data I/Os of the TXB0302 must have drive strength of at least ± 3 mA.



- (1) V_T is the input threshold voltage of the TXB0302 (typical $V_{CCI}/2$).
- (2) V_D is the supply voltage of the external driver.

Figure 2. Typical I_{IN} vs V_{IN} Curve

Power Up

There is no requirement for the power sequence. During operation, TXB0302 can work at both $V_{CCA} \leq V_{CCB}$ and $V_{CCA} \geq V_{CCB}$. During power-up sequencing, any power supply can be ramped up first. The TXB0302 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B} = 0$ V).

Enable and Disable

The TXB0302 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

Pullup or Pulldown Resistor on I/O Lines

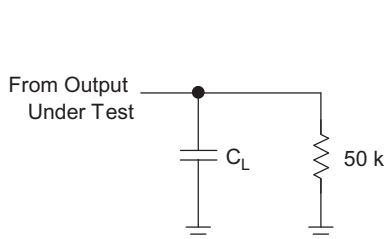
The TXB0302 is designed to drive capacitive loads of up to 50 pF. The output drivers of the TXB0302 have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 20 k Ω to ensure that they do not contend with the output drivers of the TXB0302. but if the receiver is integrated with the smaller pull down or pull up resistor, below formula can be used for estimation to evaluate the V_{oh} and V_{ol} .

$$V_{ol} = V_{CCout} \times \frac{1.5k\Omega}{1.5k\Omega + R_{pu}} \quad (1)$$

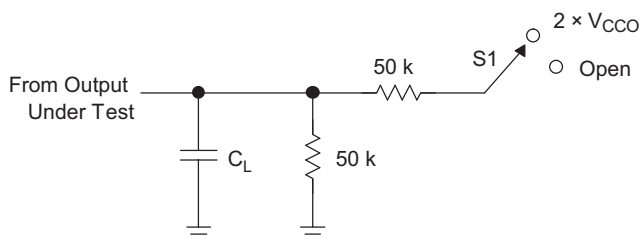
$$V_{oh} = V_{CCout} \times \frac{R_{pd}}{1.5k\Omega + R_{pd}} \quad (2)$$

For the same reason, the TXB0302 should not be used in applications such as I²C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.

PARAMETER MEASUREMENT INFORMATION

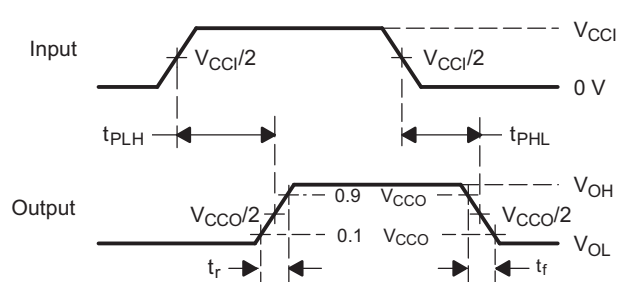


LOAD CIRCUIT FOR MAX DATA RATE,
PULSE DURATION PROPAGATION
DELAY OUTPUT RISE AND FALL TIME
MEASUREMENT

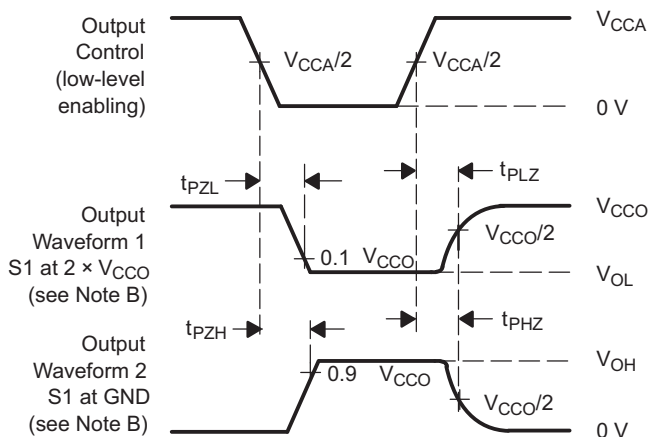


LOAD CIRCUIT FOR
ENABLE/DISABLE
TIME MEASUREMENT

TEST	S1
t_{PZL}/t_{PLZ}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1$ V/ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd} .
- E. V_{CCI} is the V_{CC} associated with the input port.
- F. V_{CCO} is the V_{CC} associated with the output port.
- G. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuits and Voltage Waveforms

REVISION HISTORY

Changes from Original (March 2012) to Revision A	Page
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Changes from Revision A (May 2012) to Revision B	Page
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- Added Application Information Section [5](#)
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0302DQMR	ACTIVE	X2SON	DQM	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	77A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0302DQMR	X2SON	DQM	8	3000	180.0	9.5	1.4	2.0	0.5	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

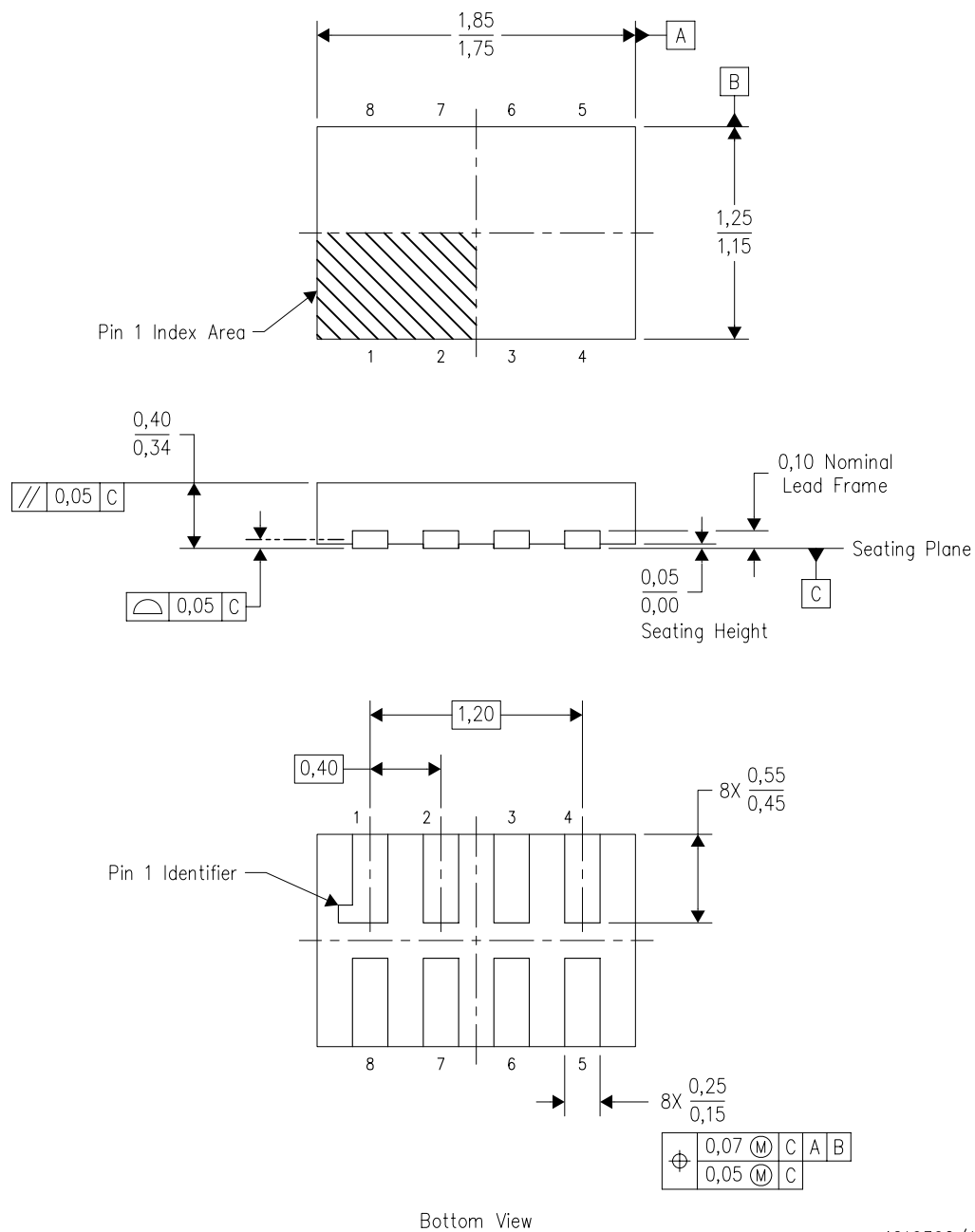


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0302DQMR	X2SON	DQM	8	3000	184.0	184.0	19.0

DQM (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



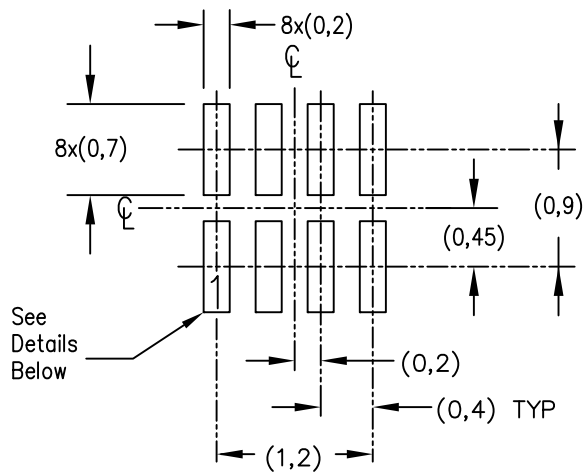
4210302/A 06/2009

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.

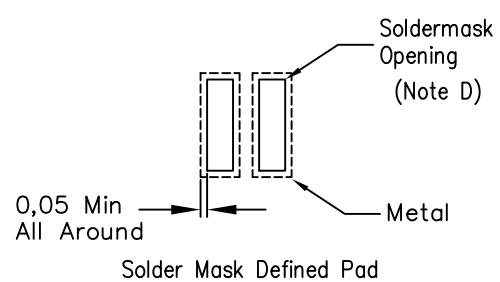
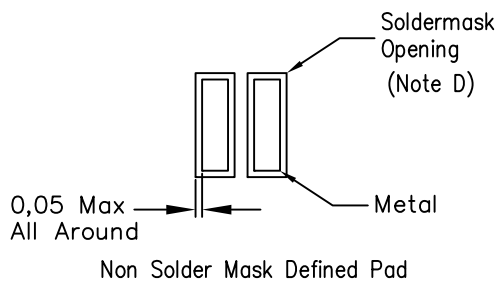
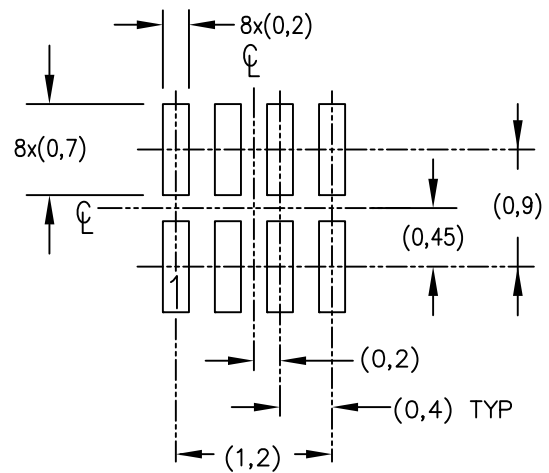
DQM (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD

Example Board Layout



Example Stencil Design
0.1mm Thick Stencil
(Note C)



Solder Mask Details

4218746/A 07/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - D. Customers should contact their board fabrication site for recommended solder mask tolerances.

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