# TPS7A03 Nanopower $I_Q$, 200-nA, 200-mA, Low-Dropout Voltage Regulator With Fast Transient Response

## 1 Features

- Ultra-low $I_Q$: 200 nA (typ), even in dropout
- Shutdown $I_Q$: 3 nA (typ)
- Excellent transient response (1 mA to 50 mA)
  - < 10-µs settling time
  - 80-mv undershoot
- Packages:
  - 1.0-mm × 1.0-mm X2SON
  - SOT23-5 (preview)
  - 0.65-mm x 0.65-mm DSBGA (preview)
- Input voltage range: 1.5 V to 6.0 V
- Output voltage range: 0.8 V to 5.0 V (fixed)
- Output accuracy: 1.5% over temperature
- Smart enable pulldown
- Very low dropout:
  - 205 mV (max) at 200 mA ($V_{OUT}$ = 3.3 V)
- Stable with a 1-µF or larger capacitor

## 2 Applications

- Wearables electronics
- Thermostats, smoke and heat detectors
- Smart meters
- Wireless IOTs
- Portable medical devices
- Building security and surveillance systems
- Electronic point of sale (EPOS)

## 3 Description

The TPS7A03 is an ultra-small, ultra-low quiescent current low-dropout linear regulator (LDO) that can source 200 mA with excellent transient performance.

The TPS7A03, with an ultra-low $I_Q$ of 200 nA, is designed specifically for applications where very-low quiescent current is a critical parameter. This device maintains low $I_Q$ consumption even in dropout mode to further increase the battery life. When in shutdown or disabled mode, the device consumes ultra-low, 3-nA $I_Q$ that helps increase the shelf life of the battery. The TPS7A03 has an output range of 0.8 V to 5.0 V available in 50-mV steps to support the lower core voltages of modern microcontrollers (MCUs).

The TPS7A03 features a smart enable circuit with an internally controlled pulldown resistor that keeps the LDO disabled even when the EN pin is left floating and helps minimize the external components used to pulldown the EN pin. This circuit also helps minimize the current drawn through the external pulldown circuit when the device is enabled.

The TPS7A03 is fully specified for $T_J$ = –40°C to +125°C operation.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS7A03 | X2SON (4) | 1.00 mm × 1.00 mm |
| | DSBGA (4)(2) | 0.65 mm × 0.65 mm |
| | SOT-23 (5)(2) | 2.90 mm × 1.60 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) Preview package.

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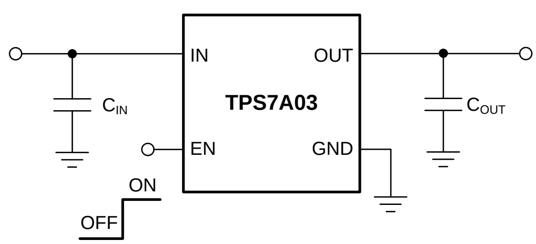
**Typical Application Circuit**

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## Table of Contents



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| July 2019 | * | Initial release. |


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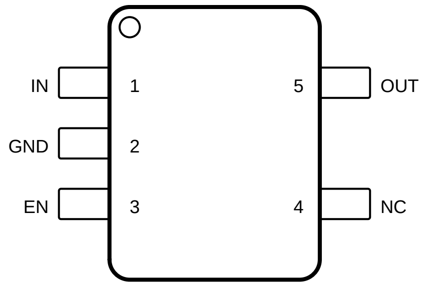
## 5 Pin Configuration and Functions

**DBV Package (Preview)**
**5-Pin SOT-23**
**Top View**

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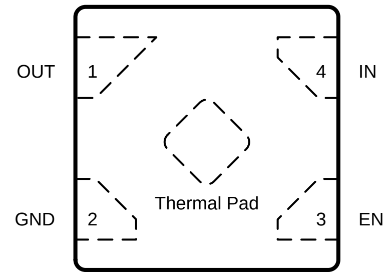
**DQN Package**
**1-mm × 1-mm X2SON-4**
**Top View**




Not to scale

### Pin Functions: DQN, DBV

| PIN | | | I/O[(1)] | DESCRIPTION |
|---|---|---|---|---|
| NAME | DQN | DBV[(2)] | | |
| EN | 3 | 3 | Input | Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN. $V_{EN}$ must not exceed $V_{IN}$. |
| GND | 2 | 2 | — | Ground pin. This pin must be connected to ground and the thermal pad. |
| IN | 4 | 1 | Input | Input pin. A 0.1-µF or greater effective capacitance is required from IN to ground to minimize input impedance. For best transient response, use a 1-µF or larger ceramic capacitor from IN to ground. Place the input capacitor as close to input of the device as possible. |
| NC | — | 4 | — | No connect pin. This pin is not internally connected. Connect to ground or leave floating. |
| OUT | 1 | 5 | Output | Regulated output pin. A 0.5-µF or greater effective capacitance is required from OUT to ground for stability. For best transient response, use a 1-µF or larger ceramic capacitor from OUT to ground. Place the output capacitor as close to output of the device as possible. |
| Thermal pad | | — | — | Connect the thermal pad to a large-area ground plane. The thermal pad is internally connect to ground. |

(1) NC = No internal connection.
(2) Preview package.

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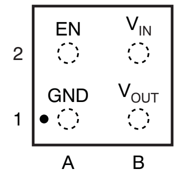
**YKA Package (Preview)**
**4-Pin 0.65-mm x 0.65-mm, 0.35-mm Pitch DSBGA**
**Top View**




## Pin Functions: YKA

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | YKA (1) | | |
| EN | A2 | Input | Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN. $V_{EN}$ must not exceed $V_{IN}$. |
| GND | A1 | — | Ground pin. This pin must be connected to ground and the thermal pad. |
| IN | B2 | Input | Input pin. A 0.1-µF or greater effective capacitance is required from IN to ground to minimize input impedance. For best transient response, use a 1-µF or larger ceramic capacitor from IN to ground. Place the input capacitor as close to input of the device as possible. |
| OUT | B1 | Output | Regulated output pin. A 0.5-µF or greater effective capacitance is required from OUT to ground for stability. For best transient response, use a 1-µF or larger ceramic capacitor from OUT to ground. Place the output capacitor as close to output of the device as possible. |

(1) Preview package.

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | $V_{IN}$ | –0.3 | 6.5 | V |
| | $V_{EN}$ | –0.3 | 6.5 | |
| | $V_{OUT}$ | –0.3 | $V_{IN}$ + 0.3 or 5.5(2) | |
| Current | Maximum output | Internally limited | | A |
| Temperature | Operating junction, $T_J$ | –40 | 150 | °C |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum is $V_{IN}$ + 0.3 V or 5.5 V, whichever is smaller.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 1.5 | | 6.0 | V |
| $V_{EN}$ | Enable voltage | 0 | | $V_{IN}$ | V |
| $V_{OUT}$ | Output voltage | 0.8 | | 5.0 | V |
| $I_{OUT}$ | Output current | 0 | | 200 | mA |
| $C_{IN}$ | Input capacitor | | 1 | | µF |
| $C_{OUT}$ | Output capacitor(1) | 1 | 1 | 22 | µF |
| $F_{EN}$ | EN toggle frequency | | | 10 | kHz |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

(1) Effective output capacitance of 0.5 µF minimum required for stability.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPS7A03 | | | UNIT |
|---|---|---|---|---|---|
| | | DQN (X2SON) | DBV (SOT23-5) | YFF (DSBGA) | |
| | | 4 PINS | 5 PINS | 4 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 179.1 | TBD | TBD | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 137.6 | TBD | TBD | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 116.3 | TBD | TBD | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6.1 | TBD | TBD | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 116.3 | TBD | TBD | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | 112.3 | TBD | TBD | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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## 6.5 Electrical Characteristics

Specified at $T_J$ = –40°C to +125°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted). Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Nominal accuracy | $T_J$ = 25°C, $V_{OUT}$ ≥ 1.0 V, 1 µA ≤ $I_{OUT}$ ≤ 1 mA | | –1 | | 1 | % |
| | Nominal accuracy | $T_J$ = 25°C; $V_{OUT}$ < 1.0 V | | –10 | | 10 | mV |
| | Accuracy over temperature | $V_{OUT}$ ≥ 1.0 V | $T_J$ = –40°C to +85°C | –1.5 | | 1.5 | % |
| | | | $T_J$ = –40°C to +125°C | –3 | | 3 | |
| | | $V_{OUT}$ < 1.0 V | $T_J$ = –40°C to +85°C | –15 | | 15 | mV |
| | | | $T_J$ = –40°C to +125°C | –30 | | 30 | |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation | $V_{OUT(nom)}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.0 V(1) | $T_J$ = –40°C to +85°C | | 2.2 | 3 | mV/V |
| | | | $T_J$ = –40°C to +125°C | | | 4 | |
| $\Delta V_{OUT}(\Delta I_{OUT})$ | Load regulation(2) | 1 mA ≤ $I_{OUT}$ ≤ 200 mA, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V(1) | $T_J$ = –40°C to +85°C | | 20 | 38 | mV |
| | | | $T_J$ = –40°C to +125°C | | | 50 | |
| $I_{GND}$ | Ground current, | $I_{OUT}$ ≤ 0.4 µA | $T_J$ = 25°C | | 200 | 250 | nA |
| | | | $T_J$ = –40°C to +85°C | | | 300 | |
| $I_{GND}/I_{OUT}$ | Ground current efficiency vs load current | 20 µA ≤ $I_{OUT}$ < 1 mA | $T_J$ = 25°C | | 1 | | % |
| | | 1 mA ≤ $I_{OUT}$ ≤ 100 mA | | | 0.25 | | |
| | | $I_{OUT}$ ≥ 100 mA | | | 0.15 | | |
| $I_{GND(DO)}$ | Ground current in dropout(3) | $I_{OUT}$ ≤ 0.4 µA, 1.5 V ≤ $V_{IN}$ < 6.0 V, | $T_J$ = –40°C to +85°C | | 220 | 250 | nA |
| $I_{SHDN}$ | Shutdown current | $V_{EN}$ = 0 V, 1.5 V ≤ $V_{IN}$ ≤ 6.0 V, $T_J$ = 25°C | | | 3 | 10 | nA |
| $I_{CL}$ | Output current limit | $V_{OUT}$ = 90% × $V_{OUT(nom)}$, $V_{IN}$ = $V_{OUT(nom)}$ + $V_{DO(max)}$ + 0.1 V | | 240 | 450 | 650 | mA |
| $I_{SC}$ | Short-circuit current limit | $V_{OUT}$ = 0 V | | | 65 | | mA |
| $V_{DO}$ | Dropout voltage(4) | $T_J$ = –40°C to +85°C | 0.8 V ≤ $V_{OUT}$ < 1.0 V | | | 1046 | mV |
| | | | 1.0 V ≤ $V_{OUT}$ < 1.2 V | | | 876 | |
| | | | 1.2 V ≤ $V_{OUT}$ < 1.5 V | | | 670 | |
| | | | 1.5 V ≤ $V_{OUT}$ < 1.8 V | | | 446 | |
| | | | 1.8 V ≤ $V_{OUT}$ < 2.5 V | | | 400 | |
| | | | 2.5 V ≤ $V_{OUT}$ < 3.3 V | | | 250 | |
| | | | 3.3 V ≤ $V_{OUT}$ < 5.0 V | | | 204 | |
| | | $T_J$ = –40°C to +125°C | 0.8 V ≤ $V_{OUT}$ < 1.0 V | | | 1114 | |
| | | | 1.0 V ≤ $V_{OUT}$ < 1.2 V | | | 953 | |
| | | | 1.2 V ≤ $V_{OUT}$ < 1.5 V | | | 803 | |
| | | | 1.5 V ≤ $V_{OUT}$ < 1.8 V | | | 535 | |
| | | | 1.8 V ≤ $V_{OUT}$ < 2.5 V | | | 430 | |
| | | | 2.5 V ≤ $V_{OUT}$ < 3.3 V | | | 299 | |
| | | | 3.3 V ≤ $V_{OUT}$ < 5.0 V | | | 245 | |
| PSRR | Power-supply rejection ratio | f = 1 kHz, $I_{OUT}$ = 30 mA | | | 55 | | dB |
| $V_N$ | Output voltage noise | BW = 10 Hz to 100 kHz, $V_{OUT}$ = 0.8 V, $I_{OUT}$ = 30 mA | | | 115 | | $µV_{RMS}$ |
| $V_{UVLO}$ | UVLO threshold | $V_{IN}$ rising | | 1.23 | 1.3 | 1.47 | V |
| | | $V_{IN}$ falling | | 1.17 | 1.12 | 1.26 | |
| $V_{UVLO(HYST)}$ | UVLO hysteresis | $V_{IN}$ hysteresis | | | 180 | | mV |

(1) $V_{IN}$ = 2.0 V for $V_{OUT}$ ≤ 0.9 V.
(2) Load Regulation is normalized to the output voltage at $I_{OUT}$ = 1 mA.
(3) $V_{IN}$ = 95% x $V_{OUT(NOM)}$.
(4) Dropout is measured by ramping $V_{IN}$ down until $V_{OUT}$ = $V_{OUT(nom)}$ x 95%, with $I_{OUT}$ = 200 mA.

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## Electrical Characteristics (continued)

Specified at $T_J$ = –40°C to +125°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted). Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{EN(HI)}$ | EN pin logic high voltage | | 1.1 | | | V |
| $V_{EN(LOW)}$ | EN pin logic low voltage | | | | 0.3 | V |
| $I_{EN}$ | EN pin leakage current | $V_{EN}$ = $V_{IN}$ = 6.0 V | | 10 | | nA |
| $R_{EN(PULLDOWN)}$ | Smart enable pulldown resistor | $V_{EN}$ = 0.3 V | | 500 | | KΩ |
| $R_{PULLDOWN}$ | Pulldown resistor | $V_{IN}$ = 3.3 V, device disabled | | 120 | | Ω |
| $T_{SD(shutdown)}$ | Thermal shutdown temperature | Shutdown, temperature increasing | | 175 | | °C |
| $T_{SD(reset)}$ | Thermal shutdown reset temperature | Reset, temperature decreasing | | 155 | | °C |

## 6.6 Switching Characteristics

At $V_{IN}$ = $V_{OUT}$ +$V_{DO(max)}$ + 0.5 V, $I_{OUT}$ = 30 mA, and$C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted). Alltypical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{STR}$ | Start-up time | From EN assertion to $V_{OUT}$ = 95% × $V_{OUT(nom)}$ , $V_{OUT}$ = 1.8 V | | 400 | 1500 | µs |

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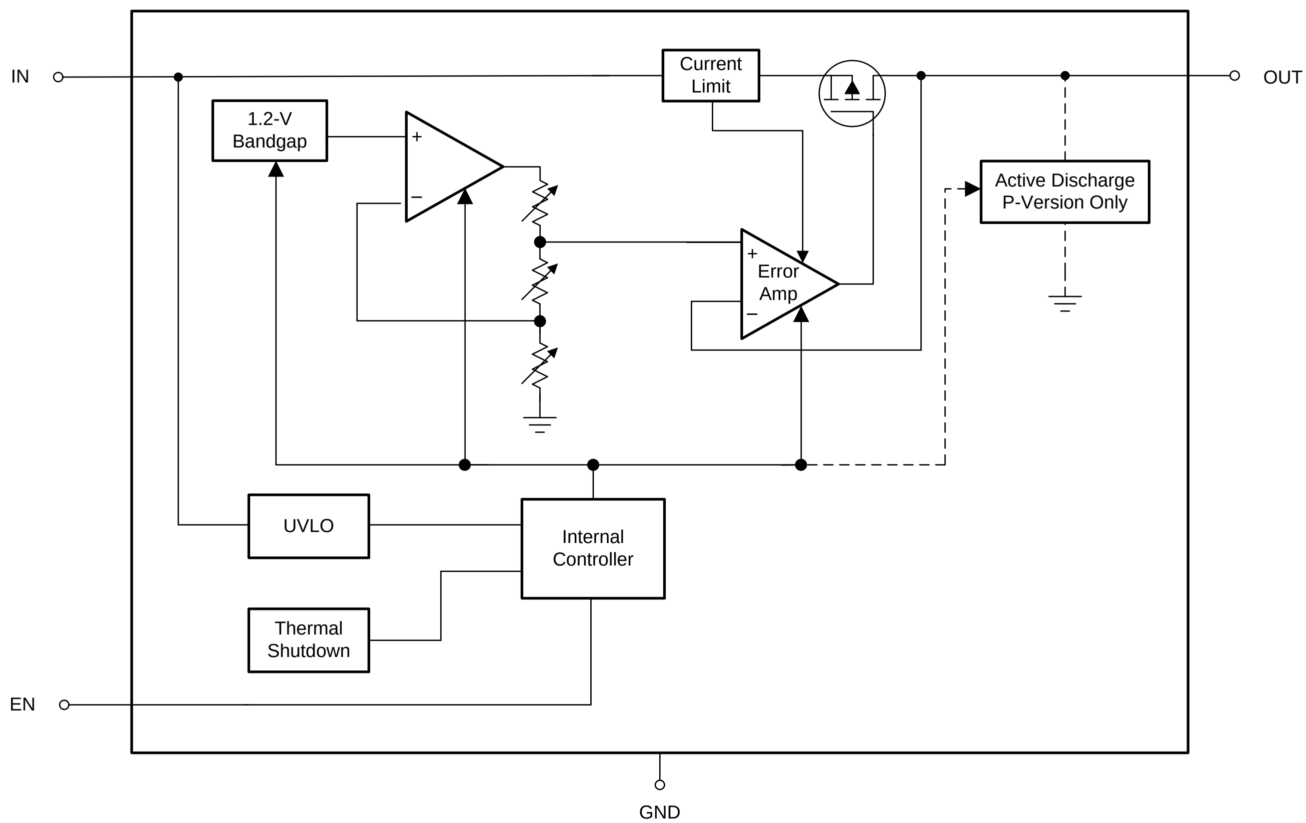
# 7 Detailed Description

## 7.1 Overview

The TPS7A03 is a ultra-low $I_Q$ linear voltage regulator that is optimized for excellent transient performance. These characteristics make the device ideal for most battery-powered applications.

This low-dropout linear regulator (LDO) offers optional active discharge, foldback current limit, shutdown, and thermal protection.

## 7.2 Functional Block Diagram

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## 7.3 Feature Description

### 7.3.1 Excellent Transient Response

The device includes several innovative circuits to ensure excellent transient response. Dynamic biasing increases the $I_Q$ for a short duration during transients to extend the closed-loop bandwidth and improve the device response time to transients.

Adaptive biasing increases the $I_Q$ as the dc load current increases, extending the bandwidth of the loop. The device response time across the output voltage range is constant because a buffered reference topology is used, which keeps the control loop in unity gain at any output voltage.

These features give the device a wide loop bandwidth during transients that ensures excellent transient response while maintaining the device low $I_Q$ in steady-state conditions.

### 7.3.2 Active Discharge (P-Version Only)

The device has an internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin or by the undervoltage lockout (UVLO).

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

### 7.3.3 Low $I_Q$ in Dropout

In most LDOs the $I_Q$ significantly increases when the device is placed into dropout, which is especially true for low $I_Q$ LDOs with adaptive biasing. The TPS7A03 detects when operating in dropout conditions and disables the adaptive biasing, thus minimizing the $I_Q$ increase.

### 7.3.4 Smart Enable

The enable pin for the device is an active-high pin. The output voltage is enabled when the voltage of the enable pin is greater than the high-level input voltage of the EN pin and disabled with the enable pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the enable pin to the input of the device.

This device has a smart enable circuit to reduce quiescent current. When the voltage on the enable pin is driven above $V_{EN(HI)}$, as listed in the *Electrical Characteristics* table, the device is enabled and the smart enable internal pulldown resistor ($R_{EN(PULLDOWN)}$) is disconnected. When the enable pin is floating, the $R_{EN(PULLDOWN)}$ is connected and pulls the enable pin low to disable the device. The $R_{EN(PULLDOWN)}$ value is listed in the *Electrical Characteristics* table.

This device has an internal pulldown circuit that activates when the device is disabled to actively discharge the output voltage.

### 7.3.5 Dropout Voltage

Dropout voltage ($V_{DO}$) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current ($I_{RATED}$), where the pass transistor is fully on. $I_{RATED}$ is the maximum $I_{OUT}$ listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use Equation 1 to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

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## Feature Description (continued)

### 7.3.6 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit ($I_{CL}$). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit ($I_{SC}$). $I_{CL}$ and $I_{SC}$ are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = TBD% × $V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [($V_{IN}$ – $V_{OUT}$) × $I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [($V_{IN}$ – $V_{OUT}$) × $I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

Figure 1 shows a diagram of the foldback current limit.

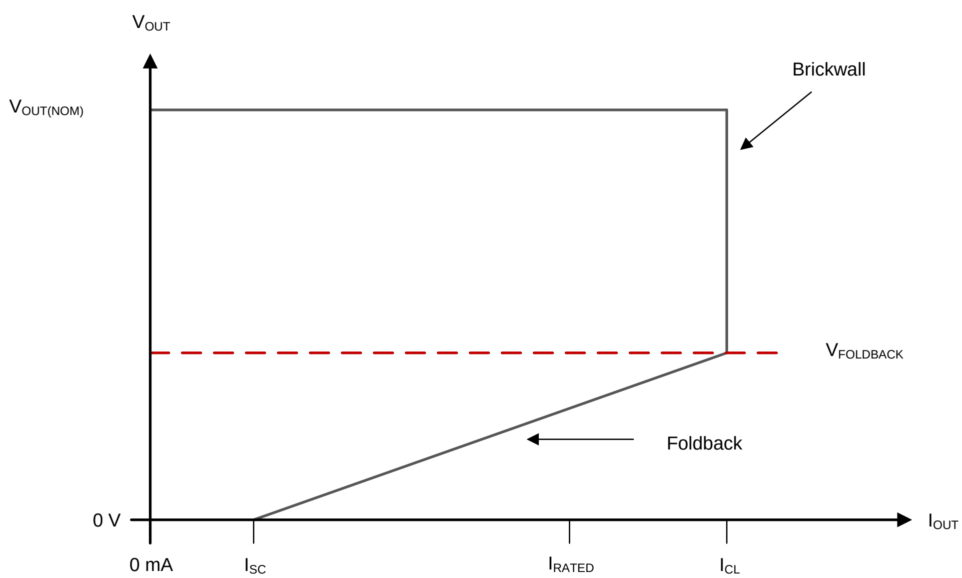


**Figure 1. Foldback Current Limit**

### 7.3.7 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

### 7.3.8 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature ($T_J$) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

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## Feature Description (continued)

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large $V_{IN}$ – $V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

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## 7.4 Device Functional Modes

### 7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

**Table 1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| | $V_{IN}$ | $V_{EN}$ | $I_{OUT}$ | $T_J$ |
| Normal operation | $V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Dropout operation | $V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Disabled (any true condition disables the device) | $V_{IN} < V_{UVLO}$ | $V_{EN} < V_{EN(LOW)}$ | Not applicable | $T_J > T_{SD(shutdown)}$ |

### 7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

### 7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

### 7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

### 8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

### 8.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

### 8.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in Figure 2 are broken down as follows. Regions A, E, and H are where the output voltage is in steady-state.

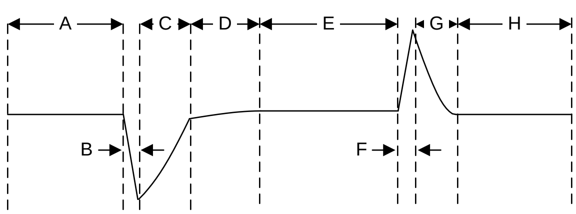


**Figure 2. Load Transient Waveform**

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation (region C)

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## Application Information (continued)

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

### 8.1.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit ensures that the device stays disabled before its input supply reaches the minimum operational voltage range, and ensures that the device shuts down when the input supply collapses. Figure 3 shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

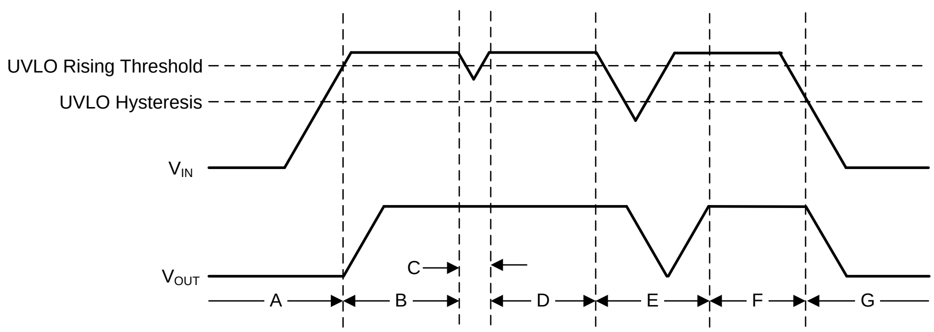


**Figure 3. Typical UVLO Operation**

### 8.1.5 Power Dissipation ($P_D$)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use Equation 2 to approximate $P_D$:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A85 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.


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## Application Information (continued)

The maximum power dissipation determines the maximum allowable junction temperature ($T_J$) for the device. According to Equation 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air ($T_A$). Equation 4 rearranges Equation 3 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (4)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the X2SON package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

### *8.1.5.1 Estimating Junction Temperature*

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) are used in accordance with Equation 5 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D$$

where:

- $P_D$ is the power dissipated as explained in Equation 2
- $T_T$ is the temperature at the center-top of the device package, and
- $T_B$ is the PCB surface temperature measured 1 mm from the device package and centered on the package edge (5)

### *8.1.5.2 Recommended Area for Continuous Operation*

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in Figure 4 and can be separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN}$ – $V_{OUT}$) at a given output current level. See the *Dropout Operation* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - The shape of the slope is given by Equation 4. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO; thus when $V_{IN}$ – $V_{OUT}$ increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN}$ – $V_{OUT}$.

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## Application Information (continued)

Figure 4 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{\theta JA}$ = TBD°C/W, as given in the *Thermal Information* table.

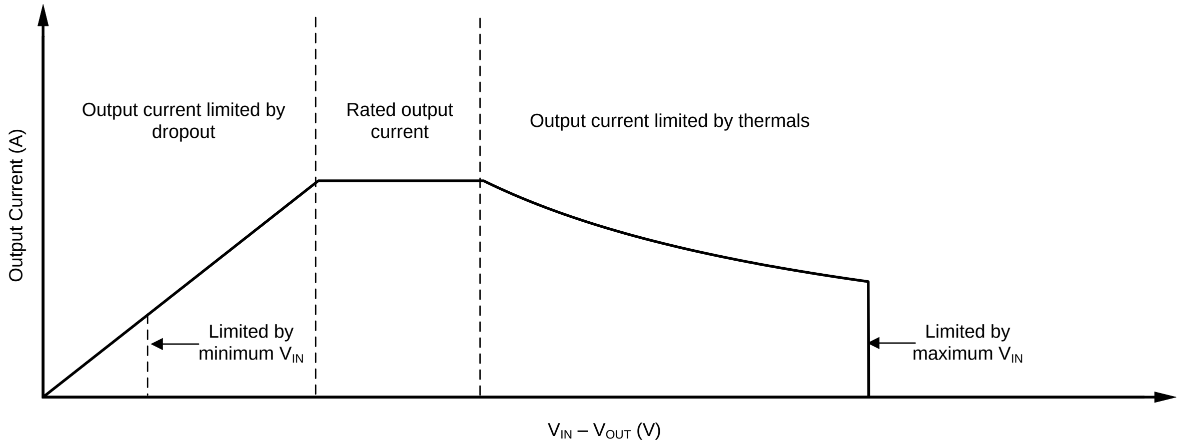


**Figure 4. Region Description of Continuous Operation Regime**

## 8.2 Typical Application

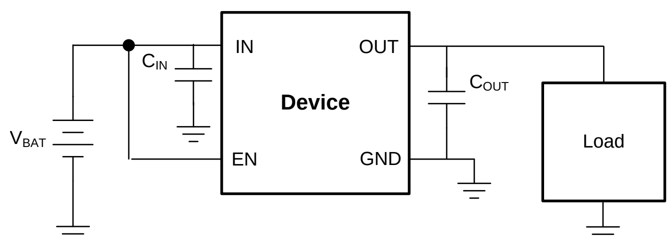


**Figure 5. Capacitor-Free Operation From a Battery Input Supply**

### 8.2.1 Design Requirements

**Table 2. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 3.0 V to 1.8 V (two 1.5-V batteries) |
| Output voltage | 1.0 V, ±1% |
| Input current | 200 mA, maximum |
| Output load | 100-mA dc |
| Maximum ambient temperature | 70°C |

### 8.2.2 Detailed Design Procedure

Use the recommend 1-µF input and output capacitor because the input source has a high ESR of 600 mΩ (typ).

# 9 Power Supply Recommendations

TI highly recommends using a 1 µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.


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# 10 Layout

## 10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DQN package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

## 10.2 Layout Examples

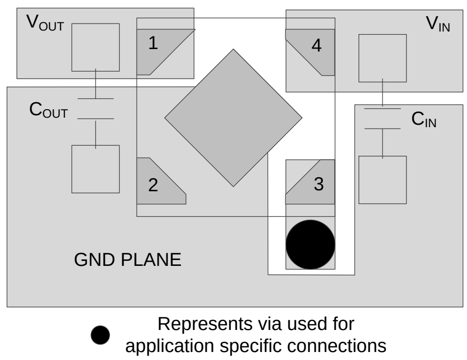


**Figure 6. Layout Example for the DQN Package**

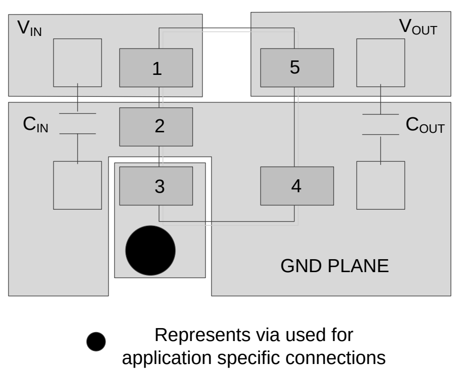


**Figure 7. Layout Example for the DBV Package**

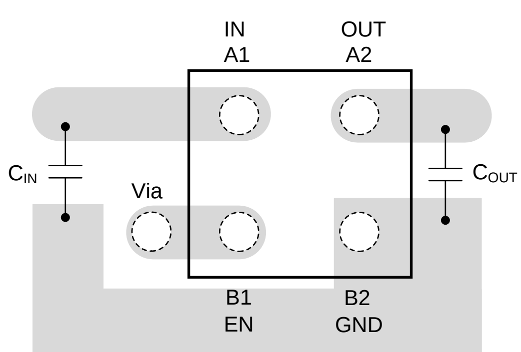


**Figure 8. Layout Example for the YKA Package**

ADVANCE INFORMATION

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Device Nomenclature

**Table 3. Device Nomenclature[1][2]**

| PRODUCT | $V_{OUT}$ |
|---|---|
| TPS7A03**xx(x)Pyyyz** | **XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V).<br>**P** indicates an active output discharge feature. All members of the TPS7A03 family actively discharge the output when the device is disabled.<br>**YYY** is the package designator.<br>**Z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces). |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.0 V to 3.3 V in 50-mV increments are available. Contact the factory for details and availability.

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 Trademarks

E2E is a trademark of Texas Instruments.
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## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PTPS7A0315PDQNR | ACTIVE | X2SON | DQN | 4 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| PTPS7A0318PDQNR | ACTIVE | X2SON | DQN | 4 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| PTPS7A0320PDQNR | ACTIVE | X2SON | DQN | 4 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| PTPS7A0325PDQNR | ACTIVE | X2SON | DQN | 4 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| PTPS7A0328PDQNR | ACTIVE | X2SON | DQN | 4 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| PTPS7A0330PDQNR | ACTIVE | X2SON | DQN | 4 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| PTPS7A0333PDQNR | ACTIVE | X2SON | DQN | 4 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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