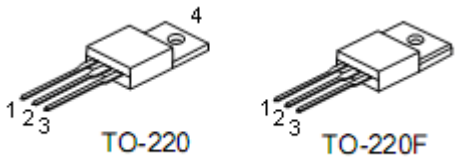
1. Description

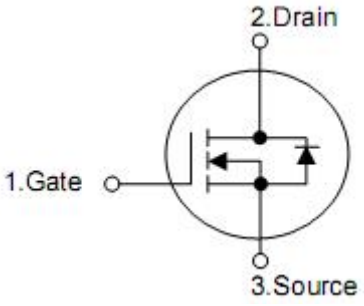
The KNX6450A-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology

2. Features

- ROHS Compliant
- RDS(ON),typ.=0.40 Ω@VGS=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

3. Pin configuration





Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Ordering Information

Part Number	Package	Brand
KNF6450A	TO-220F	KIA
KNP6450A	TO-220	KIA

5. Absolute maximum ratings

TC=25℃ unless otherwise specified

Parameter	Symbol	Ratings		Unit
		TO220	TO22F	
Drain-to-Source Voltage	V_{DSS}	500		V
Gate-to-Source Voltage	V_{GSS}	±30		
Continuous Drain Current	I_D	13		A
Pulsed Drain Current at VGS=10V	I_{DM}	52		
Single Pulse Avalanche Energy	E_{AS}	900		mJ
Power Dissipation	P_D	195	48	W
Derating Factor above 25℃		1.56	0.38	W/ ºC
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	T_L T_{PAK}	300 260		ºC
Operating and StorageTemperatureRange	T_J& T_{STG}	-55 to 150		

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Ratings		Units
		TO220	TO220F	
Thermal resistance, junction-ambient	$R_{\theta JA}$	62	100	ºC/W
Thermal resistance, Junction-case	$R_{\theta JC}$	0.64	2.6	

7. Electrical characteristics

(T_J=25°C,unless otherwise notes)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Off characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	500	-	-	V
Drain-to-source Leakage Current	I_{DSS}	V_{DS}=500V ,V_{GS}=0V	-	-	1	μA
		V_{DS}=400V , V_{GS}=0V T_C=125ºC,	-	-	10	μA
Gate-body leakage current	I_{GSS}	V_{GS}=30V,V_{DS}=0V	-	-	+100	nA
		V_{GS}=-30V,V_{DS}=0V	-	-	-100	nA
On characteristics						
Static drain-source on-resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=6.5A	-	0.4	0.48	Ω
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.0	-	4.0	V
Forward Transconductance	gfs	VDS=30V,ID=13A	-	15	-	S
Dynamic characteristics						
Input capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1MHz	-	2149	-	pF
Output capacitance	C_{oss}		-	211	-	pF
Reverse transfer capacitance	C_{rss}		-	23	-	pF
Total gate charge						
Turn-on delay time	$t_{d(on)}$	V_{DD}=250V,I_D=13.0A, V_{GS}=10V,R_G=6.1Ω	-	15	-	ns
Rise time	t_r		-	24	-	ns
Turn-off delay time	$t_{d(off)}$		-	46	-	ns
Fall time	t_f		-	34	-	ns
Total gate charge	Q_g	V_{DS}=250V,I_D=13.0A , V_{GS}=0 to10V	-	44	-	nC
Gate-source charge	Q_{gs}		-	10	-	nC
Gate-drain charge	Q_{gd}		-	17	-	nC
Drain-source diode characteristics						
Drain-source diode forward voltage	V_{SD}	V_{GS}=0V,I_S=13.0A	-	-	1.5	V
Continuous drain-source current [2]	I_{SD}	Integral pn-diode In MOSFET	-	-	13	A
Pulsed drain-source current[2]	I_{SM}		-	-	52	A
Reverse recovery time	t_{rr}	V_{GS}=0V,I_F=13.0A dI_{SD}/dt=100A/μs	-	498	-	ns
Reverse recovery charge	Q_{rr}		-	4.0	-	μC

Note: [1] TJ=+25 ºC to +150 ºC
[2] Pulse width≤380μs; duty cycle≤2%.

8. Typical Characteristics

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

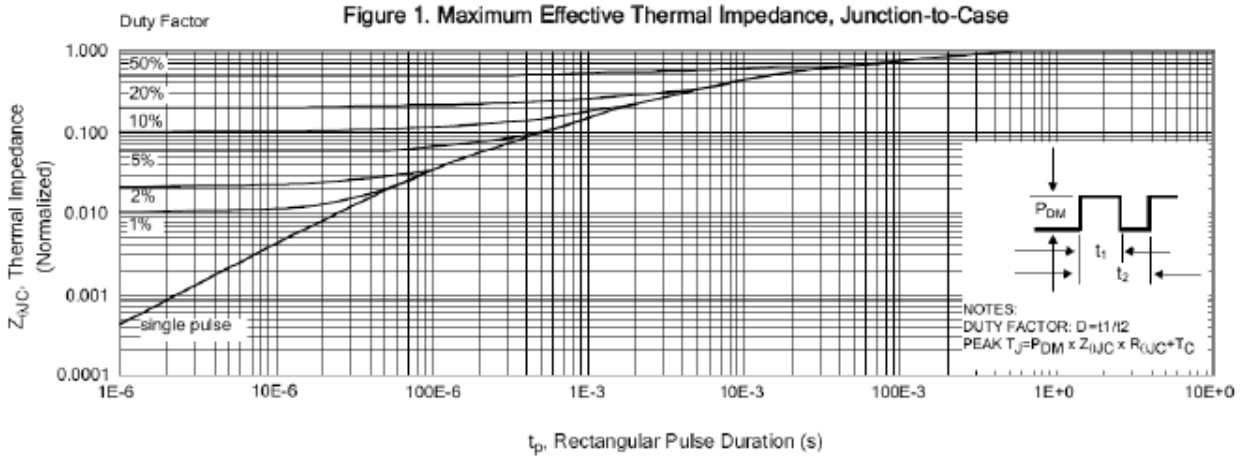


Figure 2. Maximum Power Dissipation vs Case Temperature

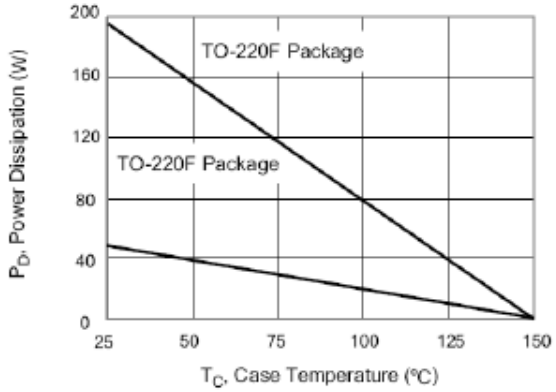


Figure 3. Maximum Continuous Drain Current vs Case Temperature

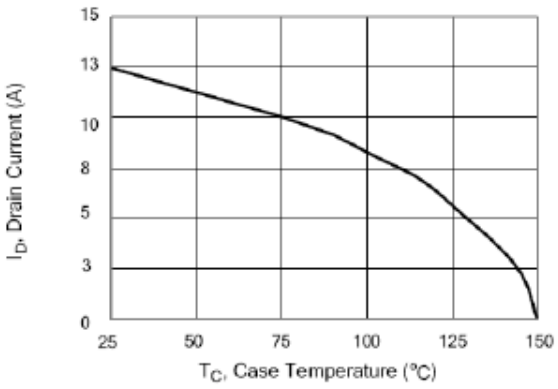


Figure 4. Typical Output Characteristics

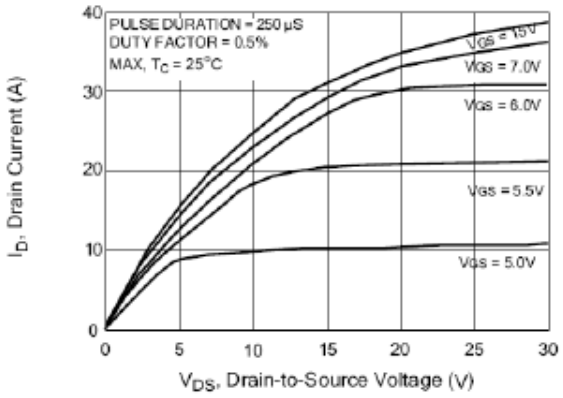


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

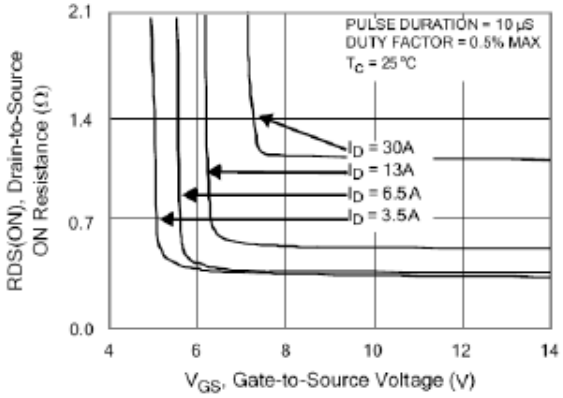


Figure 6. Maximum Peak Current Capability

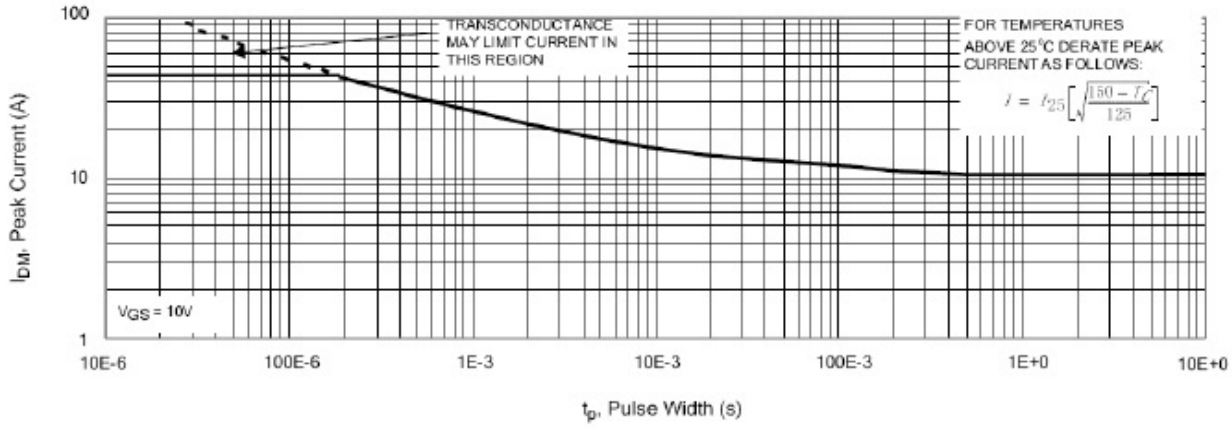


Figure 7. Typical Transfer Characteristics

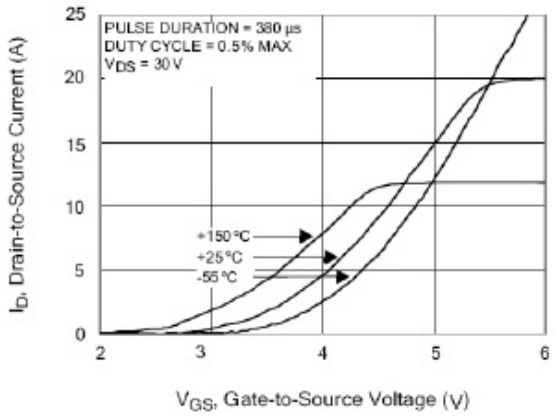


Figure 8. Unclamped Inductive Switching Capability

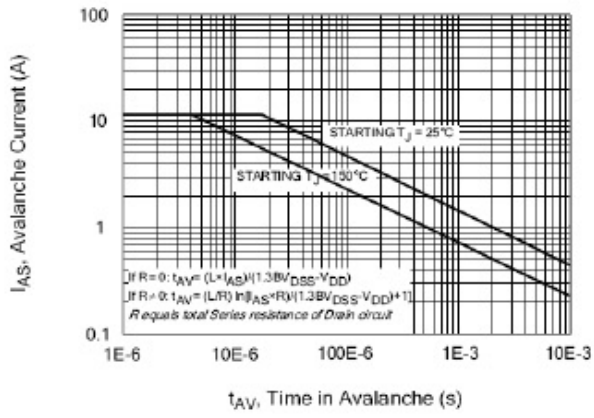


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

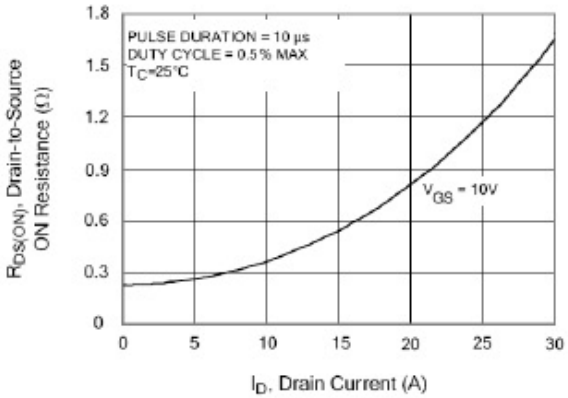


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

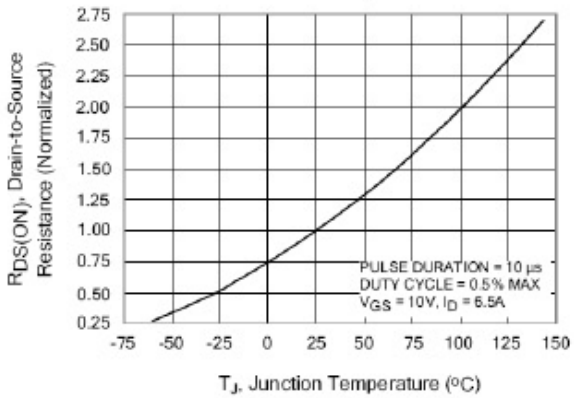


Figure 11. Typical Breakdown Voltage vs Junction Temperature

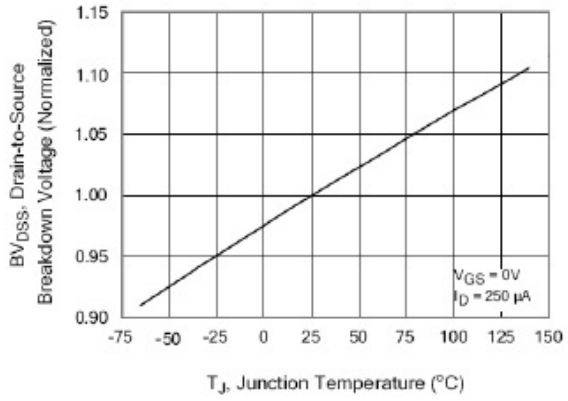


Figure 12. Typical Threshold Voltage vs Junction Temperature

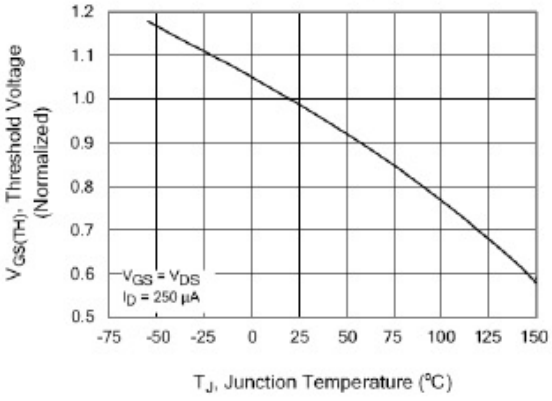


Figure 13. Maximum Forward Bias Safe Operating Area

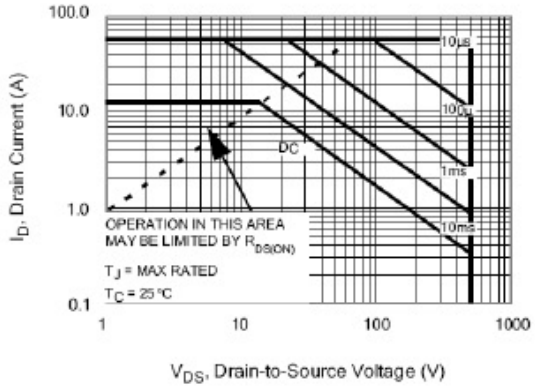


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

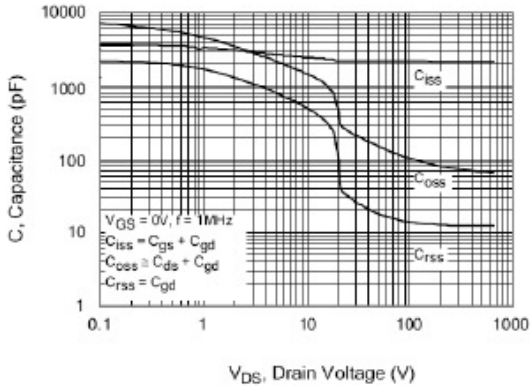


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

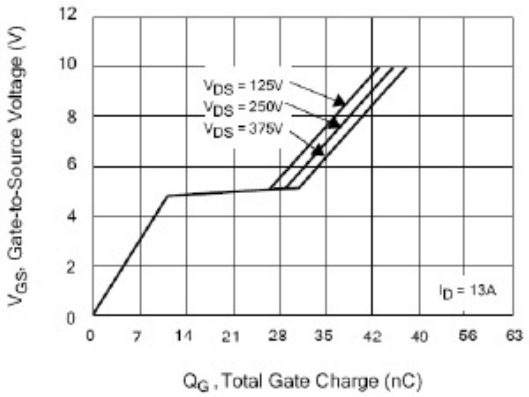
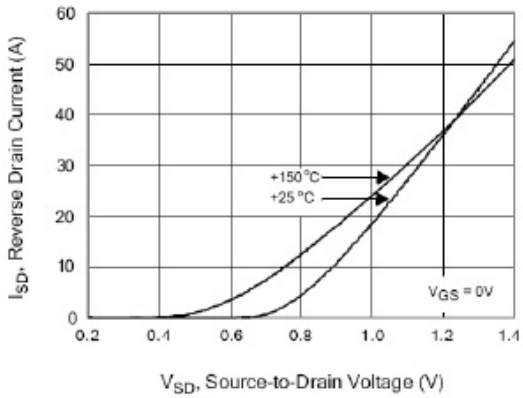


Figure 16. Typical Body Diode Transfer Characteristics



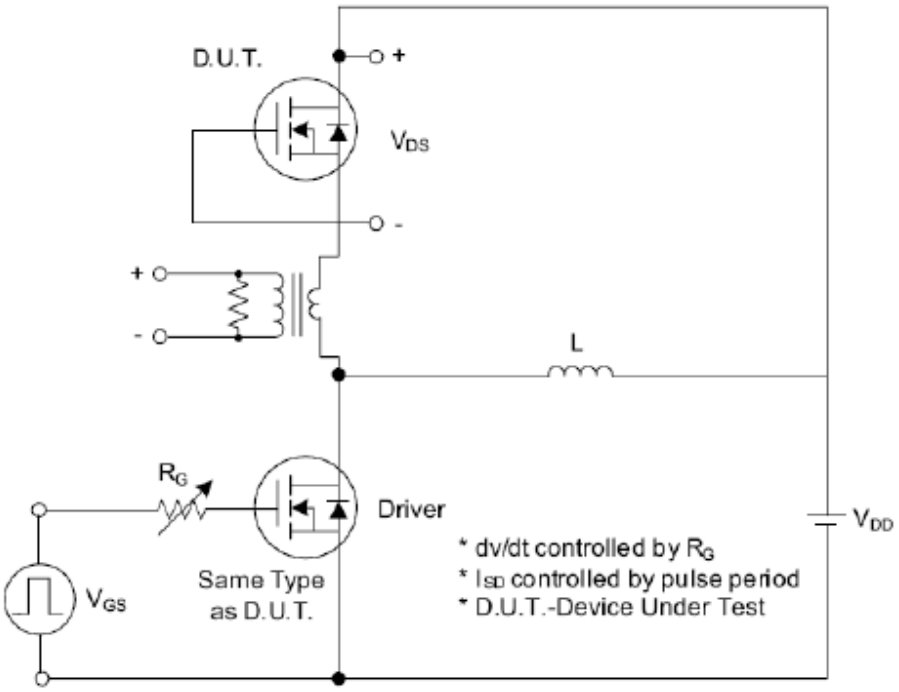


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

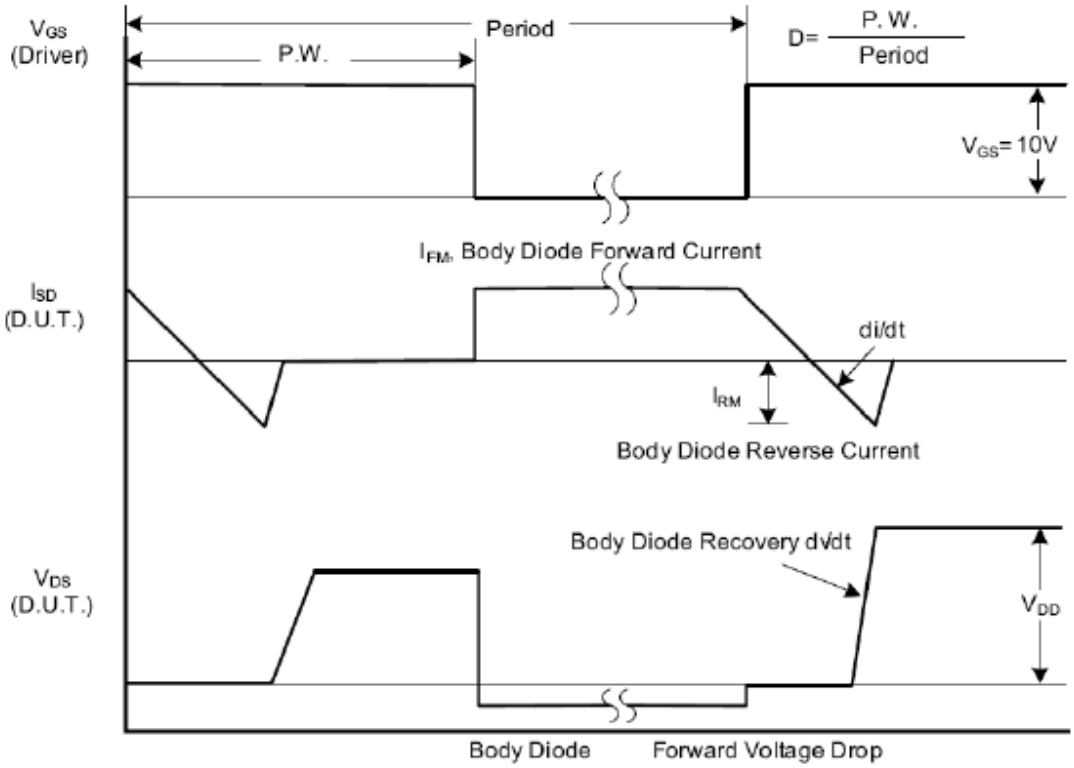


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

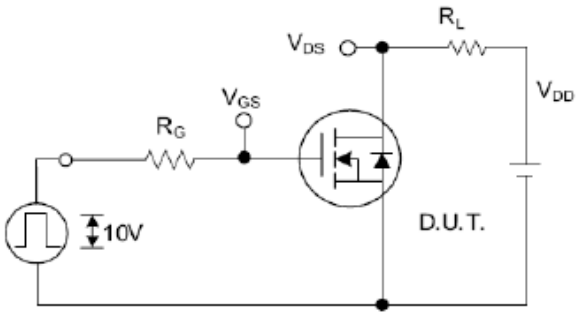


Fig. 2.1 Switching Test Circuit

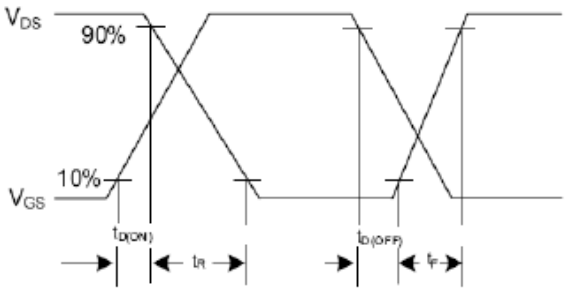


Fig. 2.2 Switching Waveforms

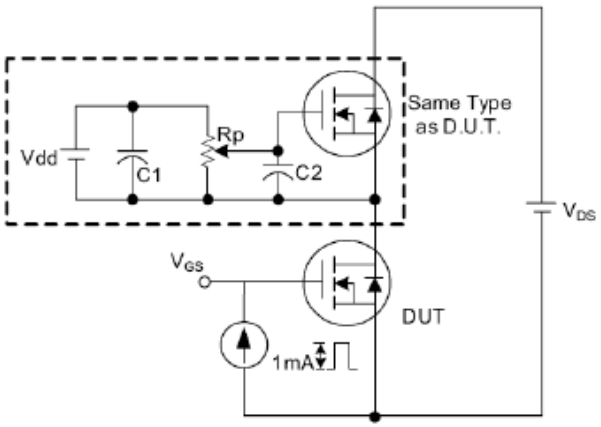


Fig. 3 . 1 Gate Charge Test Circuit

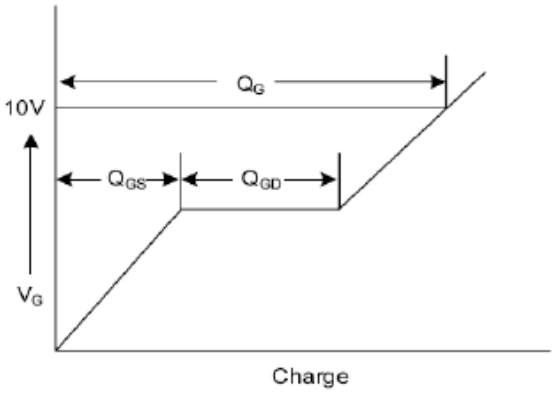


Fig. 3 . 2 Gate Charge Waveform

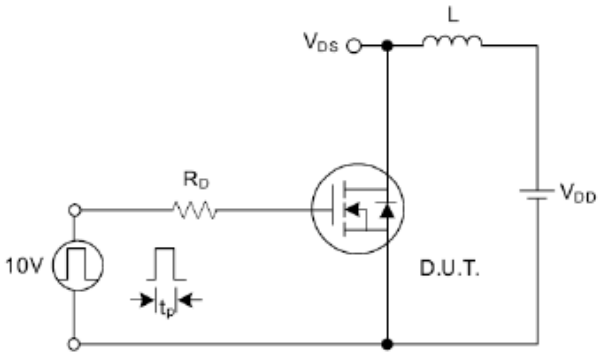


Fig. 4.1 Unclamped Inductive Switching Test Circuit

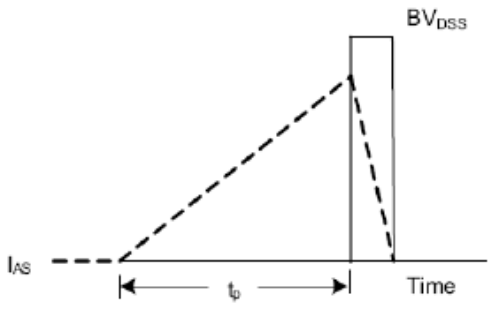


Fig. 4.2 Unclamped Inductive Switching Waveforms