## GENERAL DESCRIPTION

The XR16L784[1] (784) is a quad Universal Asynchronous Receiver and Transmitter (UART). The device is designed for high bandwidth requirement in communication systems. The global interrupt source register provides a complete interrupt status indication for all 4 channels to speed up interrupt parsing. Each UART has its own 16C550 compatible set of configuration registers, transmit and receive FIFOs of 64 bytes, fully programmable transmit and receive FIFO level triggers, transmit and receive FIFO level counters, automatic RTS/CTS or DTR/DSR hardware flow control with programmable hysteresis, automatic software (Xon/Xoff) flow control, IrDA (Infrared Data Association) encoder/decoder, and a 16-bit general purpose timer/counter.

***NOTE:*** *1 Covered by U.S. Patents #5,649,122 and #5,949,787*

### *APPLICATIONS*

- Remote Access Servers
- Ethernet Network to Serial Ports
- Network Management
- Factory Automation and Process Control
- Point-of-Sale Systems
- Multi-port RS-232/RS-422/RS-485 Cards

### *FEATURES*

- 2.97V to 5.5V operation with 5V Tolerant Inputs
- 8-bit Intel or Motorola Data Bus Interface
- Single Open Drain Interrupt output for all 4 channels
- Global Interrupt Source Registers for all channels
- 5G (Fifth Generation) "Flat" Register Set
- Each UART is Independently Controlled with:
  - 16C550 Compatible Registers
  - 64-byte Transmit and Receive FIFOs
  - Transmit and Receive FIFO Level Counters
  - Programmable TX and RX FIFO Trigger Levels
  - Automatic RTS/CTS or DTR/DSR Flow Control
  - Selectable RTS Flow Control Hysteresis
  - Automatic Xon/Xoff Software Flow Control
  - Automatic RS485 Half-duplex Control Output with 16 Selectable Turn-around Delay
  - Infrared (IrDA 1.1) Data Encoder/Decoder
  - Programmable Data Rate with Prescaler
  - Up to 3.12 (16x) and 6.25 (8x) Mbps Data Rate
- A General Purpose 16-bit Timer/Counter
- Sleep Mode with Automatic Wake-up Indicator
- 64-pin LQFP Package (10x10x1.4 mm)

**FIGURE 1. BLOCK DIAGRAM**

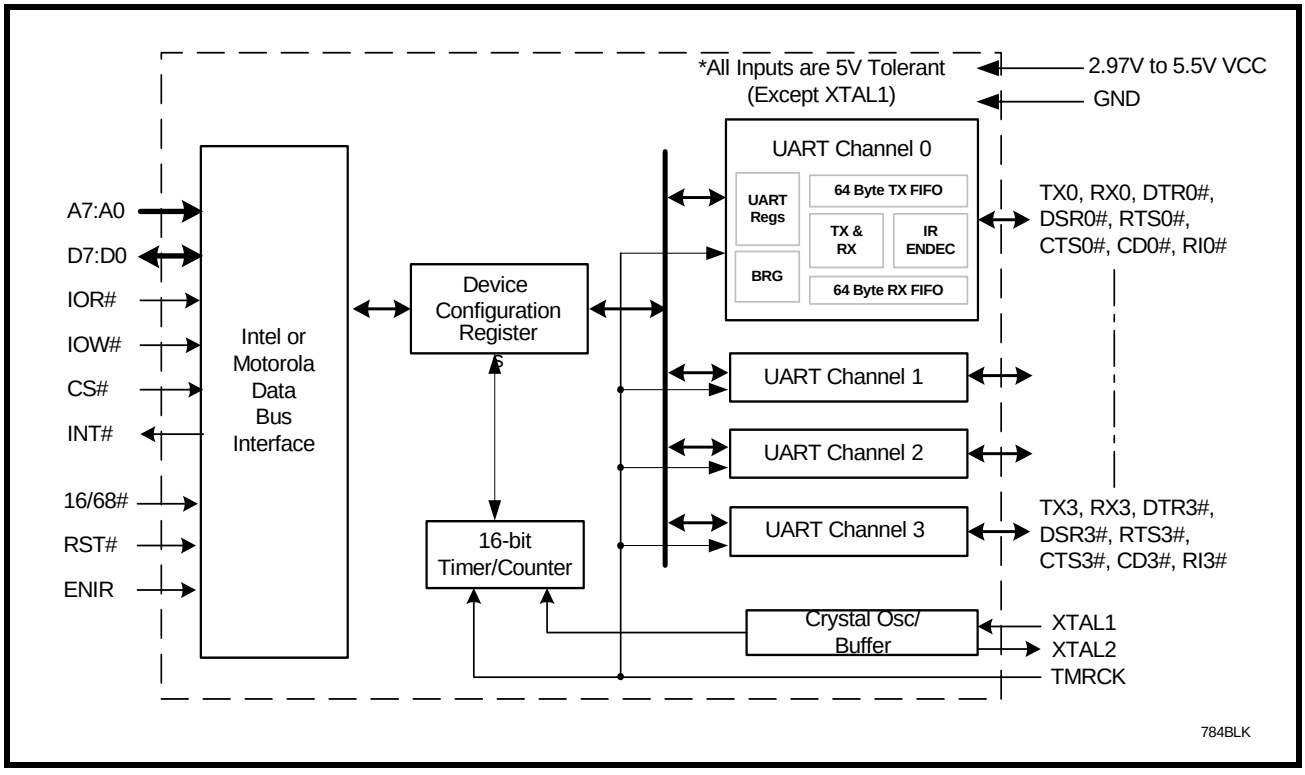
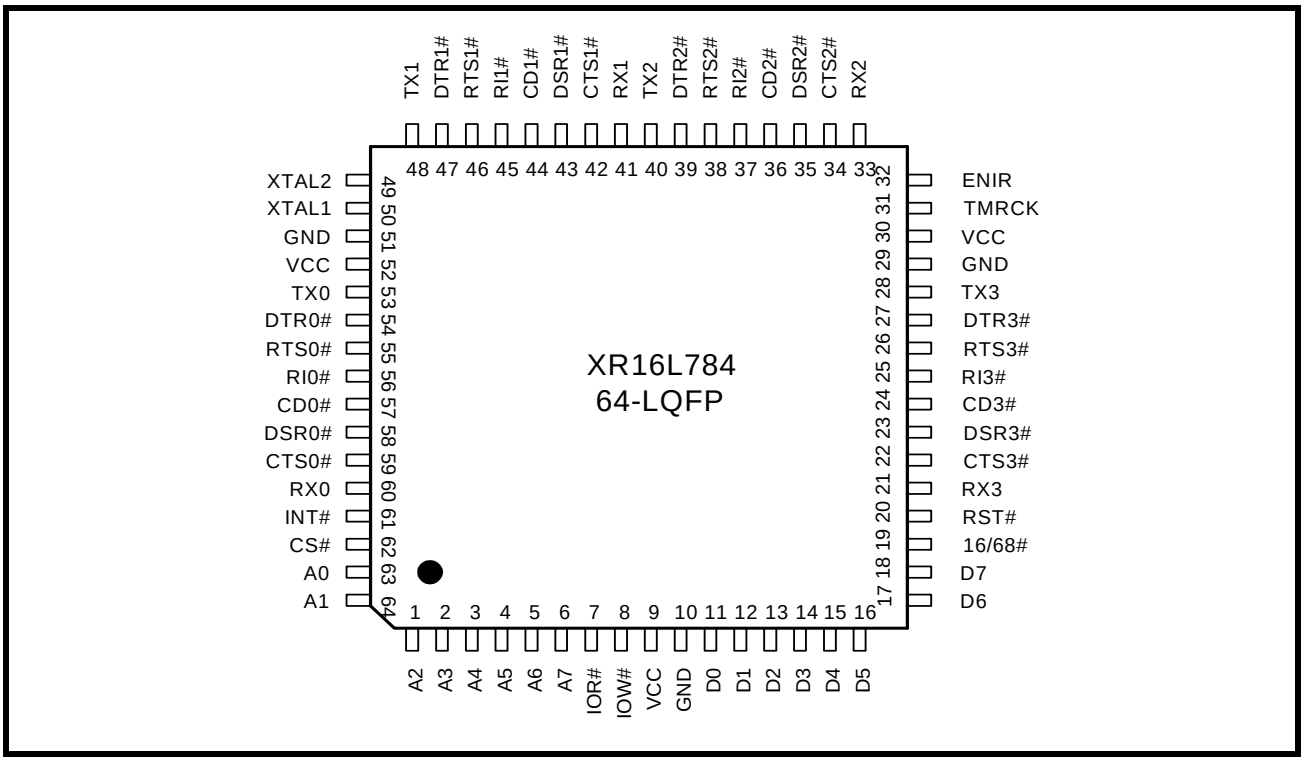


**FIGURE 2. PIN OUT ASSIGNMENT**




## *ORDERING INFORMATION*

| PART NUMBER | PACKAGE | OPERATING TEMPERATURE RANGE | DEVICE STATUS |
|---|---|---|---|
| XR16L784CV | 64-Lead LQFP | 0°C to +70°C | Active |
| XR16L784IV | 64-Lead LQFP | -40°C to +85°C | Active |

# PIN DESCRIPTIONS

## Pin Descriptions

| NAME | PIN # | TYPE | DESCRIPTION |
|---|---|---|---|
| **DATA BUS INTERFACE** | | | |
| A7-A0 | 6-1,64,63 | I | Address data lines [7:0]. A0:A3 selects individual UART's 16 configuration registers, A4:A6 selects UART channel 0 to 3, and A7 selects the global device configuration registers |
| D7:D0 | 18-11 | IO | Data bus lines (7:0] (bidirectional). |
| IOR# | 7 | I | When 16/68# pin is HIGH, it selects Intel bus interface and this input is read strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A7:A0], puts it on the data bus to allow the host processor to read it on the leading edge.<br>When 16/68# pin is LOW, it selects Motorola bus interface and this input should be connected to VCC. |
| IOW#<br>(R/W#) | 8 | I | When 16/68# pin is HIGH, it selects Intel bus interface and this input becomes write strobe (active low). The falling edge instigates the internal write cycle and the leading edge transfers the data byte on the data bus to an internal register pointed by the address lines.<br>When 16/68# pin is LOW, it selects Motorola bus interface and this input becomes read (logic 1) and write (logic 0) signal. |
| CS# | 62 | I | When 16/68# pin is HIGH, this input is chip select (active low) to enable the XR16L784 device.<br>When 16/68# pin is LOW, this input becomes the read and write strobe (active low) for the Motorola bus interface. |
| INT# | 61 | OD | Global interrupt output from XR16L784 (open drain, active low). This output requires an external pull-up resistor (47K-100K ohms) to operate properly. It may be shared with other devices in the system to form a single interrupt line to the host processor and have the software driver polls each device for the interrupt status. |
| **MODEM OR SERIAL I/O INTERFACE** | | | |
| TX0 | 53 | O | UART channel 0 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW. |
| RX0 | 60 | I | UART channel 0 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via FCTR bit-4. If this bit is a logic 0, a LOW on the RXD input is considered a mark and if this bit is a logic 1, a HIGH on the RXD input is considered a space. |
| RTS0# | 55 | O | UART channel 0 Request to Send or general purpose output (active low). This port must be asserted prior using for one of two functions:<br>1) auto RTS flow control, see EFR bit-6, MCR bits-1 & 2, FCTR bits 0-3 and IER bit-6<br>2) Auto RS485 half-duplex direction control, see FCTR bit-5, MCR bit-2 and MSR bits 4-7. |
| CTS0# | 59 | I | UART channel 0 Clear to Send or general purpose input (active low). It can be used for auto CTS flow control, see EFR bit-7, MCR bit-2 and IER bit-7. |

## Pin Descriptions

| NAME | PIN # | TYPE | DESCRIPTION |
|---|---|---|---|
| DTR0# | 54 | O | UART channel 0 Data Terminal Ready or general purpose output (active low).<br>This port must be asserted prior using for one of two functions:<br>1) auto DTR flow control, see EFR bit-6, FCTR bits-0 to 3, MCR bits-0 & 2, and IER bit-6<br>2) Auto RS485 half-duplex direction control, see FCTR bit-5, MCR bit-2 and MSR bit 4-7. |
| DSR0# | 58 | I | UART channel 0 Data Set Ready or general purpose input (active low). It can be used for auto DSR flow control, see EFR bit-7, MCR bit-2 and IER bit-7. |
| CD0# | 57 | I | UART channel 0 Carrier Detect or general purpose input (active low). |
| RI0# | 56 | I | UART channel 0 Ring Indicator or general purpose input (active low). |
| TX1 | 48 | O | UART channel 1 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW. |
| RX1 | 41 | I | UART channel 1 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via FCTR bit-4. If this bit is a logic 0, a LOW on the RXD input is considered a mark and if this bit is a logic 1, a HIGH on the RXD input is considered a space. |
| RTS1# | 46 | O | UART channel 1 Request to Send or general purpose output (active low). See description of RTS0# pin. |
| CTS1# | 42 | I | UART channel 1 Clear to Send or general purpose input (active low). See description of CTS0# pin. |
| DTR1# | 47 | O | UART channel 1 Data Terminal Ready or general purpose output (active low). See description of DTS0# pin. |
| DSR1# | 43 | I | UART channel 1 Data Set Ready or general purpose input (active low). See description of DSR0# pin. |
| CD1# | 44 | I | UART channel 1 Carrier Detect or general purpose input (active low). |
| RI1# | 45 | I | UART channel 1 Ring Indicator or general purpose input (active low). |
| TX2 | 40 | O | UART channel 2 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW. |
| RX2 | 33 | I | UART channel 2 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via FCTR bit-4. If this bit is a logic 0, a LOW on the RXD input is considered a mark and if this bit is a logic 1, a HIGH on the RXD input is considered a space. |
| RTS2# | 38 | O | UART channel 2 Request to Send or general purpose output (active low). See description of RTS0# pin. |
| CTS2# | 34 | I | UART channel 2 Clear to Send or general purpose input (active low). See description of CTS0# pin. |
| DTR2# | 39 | O | UART channel 2 Data Terminal Ready or general purpose output (active low). See description of DTS0# pin. |
| DSR2# | 35 | I | UART channel 2 Data Set Ready or general purpose input (active low). See description of DSR0# pin. |
| CD2# | 36 | I | UART channel 2 Carrier Detect or general purpose input (active low). |
| RI2# | 37 | I | UART channel 2 Ring Indicator or general purpose intput (active low). |

## Pin Descriptions

| NAME | PIN # | TYPE | DESCRIPTION |
|---|---|---|---|
| TX3 | 28 | O | UART channel 3 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW. |
| RX3 | 21 | I | UART channel 3 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via FCTR bit-4. If this bit is a logic 0, a LOW on the RXD input is considered a mark and if this bit is a logic 1, a HIGH on the RXD input is considered a space. |
| RTS3# | 26 | O | UART channel 3 Request to Send or general purpose output (active low). See description of RTS0# pin. |
| CTS3# | 22 | I | UART channel 3 Clear to Send or general purpose input (active low).d. See description of CTS0# pin. |
| DTR3# | 27 | O | UART channel 3 Data Terminal Ready or general purpose output (active low). See description of DTS0# pin. |
| DSR3# | 23 | I | UART channel 3 Data Set Ready or general purpose input (active low). See description of DSR0# pin. |
| CD3# | 24 | I | UART channel 3 Carrier Detect or general purpose input (active low). |
| RI3# | 25 | I | UART channel 3 Ring Indicator or general purpose input (active low). |
| ANCILLARY SIGNALS | | | |
| XTAL1 | 50 | I | Crystal or external clock input. Caution: this input is not 5V tolerant. |
| XTAL2 | 49 | O | Crystal or buffered clock output. |
| TMRCK | 31 | I | 16-bit timer/counter external clock input. |
| ENIR | 32 | I | Infrared mode enable (active high). This pin is sampled during power up, following a hardware reset (RST#) or soft-reset (register RESET). It can be used to start up all 8 UARTs in the infrared mode. The sampled logic state is transferred to MCR bit-6 in the UART. |
| RST# | 20 | I | Reset (active low). The configuration and UART registers are reset to default values, see Table-15. |
| 16/68# | 19 | I | Intel or Motorola data bus interface select. HIGH selects Intel bus interface and LOW selects Motorola interface. This input affects the functionality of IOR#, IOW# and CS# pins. |
| VCC | 9,30,52 | | +5V or +3.3V supply, all inputs are 5V tolerant except for XTAL1. |
| GND | 10,29,51 | | Power supply common, ground. |

***NOTE:*** *Pin type: I=Input, O=Output, IO= Input/output, OD=Output Open Drain.*

## 1.0 DESCRIPTION

The XR16L784 (784) integrates the functions of 4 enhanced 16550 UARTs, a general purpose 16-bit timer/counter and an on-chip oscillator. The device configuration registers include a set of four consecutive interrupt source registers that provides interrupt-status for all 4 UARTs, timer/counter and a sleep wake up indicator. Each UART channel has its own 16550 UART compatible configuration register set for individual channel control, status, and data transfer. Additionally, each UART channel has 64-byte of transmit and receive FIFOs, automatic RTS/CTS or DTR/DSR hardware flow control with hysteresis control, automatic Xon/Xoff and special character software flow control, programmable transmit and receive FIFO trigger levels, FIFO level counters, infrared encoder and decoder (IrDA ver 1.0), programmable baud rate generator with a prescaler of divide by 1 or 4, and data rate up to 6.25 Mbps with 8X sampling clock rate or 3.125Mbps in the 16X rate. The XR16L784 is a 5V and 3.3V device with 5 volt tolerant inputs (except XTAL1).

## 2.0 FUNCTIONAL DESCRIPTIONS

### *2.1 Device Reset*

#### 2.1.1 Hardware Reset

The RST# input resets the internal registers and the serial interface outputs in all 4 channels to their default state (see Table 19). A LOW pulse of longer than 40 ns duration will be required to activate the reset function in the device.

#### 2.1.2 Software Reset

The internal registers of each UART can be reset by writing to the RESET register in the Device Configuration Registers. For more details, see the RESET register description on page 23.

### *2.2 UART Channel Selection*

The UART provides the user with the capability to bi-directionally transfer information between an external CPU and an external serial communication device. A logic 0 on the chip select pins, CS#, allows the user to select one of the UART channels to configure, send transmit data and/or unload receive data to/from the UART. When address line A7 = 0, address lines A5:A4 are used to select one of the eight channels. See **Table 1** below for UART channel selection.

**TABLE 1: UART CHANNEL SELECTION**

| A7 | A6 | A5 | A4 | FUNCTION |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Channel 0 Selected |
| 0 | 0 | 0 | 1 | Channel 1 Selected |
| 0 | 0 | 1 | 0 | Channel 2 Selected |
| 0 | 0 | 1 | 1 | Channel 3 Selected |
| 0 | 1 | X | X | Reserved |

### *2.3 Simultaneous Write to All Channels*

During a write cycle, the setting of REGB bit-0 to a logic 1 will override the channel selection of address A5:A4 and allow a simultaneous write to all 4 UART channels when any channel is written to. This functional capability allow the registers in all 8 UART channels to be modified concurrently, saving individual channel initialization time. Caution should be considered, however, when using this capability. Any in-process serial data transfer may be disrupted by changing an active channel's mode. Also, REGB bit-0 should be reset to a logic 0 before attempting to read from the UART.

### 2.4 INT# Ouput

The INT# interrupt output changes according to the operating mode and enhanced features setup. Table 2 and 3 summarize the operating behavior for the transmitter and receiver.

**TABLE 2: INT# PIN OPERATION FOR TRANSMITTER**

| | Auto RS485 Mode | FCR BIT-0 = 0 (FIFO DISABLED) | FCR BIT-0 = 1 (FIFO ENABLED) |
|---|---|---|---|
| INT# Pin | NO | HIGH = a byte in THR<br>LOW = THR empty | HIGH = FIFO above trigger level<br>LOW = FIFO below trigger level or FIFO empty |
| INT# Pin | YES | HIGH = a byte in THR<br>LOW = transmitter empty | HIGH = FIFO above trigger level<br>LOW = FIFO below trigger level or transmitter empty |

**TABLE 3: INT# PIN OPERATION FOR RECEIVER**

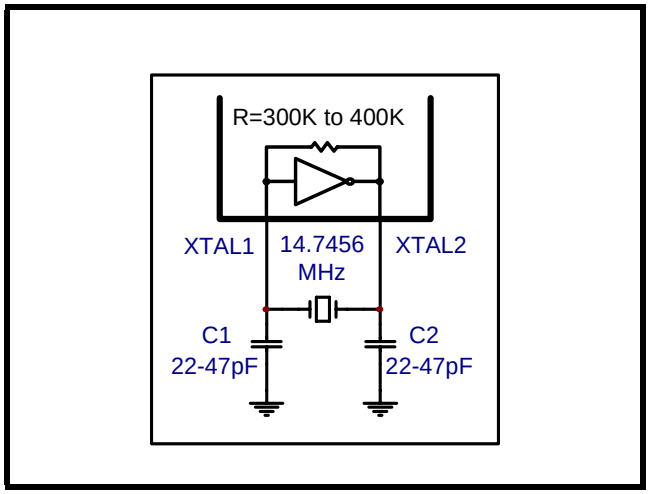
| | FCR BIT-0 = 0 (FIFO DISABLED) | FCR BIT-0 = 1 (FIFO ENABLED) |
|---|---|---|
| INT# Pin | HIGH = no data<br>LOW = 1 byte | HIGH = FIFO below trigger level<br>LOW = FIFO above trigger level |

### 2.5 CRYSTAL OSCILLATOR / BUFFER

The 784 includes an on-chip oscillator (XTAL1 and XTAL2). The crystal oscillator provides the system clock to the Baud Rate Generators (BRG) in each of the 8 UARTs, the 16-bit general purpose timer/counter and internal logics. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. For programming details, see **"Section 2.6, Programmable Baud Rate Generator" on page 8**.

The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see Figure 3). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal 8 baud rate generators for standard or custom rates. Typically, the oscillator connections are shown in Figure 3. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

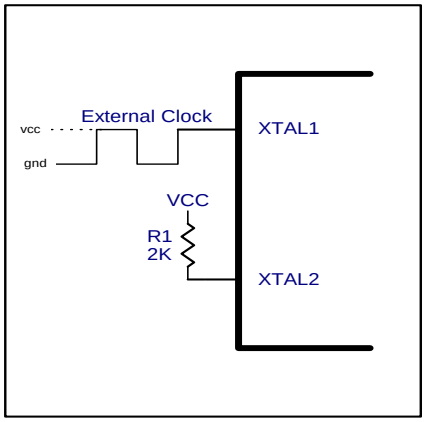
**FIGURE 3. TYPICAL OSCILLATOR CONNECTIONS**



### 2.6 Programmable Baud Rate Generator

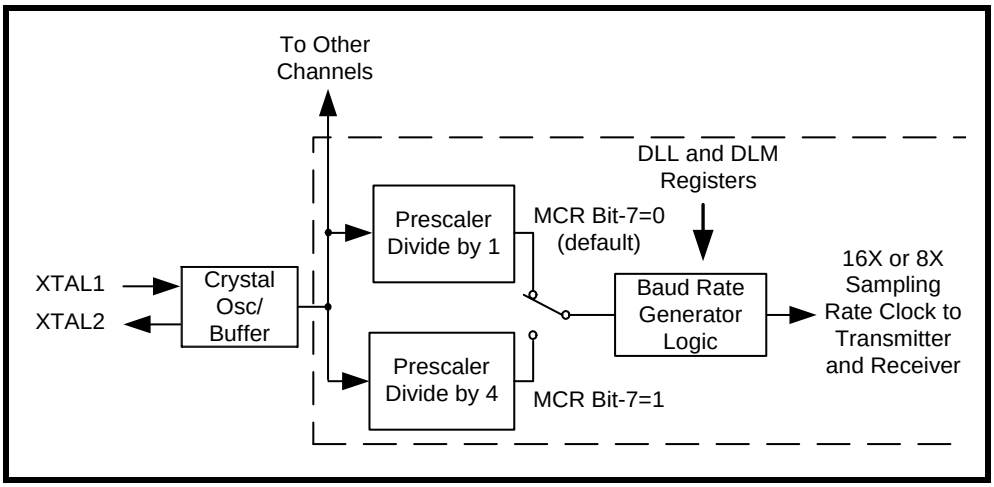
A single Baud Rate Generator (BRG) is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of operating with a crystal frequency of up to 24 MHz. However, with an external clock input on XTAL1 pin and a 2K ohms pull-up resistor on XTAL2 pin (as shown in **Figure 4**) it can extend its operation up to 50 MHz (3.125 Mbps serial data rate) at room temperature and 5.0V.

**FIGURE 4. EXTERNAL CLOCK CONNECTION FOR EXTENDED DATA RATE**




Each UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter and receiver. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The output of the prescaler clocks to the BRG. The BRG further divides this clock by a programmable divisor between 1 and ($2^{16}$ -1) to obtain a 16X or 8X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL and DLM registers) defaults to a random value upon power up. Therefore, the BRG must be programmed during initialization to the operating data rate.

**FIGURE 5. BAUD RATE GENERATOR**



Programming the Baud Rate Generator Registers DLM and DLL provides the capability of selecting the operating data rate. Table 4 shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X clock rate. At 8X sampling rate, these data rates would double. When using a non-standard data rate crystal or external clock, the divisor value can be calculated for channel 'N' with the following equation(s).

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16), **WHEN 8XMODE-BIT N IS 0**

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 8), **WHEN 8XMODE-BIT N IS 1**

**TABLE 4: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING**

| OUTPUT Data Rate MCR Bit-7=1 | OUTPUT Data Rate MCR Bit-7=0 | DIVISOR FOR 16X Clock (Decimal) | DIVISOR FOR 16X Clock (HEX) | DLM PROGRAM VALUE (HEX) | DLL PROGRAM VALUE (HEX) | DATA RATE ERROR (%) |
|---|---|---|---|---|---|---|
| 100 | 400 | 2304 | 900 | 09 | 00 | 0 |
| 600 | 2400 | 384 | 180 | 01 | 80 | 0 |
| 1200 | 4800 | 192 | C0 | 00 | C0 | 0 |
| 2400 | 9600 | 96 | 60 | 00 | 60 | 0 |
| 4800 | 19.2k | 48 | 30 | 00 | 30 | 0 |
| 9600 | 38.4k | 24 | 18 | 00 | 18 | 0 |
| 19.2k | 76.8k | 12 | 0C | 00 | 0C | 0 |
| 38.4k | 153.6k | 6 | 06 | 00 | 06 | 0 |
| 57.6k | 230.4k | 4 | 04 | 00 | 04 | 0 |
| 115.2k | 460.8k | 2 | 02 | 00 | 02 | 0 |
| 230.4k | 921.6k | 1 | 01 | 00 | 01 | 0 |

## *2.7 Transmitter*

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 64 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X internal clock. A bit time is 16 clock periods (see EMSR bit-7). The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

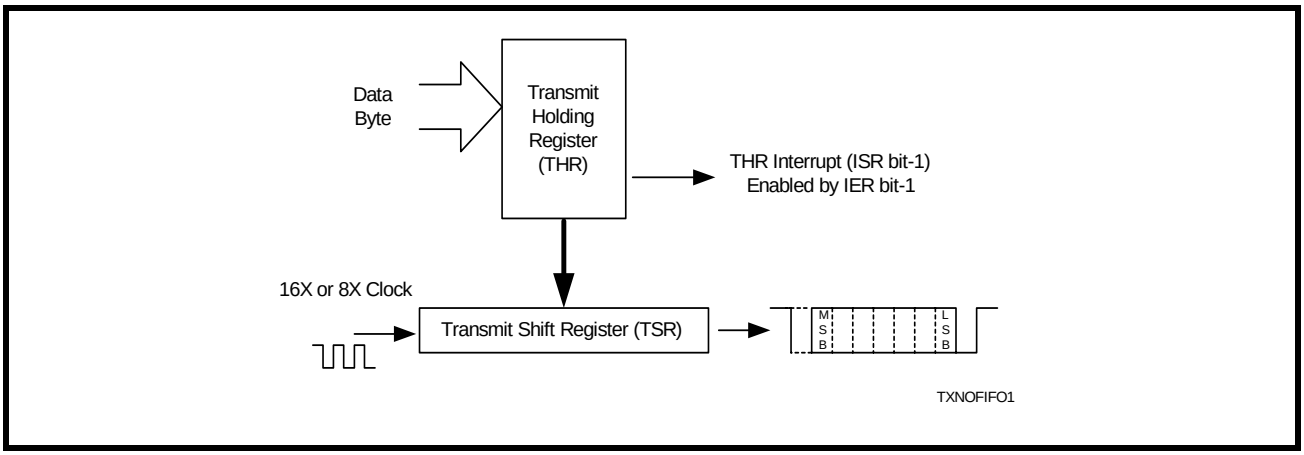
### 2.7.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 64 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

### 2.7.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

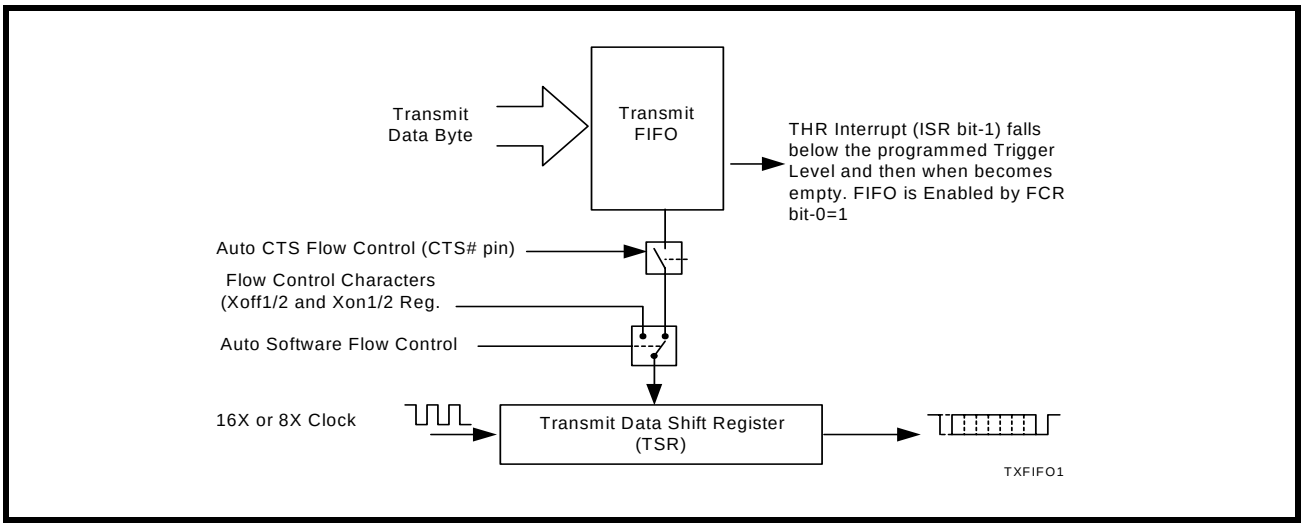
FIGURE 6. TRANSMITTER OPERATION IN NON-FIFO MODE




### 2.7.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 64 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 7. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE




## *2.8 Receiver*

The receiver section contains an 8-bit Receive Shift Register (RSR) and 64 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

### 2.8.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 64 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

**FIGURE 8. RECEIVER OPERATION IN NON-FIFO MODE**

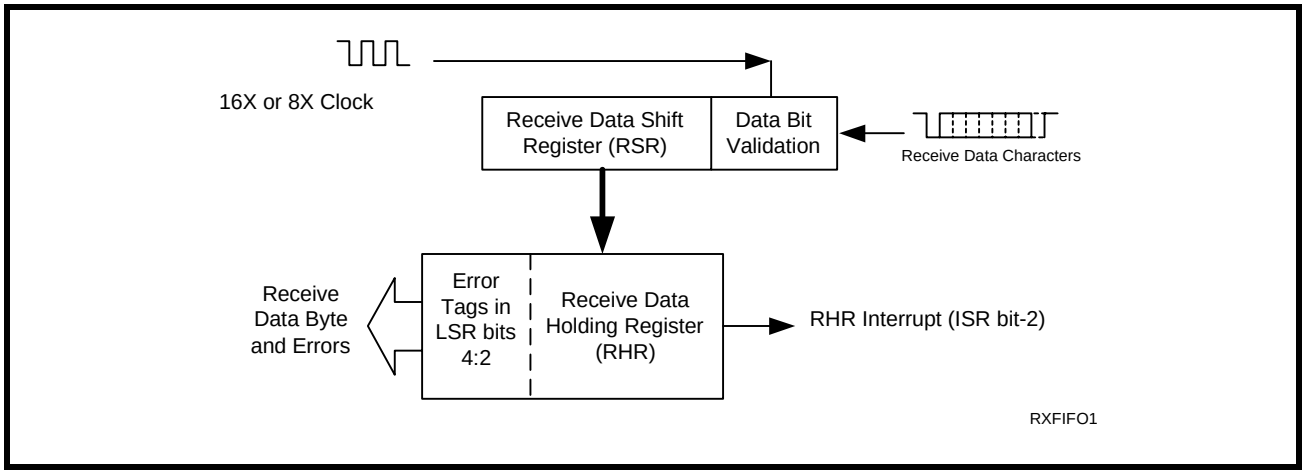
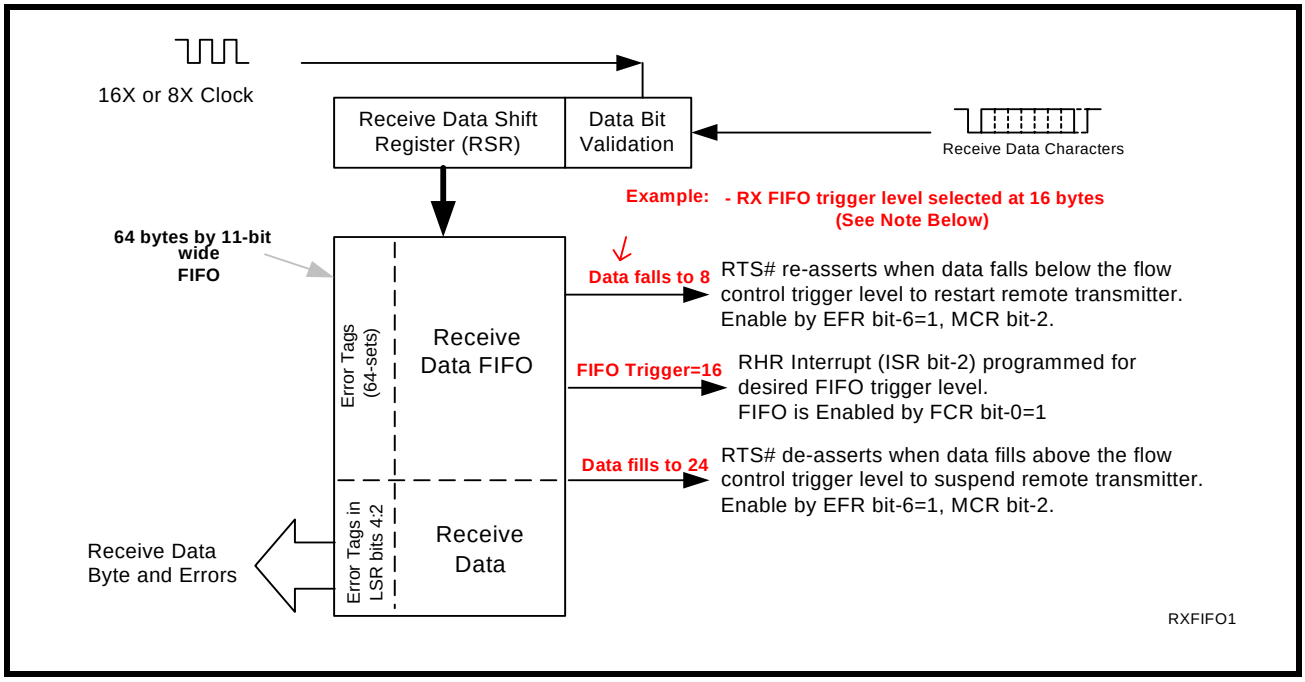



**FIGURE 9. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE**




***NOTE:*** *Table-B selected as Trigger Table for* **Figure 9** *(Table 14).*

### 2.9 THR and RHR Register Locations

The THR and RHR register addresses for channel 0 to channel 7 is shown in Table 5 below. The THR and RHR for channels 0 to 3 are located at address 0x00, 0x10, 0x20 and 0x30 respectively. Transmit data byte is loaded to the THR when writing to that address and receive data is unloaded from the RHR register when reading that address. Both THR and RHR registers are 16C550 compatible in 8-bit format, so each bus operation can only write or read in bytes.

**TABLE 5: TRANSMIT AND RECEIVE DATA REGISTER, 16C550 COMPATIBLE**

**THR and RHR Address Locations For CH0 to CH3 (16C550 Compatible)**

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| CH0 | 0x00 | Write THR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
| CH0 | 0x00 | Read RHR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
| CH1 | 0x10 | Write THR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
| CH1 | 0x10 | Read RHR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
| CH2 | 0x20 | Write THR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
| CH2 | 0x20 | Read RHR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
| CH3 | 0x30 | Write THR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
| CH3 | 0x30 | Read RHR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |

784THRRHR1

### 2.10 Automatic RTS/DTR Hardware Flow Control Operation

Automatic RTS/DTR flow control is used to prevent data overrun to the local receiver FIFO. The RTS#/DTR# output pin is used to request remote unit to suspend/resume data transmission. The flow control features are individually selected to fit specific application requirement (see Figure 10):

- Select RTS (and CTS) or DTR (and DSR) through MCR bit-2.
- Enable auto RTS/DTR flow control using EFR bit-6.
- The auto RTS or auto DTR function must be started by asserting the RTS# or DTR# output pin (MCR bit-1 or bit-0 to a logic 1, respectively) after it is enabled.
- If using programmable RX FIFO trigger levels, hysteresis levels can be selected via FCTR bits 3-0.

With the Auto RTS function enabled, the RTS# output pin will not be de-asserted (HIGH) when the receive FIFO reaches the programmed trigger level, but will be de-asserted when the FIFO reaches the next trigger level for Trigger Tables A-C (See Table 14). The RTS# output pin will be asserted (LOW) again after the FIFO is unloaded to the next trigger level below the programmed trigger level.

For Trigger Table D (or programmable trigger levels), the RTS# output pin is de-asserted when the the RX FIFO level reaches the RX trigger level plus the hysteresis level and is asserted when the RX FIFO level falls below the RX trigger level minus the hysteresis level.

However, even under these conditions, the 788 will continue to accept data until the receive FIFO is full if the remote UART transmitter continues to send data.

- If used, enable RTS/DTR interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS#/DTR# pin makes a transition: ISR bit-5 will be set to 1.

### 2.10.1 Auto CTS/DSR Flow Control

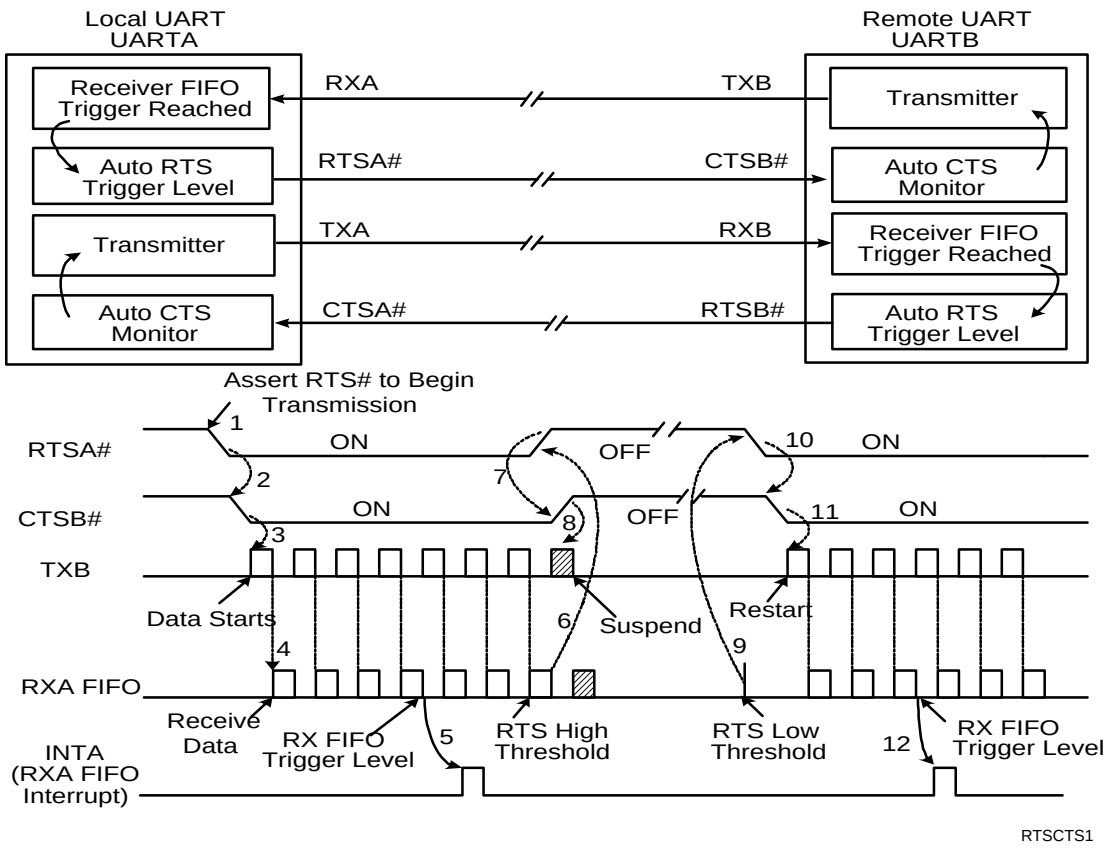
Automatic CTS/DSR flow control is used to prevent data overrun to the remote receiver FIFO. The CTS/DSR pin is monitored to suspend/restart local transmitter. The flow control features are individually selected to fit specific application requirement (see **Figure 10**):

- Select CTS (and RTS) or DSR (and DTR) through MCR bit-2.
- Enable auto CTS/DSR flow control using EFR bit-7.

With the Auto CTS or Auto DTR function enabled, the UART will suspend transmission as soon as the stop bit of the character in the Transmit Shift Register has been shifted out. Transmission is resumed after the CTS#/DTR# input is re-asserted (logic 0), indicating more data may be sent.

- If used, enable CTS/DSR interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS#/DSR# pin makes a transition: ISR bit-5 will be set to a logic 1, and UART will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS#/DSR# input returns LOW, indicating more data may be sent.

**FIGURE 10. AUTO RTS/DTR AND CTS/DSR FLOW CONTROL OPERATION**




*The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.*

### 2.11 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (See Table 18), the 784 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the 784 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the 784 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the 784 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset, any desired Xon/Xoff value can be used for software flow control. Different conditions can be set to detect Xon/Xoff characters (See Table 18) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the 784 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the 784 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The 784 sends the Xoff-1,2 characters two character times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level (for all trigger tables A-D). To clear this condition, the 784 will transmit the programmed Xon-1,2 characters as soon as receive FIFO is less than one trigger level below the programmed trigger level (for Trigger Tables A, B, and C) or when receive FIFO is less than the trigger level minus the hysteresis value (for Trigger Table D). This hysteresis value is the same as the Auto RTS/DTR Hysteresis value in **Table 17**. **Table 6** below explains this when Trigger Table-B (See **Table 14**) is selected.

**TABLE 6: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL**

| RX TRIGGER LEVEL | INT PIN ACTIVATION | XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO) | XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO) |
|---|---|---|---|
| 8 | 8 | 8* | 0 |
| 16 | 16 | 16* | 8 |
| 24 | 24 | 24* | 16 |
| 28 | 28 | 28* | 24 |

** After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2 characters); for example, after 2.083ms has elapsed for 9600 baud and 10-bit word length setting.*

### 2.12 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The 784 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the Xon, Xoff Registers corresponds with the LSB bit for the receive character.

### 2.13 Auto RS485 Half-duplex Control

The auto RS485 half-duplex direction control changes the behavior of the transmitter when enabled by FCTR bit-5. It asserts RTS# or DTR# (LOW) after a specified delay indicated in MSR[7:4] following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote station's response. The delay optimizes the time needed for the last transmission to reach the farthest station on a long cable network before switching off the line driver. This delay prevents undesirable line signal disturbance that causes signal degradation. When the host is ready to transmit next polling data packet again, it only has to load data bytes to the transmit FIFO. The transmitter automatically de-asserts RTS# or DTR# output (HIGH) prior to sending the data. The auto RS485 half-duplex direction control also changes the transmitter empty interrupt to TSR empty instead of THR empty.

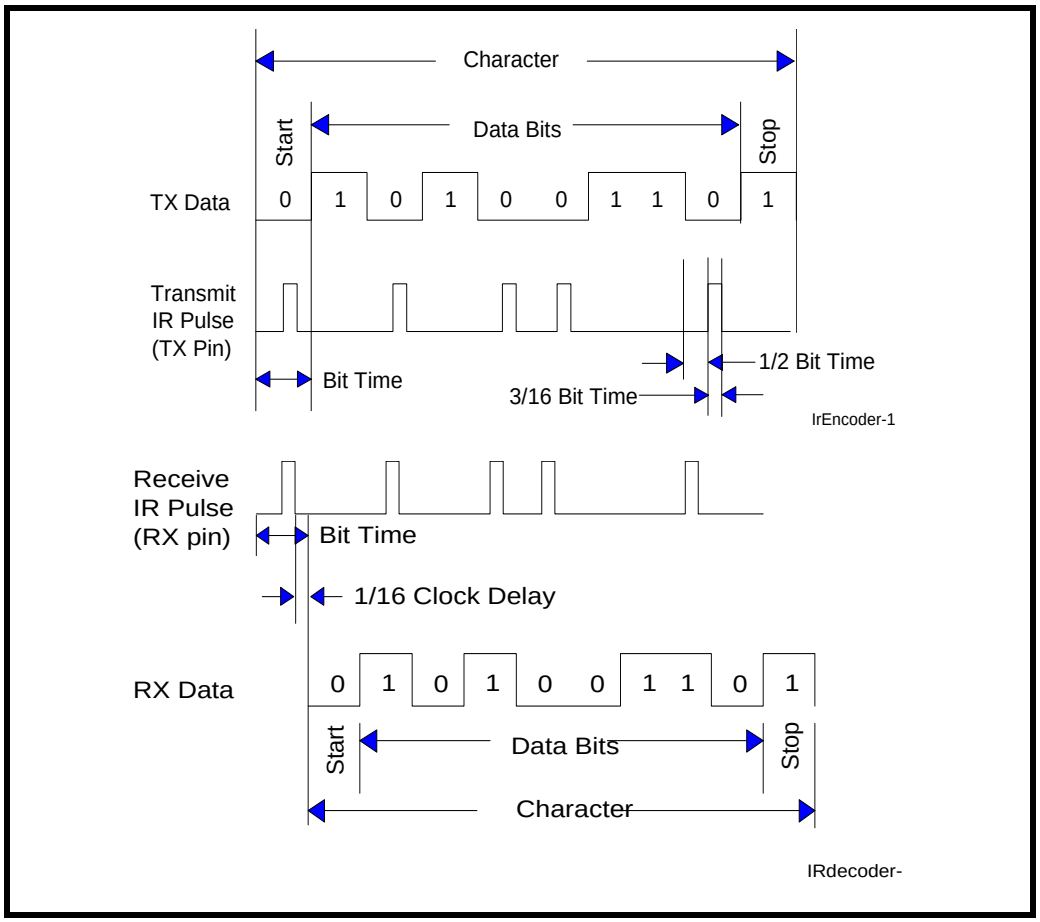
### 2.14 Infrared Mode

Each UART in the 784 includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The input pin ENIR conveniently activates all 8 UART channels to start up in the infrared mode. Note that the ENIR pin is sampled when the RST# input is de-asserted. This global control pin enables the MCR bit-6 function in every UART channel register. After power up or a reset, the software can overwrite MCR bit-6 if so desired. ENIR and MCR bit-6 also disable the receiver while the transmitter is sending data. This prevents echoed data from reaching the receiver. The global activation ENIR pin prevents the infrared emitter from turning on and drawing large amount of current while the system is starting up. When the infrared feature is enabled, the transmit data outputs, TX[3:0], would idle at logic zero level. Likewise, the RX [3:0] inputs assume an idle level of logic zero.

The infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each "0" bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See **Figure 11**.

The infrared decoder receives the input pulse from the infrared sensing diode on RX pin. Each time it senses a light pulse, it returns a logic zero to the data bit stream. The decoder also accepts (when FCTR bit-4 = 1) an inverted IR-encoded input signal. This option supports active low instead of normal active high pulse from some infrared modules on the market.

**FIGURE 11. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING**



### 2.15 Sleep Mode with Wake-Up Indicator

The 784 supports low voltage system designs, hence, a sleep mode is included to reduce its power consumption when the chip is not actively used.

All of these conditions must be satisfied for the 784 to enter sleep mode:

- no interrupts pending for all 8 channels of the 784 (ISR bit-0 = 1)
- SLEEP register = 0x0F
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pin of all 4 channels are idling HIGH

The 784 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The 784 resumes normal operation by any of the following:

- a receive data start bit transition (HIGH to LOW)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

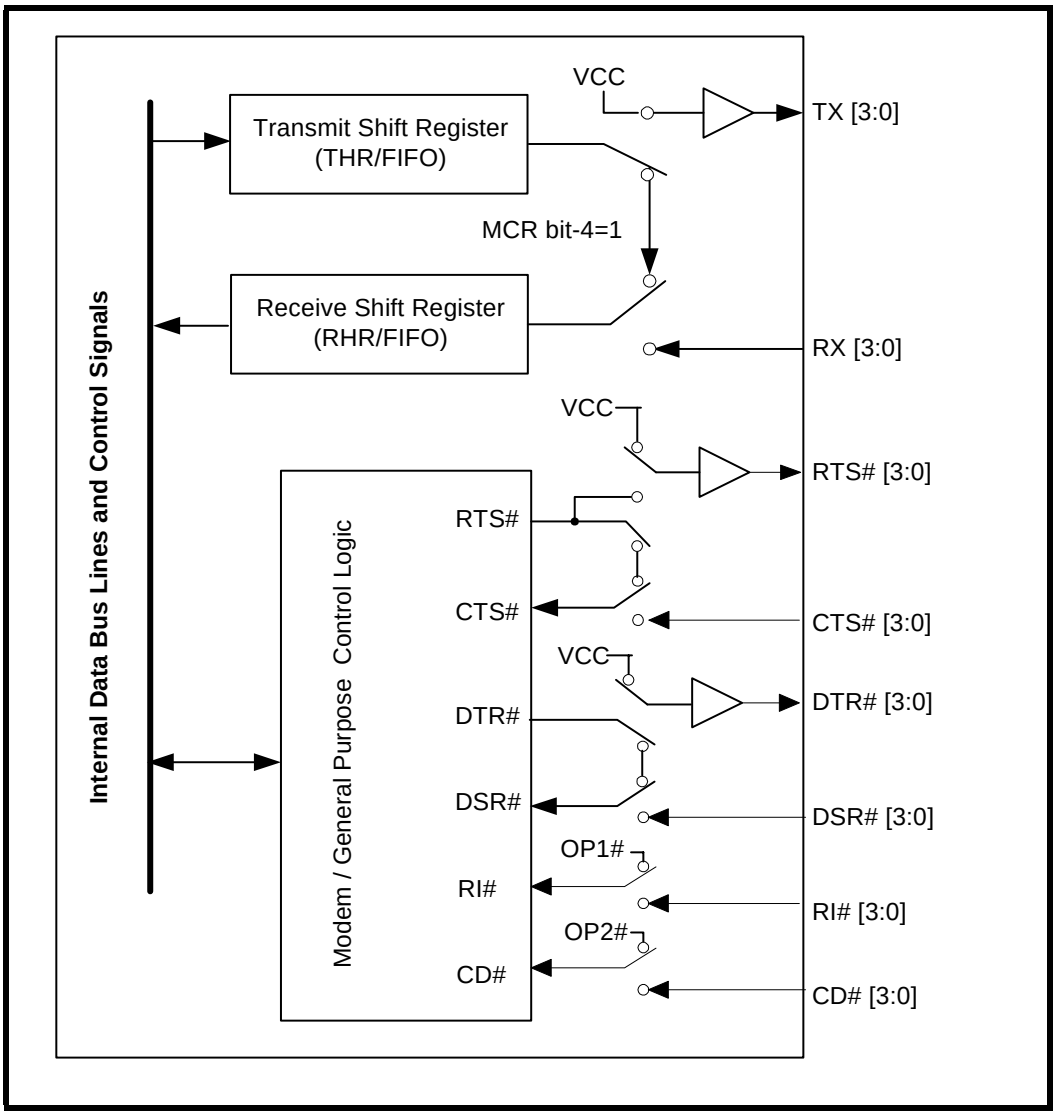
If the 784 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the 784 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending in any channel. Also, a special interrupt is generated with an indication of no pending interrupt. Reading INT0 will clear this special interrupt. The 784 will stay in the sleep mode of operation until it is disabled by setting SLEEP = 0x00.

A word of caution: owing to the starting up delay of the crystal oscillator after waking up from sleep mode, the first few receive characters may be lost. The number of characters lost during the restart also depends on your operating data rate. More characters are lost when operating at higher data rate.

### 2.16 Internal Loopback

Each UART channel provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 12 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX, RTS# and DTR# pins are held HIGH (idle or de-asserted state), and the CTS#, DSR# CD# and RI# inputs are ignored.

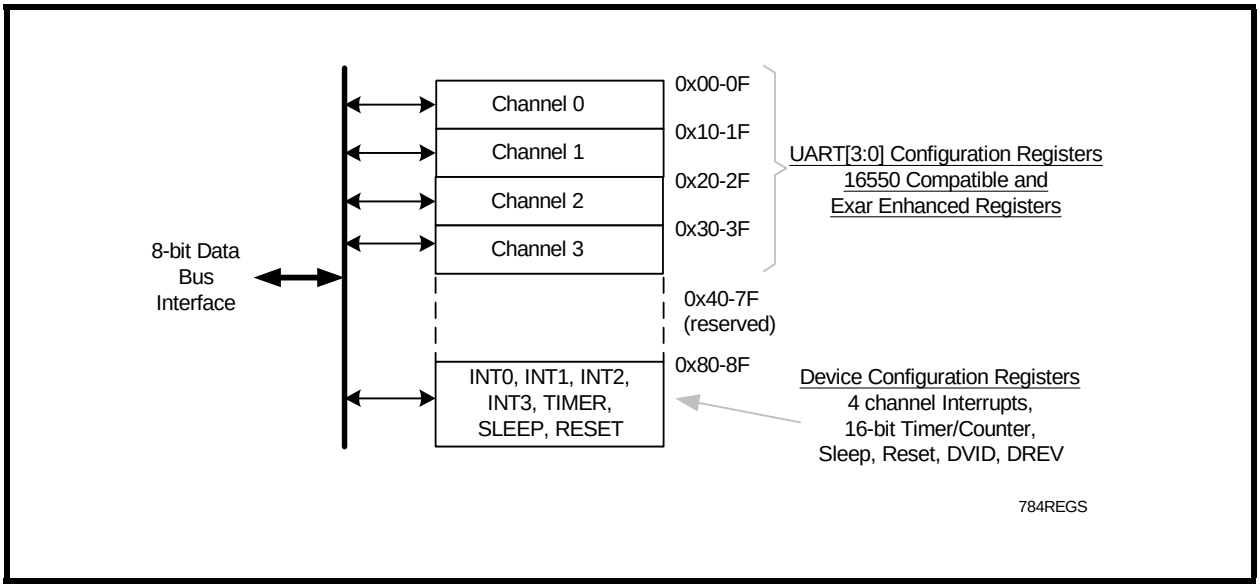
**FIGURE 12. INTERNAL LOOP BACK**



## 3.0 XR16L784 REGISTERS

The XR16L784 quad UART register set consists of the Device Configuration Registers that are accessible directly from the data bus for programming general operating conditions of the UARTs and monitoring the status of various functions. These functions include all 4 channel UART's interrupt control and status, 16-bit general purpose timer control and status, sleep mode, soft-reset, and device identification and revision. Also, each UART channel has its own set of internal UART Configuration Registers for its own operation control, status reporting and data transfer. These registers are mapped into a 256-byte of the data memory address space. The following paragraphs describe all the registers in detail.

**FIGURE 13. THE XR16L784 REGISTERS MAPPING**




### 3.1 DEVICE CONFIGURATION REGISTER SET

The device configuration registers are directly accessible from the bus. This provides easy programming of general operating parameters to the 784 UART and for monitoring the status of various functions. The device configuration registers are mapped onto address 0x80-8F as shown on the register map in **Table 8** and **Figure 13**. These registers provide global controls and status of all 4 channel UARTs that include interrupt status, 16-bit general purpose timer control and status, 8X or 16X sampling clock, sleep mode control, soft-reset control, simultaneous UART initialization, and device identification and revision.

.

**TABLE 7: XR16L784 REGISTER SETS**

| ADDRESS [A7:A0] | UART CHANNEL SPACE | REFERENCE | COMMENT |
|---|---|---|---|
| 0x00 - 0x0F | UART channel 0 Registers | (**Table 11** & 12) | First 8 registers are 16550 compatible |
| 0x10 - 0x1F | UART channel 1 Registers | (**Table 11** & 12) | |
| 0x20 - 0x2F | UART channel 2 Registers | (**Table 11** & 12) | |
| 0x30 - 0x3F | UART channel 3 Registers | (**Table 11** & 12) | |
| 0x40 - 0x7F | None | | Reserved |
| 0x80 - 0x8F | Device Configuration Registers | (**Table 8**) | Interrupt registers and global controls |

**TABLE 8: DEVICE CONFIGURATION REGISTERS**

| ADDRESS [A7:A0] | READ/ WRITE | REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x80 | R | INT0 Source | Rsvd | Rsvd | Rsvd | Rsvd | UART 3 | UART 2 | UART 1 | UART 0 |
| 0x81 | R | INT1 | UART 2 bit 1 | source bit 0 | UART 1 bit 2 | interrupt bit 1 | source bit 0 | UART 0 bit 2 | interrupt bit 1 | source bit 0 |
| 0x82 | R | INT2 | Rsvd | Rsvd | Rsvd | Rsvd | UART 3 bit 2 | interrupt bit 1 | source bit 0 | UART 2 bit 2 |
| 0x83 | R | INT3 | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd |
| 0x84 | R/W | TIMER CTRL | 0 | 0 | 0 | 0 | clock source | function select | start timer | enable timer INT |
| 0x85 | R | TIMER | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x86 | R/W | TIMER LSB | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x87 | R/W | TIMER MSB | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x88 | R/W | 8X MODE | Rsvd | Rsvd | Rsvd | Rsvd | UART 3 | UART 2 | UART 1 | UART 0 |
| 0x89 | R | REG 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x8A | W | RESET | Rsvd | Rsvd | Rsvd | Rsvd | Reset UART 3 | Reset UART 2 | Reset UART 1 | Reset UART 0 |
| 0x8B | R/W | SLEEP | Rsvd | Rsvd | Rsvd | Rsvd | Enable sleep UART 3 | Enable sleep UART 2 | Enable sleep UART 1 | Enable sleep UART 0 |
| 0x8C | R | DREV | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x8D | R | DVID | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x8E | R/W | REG 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Write to all UARTs |

### 3.1.1 The Global Interrupt Source Registers

The XR16L784 has a global interrupt source register set that consists of 4 consecutive registers [INT0, INT1, INT2 and INT3]. Register INT3 is not used in the 784 UART, only in the 8-channel XR16L788. The 3 registers are in the device configuration register address space.

| | | | |
|---|---|---|---|
| INT3 (Rsvd)<br>[0x00] | INT2<br>[0x00] | INT1<br>[0x00] | INT0<br>[0x00] |

All 4 registers default to logic zero (as indicated in square braces) for no interrupt pending. All 4 channel interrupts are enabled or disabled in each channel's IER register. INT0 shows individual status for each channel while INT1 and INT2 show the details of the source of each channel's interrupt with its unique 3-bit encoding. **Figure 14** shows the 4 interrupt registers in sequence for clarity. The 16-bit timer and sleep wake-up interrupts are masked in the device configuration registers, TIMERCNTL and SLEEP. An interrupt is generated by the 784 when awakened from sleep if all 4 channels were placed in the sleep mode previously. Reading INT0 will clear this wake-up interrupt.

Each bit in the INT0 register gives an indication of the channel that has requested service.

#### *3.1.1.1 INT0 Channel Interrupt Indicator:*

**INT0 Register**
Individual UART Channel Interrupt Status

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|---|---|---|---|---|---|---|---|
| Rsvd | Rsvd | Rsvd | Rsvd | Ch-3 | Ch-2 | Ch-1 | Ch-0 |

For example, bit-0 represents channel 0 and bit-3 indicates channel 3. Bits 4 to 7 are reserved and remains at logic zero. Logic one indicates the channel N [3:0] has called for service. The interrupt bit clears after reading the appropiate register of the interrupting UART channel register (ISR, LSR and MSR). **See Table 13** for interrupt clearing details.

#### *3.1.1.2 INT1 and INT2 Interrupt Source Locator*

INT2 and INT1 provide a 12-bit (3 bits per channel) encoded interrupt indicator. **Table 9** shows the 3 bit encoding and their priority order. The 16-bit Timer time-out interrupt will show up only as a channel 0 interrupt . For other channels, interrupt 7 is reserved.

**FIGURE 14. THE GLOBAL INTERRUPT REGISTERS, INT0, INT1, INT2 AND INT3**

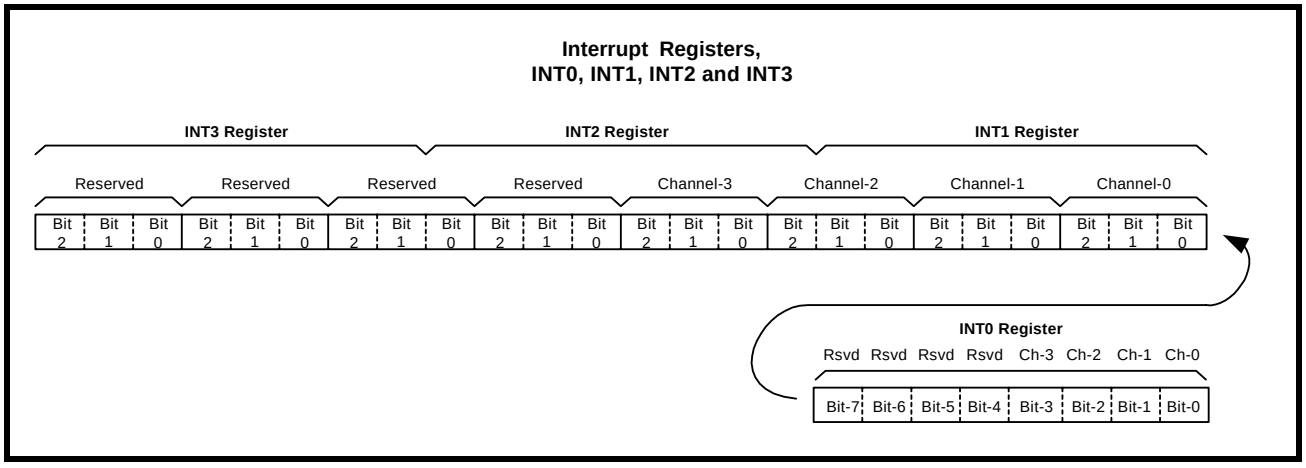


**TABLE 9: UART CHANNEL [3:0] INTERRUPT SOURCE ENCODING AND CLEARING**

| PRIORITY | BIT2 | BIT1 | BIT0 | INTERRUPT SOURCE(S) AND CLEARING |
|---|---|---|---|---|
| x | 0 | 0 | 0 | None |
| 1 | 0 | 0 | 1 | RXRDY & RX Line Status (logic OR of LSR[4:1]). RXRDY INT clears by reading data in the RX FIFO until it falls below the trigger level; RX Line Status INT cleared after reading LSR register. |
| 2 | 0 | 1 | 0 | RXRDY Time-out: Cleared when the FIFO becomes empty. |
| 3 | 0 | 1 | 1 | TXRDY, THR or TSR (auto RS485 mode) empty, clears after reading ISR register. |
| 4 | 1 | 0 | 0 | MSR, RTS/CTS or DTR/DSR delta or Xoff/Xon or special character detected. The first two clear after reading MSR register; Xoff/Xon or special char. detect INT clears after reading ISR register. |
| 5 | 1 | 0 | 1 | Reserved. |
| 6 | 1 | 1 | 0 | Reserved. |
| 7 | 1 | 1 | 1 | TIMER Time-out, shows up as a channel 0 INT. It clears after reading the TIMERCNTL register. Reserved in other channels. |

### 3.1.2 General Purpose 16-bit Timer/Counter. [TIMERMSB, TIMELSB, TIMER, TIMECNTL] (DEFAULT 0XXX-XX-00-00)

A 16-bit down-count timer for general purpose timer or counter. Its clock source may be selected from internal crystal oscillator or externally on pin TMRCK. The timer can be set to be a single-shot for a one-time event or re-triggerable for a periodic event. An interrupt may be generated in the INT Register when the timer times out. It is controlled through 4 configuration registers [TIMERCNTL, TIMER, TIMELSB, TIMERMSB]. These registers provide start/stop and re-triggerable or one-shot operation. The time-out output of the Timer can be set to generate an interrupt for system or event alarm.

**FIGURE 15. TIMER/COUNTER CIRCUIT.**

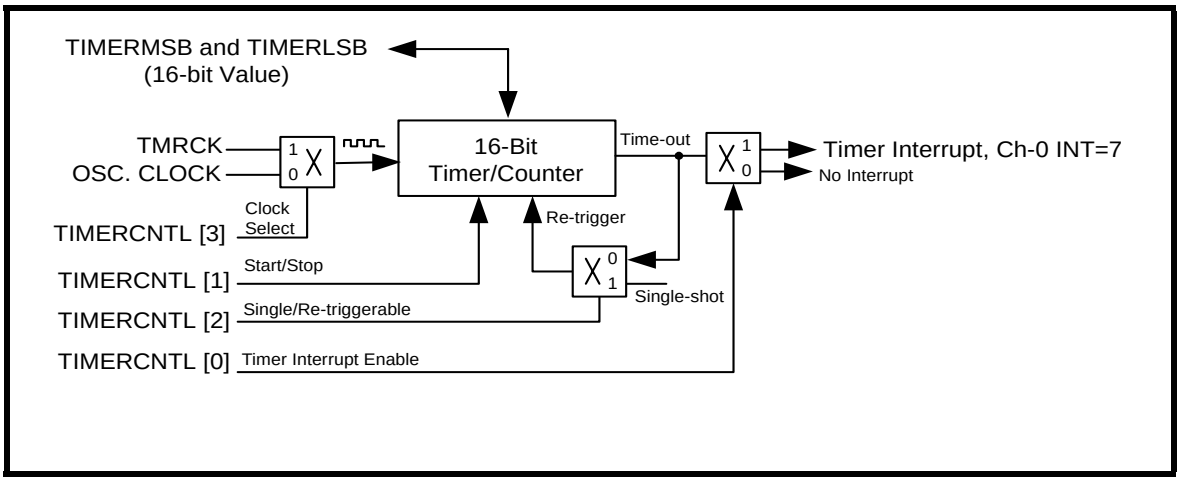



**TABLE 10: TIMER CONTROL REGISTER**

| | |
|---|---|
| TIMERCNTL [0] | Logic 0 (default) disables Timer-Counter interrupt and logic one enables the interrupt, reading the TIMERCNTL clears the interrupt. |
| TIMERCNLT [1] | Logic 0 (default) stops/pauses the timer and logic one starts/re-starts the timer/counter. |
| TIMERCNTL [2] | Logic0 (default) selects re-trigger timer function and logic one selects one-shot (timer function. |
| TIMERCNTL [3] | Logic 0 (default) selects internal and logic one selects external clock to the timer/counter. |
| TIMERCNTL [7:4] | Reserved (defaults to zero). |

**TIMERCNTL Register**

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|---|---|---|---|---|---|---|---|
| Rsvd | Rsvd | Rsvd | Rsvd | Clock Select | Single/ Re-trigger | Start/ Stop | INT Enable |

**TIMER [7:0] (default 0x00):** Reserved.

**TIMERMSB [7:0] and TIMERLSB [7:0]**

TIMERMSB and TIMERLSB form a 16-bit value. The least-significant bit of the timer is being bit [0] of the TIMERLSB with most-significant-bit being bit [7] in TIMERMSB. Reading the TIMERCNTL register will clear its interrupt. Default value is zero upon powerup and reset.

16-Bit Timer/Counter Programmable Registers

**TIMERMSB Register**

| Bit-15 | Bit-14 | Bit-13 | Bit-12 | Bit-11 | Bit-10 | Bit-9 | Bit-8 |
|---|---|---|---|---|---|---|---|

**TIMERLSB Register**

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|---|---|---|---|---|---|---|---|

### 3.1.3 8XMODE [7:0] (default 0x00)

Each bit selects 8X or 16X sampling rate for that UART channel, bit-0 is channel 0. Logic 0 (default) selects normal 16X sampling with logic one selects 8X sampling rate. Transmit and receive data rates will double by selecting 8X.

**8XMODE Register**

Individual UART Channel 8X Clock Mode Enable

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|---|---|---|---|---|---|---|---|
| Rsvd | Rsvd | Rsvd | Rsvd | Ch-3 | Ch-2 | Ch-1 | Ch-0 |

### 3.1.4 REGA [7:0] reserved (default 0x00)

### 3.1.5 RESET [7:0] (default 0x00)

**RESET Register**

Individual UART Channel Reset Enable

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|---|---|---|---|---|---|---|---|
| Rsvd | Rsvd | Rsvd | Rsvd | Ch-3 | Ch-2 | Ch-1 | Ch-0 |

The 8-bit Reset register [RESET] provides the software with the ability to reset individual UART(s) when there is a need. Each bit is self-resetting after it is written a logic 1 to perform a reset to that channel. All registers in that channel will be reset to the default condition, see **Table 19** for details. As an example, bit-0 =1 resets UART channel 0 with bit-3=1 resets channel 3.

### 3.1.6 SLEEP [7:0] - (default 0x00)

The 8-bit Sleep register enables each UART separately to enter Sleep mode. Sleep mode reduces power consumption when the system needs to put the UART(s) to idle. The UART enters sleep mode when there is no interrupt pending. When all 4 UARTs are put to sleep, the on-chip oscillator shuts off to further conserve power. In this case, the quad UART is awakened by any of the UART channel on from a receive data byte or a change on the modem port (CTS#, DSR#, CD# and RI#). The UART is ready after 32 crystal clocks to ensure full functionality. Also, a special interrupt is generated with an indication of no pending interrupt. Reading INT0 will clear this wake-up interrupt. Logic 0 (default) and logic 1 disable and enable sleep mode respectively.

**SLEEP Register**
Individual UART Channel Sleep Enable

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|---|---|---|---|---|---|---|---|
| Rsvd | Rsvd | Rsvd | Rsvd | Ch-3 | Ch-2 | Ch-1 | Ch-0 |

### 3.1.7 Device Identification and Revision

There are 2 internal registers that provide device identification and revision, DVID and DREV registers. The 8-bit content in the DVID register provides device identification. A return value of 0x24 from this register indicates the device is a XR16L784. The DREV register returns a 8-bit value of 0x01 for revision A, 0x02 for revision B and so on. This information is very useful to the software driver for identifying which device it is communicating with and to keep up with revision changes.

**DVID [7:0] (default 0x24)**

Device identification for the type of UART. The upper nibble indicates it is a XR16L78x series with lower nibble indicating the number of channels.

Examples:

XR16L784 = 0x24

XR16L788 = 0x28

**DREV [7:0]**

Revision number of the XR16L784. A 0x01 represents "revision-A" with 0x02 for rev-B and so forth.

### 3.1.8 REGB [7:0] - (default 0x00)

REGB register provides a control for simultaneous write to all 4 UARTs configuration registers or individually. This is very useful for device intialization in the power up and reset routines.

| | |
|---|---|
| REGB[0] | Logic 0 (default) write to each UART configuration registers individually. |
| | Logic 1 enables simultaneous write to all 4 UARTs configuration register. Useful during device initialization. |
| REGB[7:1] | Reserved |

### 3.2 UART CHANNEL CONFIGURATION REGISTERS

The first 8 registers are 16550 compatible with EXAR enhanced feature registers located on the upper 8 addresses. The 4 sets of UART configuration registers are decoded using address lines A0 to A3 as shown below.

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**TABLE 11: UART CHANNEL CONFIGURATION REGISTERS**

| ADDRESS | | | | REGISTER | READ/WRITE | COMMENTS |
|---|---|---|---|---|---|---|
| A3 | A2 | A1 | A0 | | | |
| **16550 COMPATIBLE REGISTERS** | | | | | | |
| 0 | 0 | 0 | 0 | RHR - Receive Holding Register | Read-only | LCR[7] = 0 |
| 0 | 0 | 0 | 0 | THR - Transmit Holding Register | Write-only | LCR[7] = 0 |
| 0 | 0 | 0 | 0 | DLL - Div Latch Low | Read/Write | LCR[7] = 1 |
| 0 | 0 | 0 | 1 | DLM - Div Latch High | Read/Write | LCR[7] = 1 |
| 0 | 0 | 0 | 1 | IER - Interrupt Enable Register | Read/Write | LCR[7] = 0 |
| 0 | 0 | 1 | 0 | ISR - Interrupt Status Register | Read-only | |
| 0 | 0 | 1 | 0 | FCR - FIFO Control Register | Write-only | |
| 0 | 0 | 1 | 1 | LCR - Line Control Register | Read/Write | |
| 0 | 1 | 0 | 0 | MCR - Modem Control Register | Read/Write | |
| 0 | 1 | 0 | 1 | LSR - Line Status Register | Read-only | |
| 0 | 1 | 1 | 0 | MSR - Modem Status Register | Read-only | |
| 0 | 1 | 1 | 0 | RS485 Turn-Around Delay Register | Write-only | |
| 0 | 1 | 1 | 1 | SPR - Scratch Pad Register | Read/Write | |
| **ENHANCED REGISTERS** | | | | | | |
| 1 | 0 | 0 | 0 | FCTR - Feature Control Register | Read/Write | |
| 1 | 0 | 0 | 1 | EFR - Enhanced Function Register | Read/Write | |
| 1 | 0 | 1 | 0 | TXCNT - Transmit FIFO Level Counter | Read-only | |
| 1 | 0 | 1 | 0 | TXTRG - Transmit FIFO Trigger Level | Write-only | |
| 1 | 0 | 1 | 1 | RXCNT - Receive FIFO Level Counter | Read-only | |
| 1 | 0 | 1 | 1 | RXTRG - Receive FIFO Trigger Level | Write-only | |
| 1 | 1 | 0 | 0 | Xoff-1 - Xoff Character 1 | Write-only | |
| 1 | 1 | 0 | 0 | Xchar | Read-only | Xon,Xoff Rcvd. Flags |
| 1 | 1 | 0 | 1 | Xoff-2 - Xoff Character 2 | Write-only | |
| 1 | 1 | 1 | 0 | Xon-1 - Xon Character 1 | Write-only | |
| 1 | 1 | 1 | 1 | Xon-2 - Xon Character 2 | Write-only | |

**TABLE 12: UART CHANNEL CONFIGURATION REGISTERS DESCRIPTION.** SHADED BITS ARE ENABLED BY EFR BIT-4.

| ADDRESS A3-A0 | REG NAME | READ/ WRITE | BIT-7 | BIT-6 | BIT-5 | BIT-4 | BIT-3 | BIT-2 | BIT-1 | BIT-0 | COMMENT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 0 0 0 | RHR | R | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR[7]=0 |
| 0 0 0 0 | THR | W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR[7]=0 |
| 0 0 0 0 | DLL | R/W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR[7]=1 |
| 0 0 0 1 | DLM | R/W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR[7]=1 |
| 0 0 0 1 | IER | R/W | 0<br>CTS/ DSR# Int. Enable | 0<br>RTS/ DTR# Int. Enable | 0<br>Xon/Xoff/ Sp. Char. Int. Enable | 0 | Modem Status Int. Enable | RX Line Status Int. Enable | TX Empty Int. Enable | RX Data Int. Enable | |
| 0 0 1 0 | ISR | R | FIFOs Enable | FIFOs Enable | 0<br>Delta-Flow Cntl | 0<br>Xoff/special char | INT Source Bit-3 | INT Source Bit-2 | INT Source Bit-1 | INT Source Bit-0 | |
| 0 0 1 0 | FCR | W | RX FIFO Trigger | RX FIFO Trigger | TX FIFO Trigger | TX FIFO Trigger | DMA Mode | TX FIFO Reset | RX FIFO Reset | FIFOs Enable | |
| 0 0 1 1 | LCR | R/W | Divisor Enable | Set TX Break | Set Parity | Even Parity | Parity Enable | Stop Bits | Word Length Bit-1 | Word Length Bit-0 | |
| 0 1 0 0 | MCR | R/W | 0<br>BRG Prescaler | 0<br>IR Enable | 0<br>XonAny | Internal Lopback Enable | OP2[2] | OP1[2]<br>RTS/ DTR Flow Sel | RTS# Pin Control | DTR# Pin Control | |
| 0 1 0 1 | LSR | R/W | RX FIFO ERROR | TSR Empty | THR Empty | RX Break | RX Framing Error | RX Parity Error | RX Overrun | RX Data Ready | |
| 0 1 1 0 | MSR | R | CD | RI | DSR | CTS | Delta CD# | Delta RI# | Delta DSR# | Delta CTS# | |
| | MSR | W | RS485 DLY-3 | RS485 DLY-2 | RS485 DLY-1 | RS485 DLY-0 | 0 | 0 | 0 | 0 | |
| 0 1 1 1 | SPR | R/W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | User Data |
| 1 0 0 0 | FCTR | R/W | TRG Table Bit-1 | TRG Table Bit-0 | Auto RS485 Enable | Invert IR RX Input | RTS/ DTR Hyst Bit-3 | RTS/ DTR Hyst Bit-2 | RTS/ DTR Hyst Bit-1 | RTS/ DTR Hyst Bit-0 | |
| 1 0 0 1 | EFR | R/W | Auto CTS/ DSR Enable | Auto RTS/ DTR Enable | Special Char Select | Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5] MSR[7:4] | Software Flow Cntl Bit-3 | Software Flow Cntl Bit-2 | Software Flow Cntl Bit-1 | Software Flow Cntl Bit-0 | |
| 1 0 1 0 | TXCNT | R | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 0 1 0 | TXTRG | W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |

**TABLE 12: UART CHANNEL CONFIGURATION REGISTERS DESCRIPTION.** SHADED BITS ARE ENABLED BY EFR BIT-4.

| ADDRESS A3-A0 | REG NAME | READ/ WRITE | BIT-7 | BIT-6 | BIT-5 | BIT-4 | BIT-3 | BIT-2 | BIT-1 | BIT-0 | COMMENT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 0 1 1 | RXCNT | R | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 0 1 1 | RXTRG | W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 1 0 0 | XCHAR | R | 0 | 0 | 0 | 0 | 0 | 0 | Xon Det. Indicator | Xoff Det. Indicator | Self-clear after read |
| 1 1 0 0 | XOFF1 | W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 1 0 1 | XOFF2 | W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 1 1 0 | XON1 | W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 1 1 1 | XON2 | W | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |

***NOTE:*** *MCR bits 2 and 3 (OP1 and OP2 outputs) are not available in the XR16L784. They are present for 16C550 compatibility during Internal loopback, see* **Figure 12**.

## 4.0 INTERNAL REGISTER DESCRIPTIONS

### *4.1 Receive Holding Register (RHR) - Read Only*

**SEE"RECEIVER" ON PAGE 10.**

### *4.2 Transmit Holding Register (THR) - Write Only*

**SEE"TRANSMITTER" ON PAGE 9.**

### *4.3 Interrupt Enable Register (IER) - Read/Write*

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR) register and also encoded in INT (INT0-INT3) register in the Device Configuration Registers.

#### 4.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = a logic 1) and receive interrupts (IER BIT-0 = logic 1) are enabled, the RHR interrupts (see ISR bits 3 and 4) status will reflect the following:

**A.** The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

**B.** FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

**C.** The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

#### 4.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the XR16L788 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

**A.** LSR BIT-0 indicates there is data in RHR or RX FIFO.

**B.** LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

**C.** LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

**D.** LSR BIT-5 indicates THR is empty.

**E.** LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

**F.** LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

**IER[0]: RHR Interrupt Enable**

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

**IER[1]: THR Interrupt Enable**

This interrupt is associated with bit-5 in the LSR register. An interrupt is issued whenever the THR becomes empty or when data in the TX FIFO falls below the programmed trigger level.

- Logic 0 = Disable Transmit Holding Register empty interrupt (default).
- Logic 1 = Enable Transmit Holding Register empty interrupt.

**IER[2]: Receive Line Status Interrupt Enable**

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bits 1-4 generate an interrupt immediately when the character has been received.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

**IER[3]: Modem Status Interrupt Enable**

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

**IER[4]: Reserved**.

**IER[5]: Xoff Interrupt Enable (requires EFR bit-4=1)**

- Logic 0 = Disable the software flow control, receive Xoff interrupt (default).
- Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

**IER[6]: RTS# Output Interrupt Enable (requires EFR bit-4=1)**

- Logic 0 = Disable the RTS# interrupt (default).
- Logic 1 = Enable the RTS# interrupt. The UART issues an interrupt when the RTS# pin makes a transition.

**IER[7]: CTS# Input Interrupt Enable (requires EFR bit-4=1)**

- Logic 0 = Disable the CTS# interrupt (default).
- Logic 1 = Enable the CTS# interrupt. The UART issues an interrupt when CTS# pin makes a transition.

### *4.4 Interrupt Status Register (ISR) - Read Only*

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others queue up for next service. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, **Table 13**, shows the data values (bit 0-5) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

### 4.4.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty (or transmitter empty in auto RS-485 control).
- MSR is by any of the MSR bits 0, 1, 2 and 3.
- Receive Xon/Xoff/Special character is by detection of a Xon, Xoff or Special character.
- CTS#/DSR# is when its transmitter toggles the input pin (from LOW to HIGH) during auto CTS/DSR flow control enabled by EFR bit-7 and selection on MCR bit-2.
- RTS#/DTR# is when its receiver toggles the output pin (from LOW to HIGH) during auto RTS/DTR flow control enabled by EFR bit-6 and selection on MCR bit-2.

### 4.4.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.
- Xon or Xoff interrupt is cleared by a read to ISR register.
- Special character interrupt is cleared by a read to ISR or after the next character is received.
- RTS#/DTR# and CTS#/DSR# status change interrupts are cleared by a read to the MSR register.

**TABLE 13: INTERRUPT SOURCE AND PRIORITY LEVEL**

| PRIORITY LEVEL | ISR REGISTER STATUS BITS | | | | | | SOURCE OF THE INTERRUPT+ |
|---|---|---|---|---|---|---|---|
| | BIT-5 | BIT-4 | BIT-3 | BIT-2 | BIT-1 | BIT-0 | |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | LSR (Receiver Line Status Register) |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 | RXRDY (Received Data Ready) |
| 3 | 0 | 0 | 1 | 1 | 0 | 0 | RXRDY (Receive Data Time-out) |
| 4 | 0 | 0 | 0 | 0 | 1 | 0 | TXRDY (Transmitter Holding Register Empty) |
| 5 | 0 | 0 | 0 | 0 | 0 | 0 | MSR (Modem Status Register) |
| 6 | 0 | 1 | 0 | 0 | 0 | 0 | RXRDY (Received Xon/Xoff or Special character) |
| 7 | 1 | 0 | 0 | 0 | 0 | 0 | CTS#/DSR#, RTS#/DTR# change of state |
| X | 0 | 0 | 0 | 0 | 0 | 1 | None (default) |

**ISR[0]: Interrupt Status**

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending. (default condition)

**ISR[5:1]: Interrupt Status**

These bits indicate the source for a pending interrupt at interrupt priority levels (See **Table 13**). See **"Section 4.4.1, Interrupt Generation:" on page 29** and **"Section 4.4.2, Interrupt Clearing:" on page 29** for details.

**ISR[7:6]: FIFO Enable Status**

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

### *4.5 FIFO Control Register (FCR) - Write Only*

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

**FCR[0]: TX and RX FIFO Enable**

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

**FCR[1]: RX FIFO Reset**

This bit is only active when FCR bit-0 is active.

- Logic 0 = No receive FIFO reset (default).
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

**FCR[2]: TX FIFO Reset**

This bit is only active when FCR bit-0 is active.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

**FCR[3]: DMA Mode Select**

This bit has no effect since TXRDY and RXRDY pins are not available in this device. It is provided for legacy software.

- Logic 0 = Set DMA to mode 0 (default).
- Logic 1 = Set DMA to mode 1.

**FCR[5:4]: Transmit FIFO Trigger Select**

(logic 0 = default, TX trigger level = one)

The FCTR Bits 6-7 are associated with these 2 bits by selecting one of the four tables. The 4 user selectable trigger levels in 4 tables are supported for compatibility reasons. These 2 bits set the trigger level for the transmit FIFO interrupt. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. **Table 14** below shows the selections.

**FCR[7:6]: Receive FIFO Trigger Select**

(logic 0 = default, RX trigger level =1)

The FCTR Bits 5-4 are associated with these 2 bits. These 2 bits are used to set the trigger level for the receive FIFO. The UART will issue a receive interrupt when the number of the characters in the FIFO crosses the trigger level. **Table 14** shows the complete selections. Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side.

**TABLE 14: TRANSMIT AND RECEIVE FIFO TRIGGER TABLE AND LEVEL SELECTION**

| TRIGGER TABLE | FCTR BIT-7 | FCTR BIT-6 | FCR BIT-7 | FCR BIT-6 | FCR BIT-5 | FCR BIT-4 | RECEIVE TRIGGER LEVEL | TRANSMIT TRIGGER LEVEL | COMPATIBILITY |
|---|---|---|---|---|---|---|---|---|---|
| **Table-A** | 0 | 0 | | | 0 | 0 | | 1 (default) | 16C550, 16C2550, 16C2552, 16C554, 16C580 |
| | | | 0 | 0 | | | 1 (default) | | |
| | | | 0 | 1 | | | 4 | | |
| | | | 1 | 0 | | | 8 | | |
| | | | 1 | 1 | | | 14 | | |
| **Table-B** | 0 | 1 | | | 0 | 0 | | 16 | 16C650A |
| | | | | | 0 | 1 | | 8 | |
| | | | | | 1 | 0 | | 24 | |
| | | | | | 1 | 1 | | 30 | |
| | | | 0 | 0 | | | 8 | | |
| | | | 0 | 1 | | | 16 | | |
| | | | 1 | 0 | | | 24 | | |
| | | | 1 | 1 | | | 28 | | |
| **Table-C** | 1 | 0 | | | 0 | 0 | | 8 | 16C654 |
| | | | | | 0 | 1 | | 16 | |
| | | | | | 1 | 0 | | 32 | |
| | | | | | 1 | 1 | | 56 | |
| | | | 0 | 0 | | | 8 | | |
| | | | 0 | 1 | | | 16 | | |
| | | | 1 | 0 | | | 56 | | |
| | | | 1 | 1 | | | 60 | | |
| **Table-D** | 1 | 1 | X | X | X | X | Programmable via RXTRG register. | Programmable via TXTRG register. | 16L2752, 16L2750, 16C2852, 16C850, 16C854, 16C864 |

### *4.6 Line Control Register (LCR) - Read/Write*

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

**LCR[1:0]: TX and RX Word Length Select**

These two bits specify the word length to be transmitted or received.

| BIT-1 | BIT-0 | WORD LENGTH |
|---|---|---|
| 0 | 0 | 5 (default) |
| 0 | 1 | 6 |
| 1 | 0 | 7 |
| 1 | 1 | 8 |

### LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

| BIT-2 | WORD LENGTH | STOP BIT LENGTH (BIT TIME(S)) |
|---|---|---|
| 0 | 5,6,7,8 | 1 (default) |
| 1 | 5 | 1-1/2 |
| 1 | 6,7,8 | 2 |

### LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See **Table 15** for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

### LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even the number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

### LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR BIT-5 = logic 0, parity is not forced (default).
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

**TABLE 15: PARITY SELECTION**

| LCR BIT-5 | LCR BIT-4 | LCR BIT-3 | PARITY SELECTION |
|---|---|---|---|
| X | X | 0 | No parity |
| 0 | 0 | 1 | Odd parity |
| 0 | 1 | 1 | Even parity |
| 1 | 0 | 1 | Force parity to mark, "1" |
| 1 | 1 | 1 | Forced parity to space, "0" |

### LCR[6]: Transmit Break Enable

When enabled the Break control bit causes a break condition to be transmitted (the TX output is forced to a "space', logic 0, state). This condition remains until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition. (default)
- Logic 1 = Forces the transmitter output (TX) to a "space", logic 0, for alerting the remote receiver of a line break condition.

**LCR[7]: Baud Rate Divisors Enable**

Baud rate generator divisor (DLL/DLM) enable.

- Logic 0 = Data registers are selected (default).
- Logic 1 = Divisor latch registers are selected.

### *4.7 Modem Control Register (MCR) - Read/Write*

The MCR register is used for controlling the modem interface signals or general purpose inputs/outputs.

**MCR[0]: DTR# Output**

The DTR# pin may be used for automatic hardware flow control enabled by EFR bit-6 and MCR bit-2=1. If the modem interface is not used, this output may be used for general purpose.

- Logic 0 = Force DTR# output to a logic 1 (default).
- Logic 1 = Force DTR# output to a logic 0.

**MCR[1]: RTS# Output**

The RTS# pin may be used for automatic hardware flow control by enabled by EFR bit-6 and MCR bit-2=0. If the modem interface is not used, this output may be used for general purpose.

- Logic 0 = Force RTS# output to a logic 1 (default).
- Logic 1 = Force RTS# output to a logic 0.

**MCR[2]: RTS/CTS or DTR/DSR for Auto Flow Control**

DTR# or RTS# auto hardware flow control select. This bit is in effect only when auto RTS/DTR is enabled by EFR bit-6.

- Logic 0 = RTS# (RX side) and CTS# (TX side) pins are used for auto hardware flow control (default).
- Logic 1 = DTR# (RX side) and DSR# (TX side) pins are used for auto hardware flow control.

**MCR[3]: Reserved**

**MCR[4]: Internal Loopback Enable**

- Logic 0 = Disable loopback mode (default).
- Logic 1 = Enable local loopback mode, see loopback section and **Figure 12**.

**MCR[5]: Xon-Any Enable**

- Logic 0 = Disable Xon-Any function (default).
- Logic 1 = Enable Xon-Any function. In this mode any RX character received will enable Xon, resume data transmission.

**MCR[6]: Infrared Encoder/Decoder Enable**

The state of this bit depends on the sampled logic level of pin ENIR during power up, following a hardware reset (rising edge of RST# input). Afterward user can override this bit for desired operation.

- Logic 0 = Enable the standard modem receive and transmit character interface.
- Logic 1 = Enable infrared IrDA receive and transmit inputs/outputs. While in this mode, the TX/RX output/input are routed to the infrared encoder/decoder. The data input and output levels will conform to the IrDA infrared interface requirement. As such, while in this mode the infrared TX output will be a logic 0 during idle data conditions. FCTR bit-4 may be selected to invert the RX input signal level going to the decoder for infrared modules that provide rather an inverted output.

**MCR[7]: Clock Prescaler Select**

- Logic 0 = Divide by one. The input clock from the crystal or external clock is fed directly to the Programmable Baud Rate Generator without further modification, i.e., divide by one (default).
- Logic 1 = Divide by four. The prescaler divides the input clock from the crystal or external clock by four and feeds it to the Programmable Baud Rate Generator, hence, data rates become one forth.

### 4.8 Line Status Register (LSR) - Read Only

This register provides the status of data transfers between the UART and the host. If IER bit-2 is set to a logic 1, an LSR interrupt will be generated immediately when any character in the RX FIFO has an error (parity, framing, overrun, break).

**LSR[0]: Receive Data Ready Indicator**

- Logic 0 = No data in receive holding register or FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

**LSR[1]: Receiver Overrun Flag**

- Logic 0 = No overrun error (default).
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

**LSR[2]: Receive Data Parity Error Flag**

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The receive character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR.

**LSR[3]: Receive Data Framing Error Flag**

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR.

**LSR[4]: Receive Break Flag**

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO. The break indication remains until the RX input returns to the idle condition, “mark” or logic 1.

**LSR[5]: Transmit Holding Register Empty Flag**

This bit is the Transmit Holding Register Empty indicator. This bit indicates that the transmitter is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the host when the THR interrupt enable is set. The THR bit is set to a logic 1 when the last data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host. In the FIFO mode this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.

**LSR[6]: Transmit Shift Register Empty Flag**

This bit is the Transmit Shift Register Empty indicator. This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmit FIFO and transmit shift register are both empty.

**LSR[7]: Receive FIFO Data Error Flag**

- Logic 0 = No FIFO error (default).
- Logic 1 = An indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there is no more error(s) in the FIFO.

### 4.9 Modem Status Register (MSR) - Read Only

This register provides the current state of the modem interface signals, or other peripheral device that the UART is connected. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used as general purpose inputs/outputs when they are not used with modem signals.

**MSR[0]: Delta CTS# Input Flag**

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3.

**MSR[1]: Delta DSR# Input Flag**

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3.

**MSR[2]: Delta RI# Input Flag**

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from a logic 0 to a logic 1, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3.

**MSR[3]: Delta CD# Input Flag**

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3.

**MSR[4]: CTS Input Status**

CTS# pin may function as automatic hardware flow control signal input if it is enabled and selected by Auto CTS (EFR bit-7) and RTS/CTS flow control select (MCR bit-2). Auto CTS flow control allows starting and stopping of local data transmissions based on the modem CTS# signal. A HIGH on the CTS# pin will stop UART transmitter as soon as the current character has finished transmission, and a LOW will resume data transmission. Normally MSR bit-4 bit is the complement of the CTS# input. However in the loopback mode, this bit is equivalent to the RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

**MSR[5]: DSR Input Status**

This input may be used for auto DTR/DSR flow control function, see auto hardware flow control section. Normally this bit is the complement of the DSR# input. In the loopback mode, this bit is equivalent to the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

**MSR[6]: RI Input Status**

Normally this bit is the complement of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

**MSR[7]: CD Input Status**

Normally this bit is the complement of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input when the modem interface is not used.

### *4.10 Modem Status Register (MSR) - Write Only*

The upper four bits 4-7 of this register sets the delay in number of bits time for the auto RS485 turn around from transmit to receive.

**MSR [7:4]**

When Auto RS485 feature is enabled (FCTR bit-5=1) and RTS# output is connected to the enable input of a RS-485 transceiver. These 4 bits select from 0 to 15 bit-time delay after the end of the last stop-bit of the last transmitted character. This delay controls when to change the state of RTS# output. This delay is very useful in long-cable networks. **Table 16** shows the selection. The bits are enabled by EFR bit-4.

TABLE 16: AUTO RS485 HALF-DUPLEX DIRECTION CONTROL DELAY FROM TRANSMIT-TO-RECEIVE

| MSR[7] | MSR[6] | MSR[5] | MSR[4] | DELAY IN DATA BIT(S) TIME |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 9 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | 10 |
| 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 0 | 0 | 12 |
| 1 | 1 | 0 | 1 | 13 |
| 1 | 1 | 1 | 0 | 14 |
| 1 | 1 | 1 | 1 | 15 |

### *4.11 SCRATCH PAD REGISTER (SPR) - Read/Write*

This is a 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

### *4.12 FEATURE CONTROL REGISTER (FCTR) - Read/Write*

This register controls the UART enhanced functions that are not available on ST16C554 or ST16C654.

**FCTR [3:0] - Auto RTS/DTR Flow Control Hysteresis Select**

These bits select the auto RTS/DTR flow control hysteresis and only valid when TX and RX Trigger Table-D is selected (FCTR bit-6 and 7 are set to logic 1). The RTS/DTR hysteresis is referenced to the RX FIFO trigger level. After reset, these bits are set to logic 0 selecting the next FIFO trigger level for hardware flow control. **Table 17** below shows the 16 selectable hysteresis levels.

**TABLE 17: 16 SELECTABLE HYSTERESIS LEVELS WHEN TRIGGER TABLE-D IS SELECTED**

| FCTR BIT-3 | FCTR BIT-2 | FCTR BIT-1 | FCTR BIT-0 | RTS/DTR HYSTERESIS (CHARACTERS) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | +/- 4 |
| 0 | 0 | 1 | 0 | +/- 6 |
| 0 | 0 | 1 | 1 | +/- 8 |
| 0 | 1 | 0 | 0 | +/- 8 |
| 0 | 1 | 0 | 1 | +/- 16 |
| 0 | 1 | 1 | 0 | +/- 24 |
| 0 | 1 | 1 | 1 | +/- 32 |
| 1 | 1 | 0 | 0 | +/- 12 |
| 1 | 1 | 0 | 1 | +/- 20 |
| 1 | 1 | 1 | 0 | +/- 28 |
| 1 | 1 | 1 | 1 | +/- 36 |
| 1 | 0 | 0 | 0 | +/- 40 |
| 1 | 0 | 0 | 1 | +/- 44 |
| 1 | 0 | 1 | 0 | +/- 48 |
| 1 | 0 | 1 | 1 | +/- 52 |

**FCTR[4]: Infrared RX Input Logic Select**

- Logic 0 = Select RX input as active high encoded IrDA data, normal, (default).
- Logic 1 = Select RX input as active low encoded IrDA data, inverted.

**FCTR[5]: Auto RS485 Enable**

Auto RS485 half duplex control enable/disable.

- Logic 0 = Standard ST16C550 mode. Transmitter generates an interrupt when transmit holding register (THR) becomes empty. Transmit Shift Register (TSR) may still be shifting data bit out.
- Logic 1 = Enable Auto RS485 half duplex direction control. RTS# output changes its logic level from HIGH to LOW when finished sending the last stop bit of the last character out of the TSR register. It changes from LOW to HIGH when a data byte is loaded into the THR or transmit FIFO. The change to HIGH occurs prior sending the start-bit. It also changes the transmitter interrupt from transmit holding to transmit shift register (TSR) empty.

**FCTR[7:6]: TX and RX FIFO Trigger Table Select**

These 2 bits select the transmit and receive FIFO trigger level table A, B, C or D. When table A, B, or C is selected the auto RTS flow control trigger level is set to "next FIFO trigger level" for compatibility to ST16C550 and ST16C650 series. RTS/DTR# triggers on the next level of the RX FIFO trigger level, in another word, one FIFO level above and one FIFO level below. See in **Table 14** for complete selection with FCR bit 4-5 and FCTR bit 6-7, i.e. if Table C is used on the receiver with RX FIFO trigger level set to 56 bytes, RTS/DTR# output will de-assert at 60 and re-assert at 16.

### 4.13 Enhanced Feature Register (EFR) - Read/Write

Enhanced features are enabled or disabled using this register. Bit 0-3 provide single or dual consecutive character software flow control selection (see Table 18). When the Xon1 and Xon2 and Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential characters. Caution: note that whenever changing the TX or RX flow control bits, always reset all bits back to logic 0 (disable) before programming a new setting.

**TABLE 18: SOFTWARE FLOW CONTROL FUNCTIONS**

| EFR BIT-3 CONT-3 | EFR BIT-2 CONT-2 | EFR BIT-1 CONT-1 | EFR BIT-0 CONT-0 | TRANSMIT AND RECEIVE SOFTWARE FLOW CONTROL |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | No TX and RX flow control (default and reset) |
| 0 | 0 | X | X | No transmit flow control |
| 1 | 0 | X | X | Transmit Xon1/Xoff1 |
| 0 | 1 | X | X | Transmit Xon2/Xoff2 |
| 1 | 1 | X | X | Transmit Xon1 and Xon2/Xoff1 and Xoff2 |
| X | X | 0 | 0 | No receive flow control |
| X | X | 1 | 0 | Receiver compares Xon1/Xoff1 |
| X | X | 0 | 1 | Receiver compares Xon2/Xoff2 |
| 1 | 0 | 1 | 1 | Transmit Xon1/ Xoff1,<br>Receiver compares Xon1 or Xon2, Xoff1 or Xoff2 |
| 0 | 1 | 1 | 1 | Transmit Xon2/Xoff2,<br>Receiver compares Xon1 or Xon2, Xoff1 or Xoff2 |
| 1 | 1 | 1 | 1 | Transmit Xon1 and Xon2/Xoff1 and Xoff2,<br>Receiver compares Xon1 and Xon2/Xoff1 and Xoff2 |
| 0 | 0 | 1 | 1 | No transmit flow control,<br>Receiver compares Xon1 and Xon2/Xoff1 and Xoff2 |

**EFR[3:0]: Software Flow Control Select**

Combinations of software flow control can be selected by programming these bits.

**EFR[4]: Enhanced Function Bits Enable**

Enhanced function control bit. This bit enables the functions in IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 to be modified. After modifying any enhanced bits, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents legacy software from altering or overwriting the enhanced functions once set. Normally, it is recommended to leave it enabled, logic 1.

- Logic 0 = modification disable/latch enhanced features. IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are saved to retain the user settings. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are set to a logic 0 to be compatible with ST16C554 mode (default).
- Logic 1 = Enables the enhanced functions. When this bit is set to a logic 1 all enhanced features are enabled.

**EFR[5]: Special Character Detect Enable**

- Logic 0 = Special Character Detect Disabled (default).
- Logic 1 = Special Character Detect Enabled. The UART compares each incoming receive character with data in Xoff-2 register. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of the special character. Bit-0 corresponds with the LSB bit for the receive character. If flow control is set for comparing Xon1, Xoff1 (EFR [1:0]=10) then flow control and special character work normally. However, if flow control is set for comparing Xon2, Xoff2 (EFR[1:0]=01) then flow control works normally, but Xoff2 will not go to the FIFO, and will generate an Xoff interrupt and a special character interrupt.

**EFR[6]: Auto RTS or DTR Flow Control Enable**

RTS#/DTR# output may be used for hardware flow control by setting EFR bit-6 to logic 1. When Auto RTS/DTR is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and RTS/DTR# will de-assert (HIGH) at the next upper trigger or selected hysteresis level. RTS/DTR# will re-assert (LOW) when FIFO data falls below the next lower trigger or selected hysteresis level (see FCTR bits 4-7). The RTS# or DTR# output must be asserted (LOW) before the auto RTS/DTR can take effect. The selection for RTS# or DTR# is through MCR bit-2. RTS/DTR# pin will function as a general purpose output when hardware flow control is disabled.

- Logic 0 = Automatic RTS/DTR flow control is disabled (default).
- Logic 1 = Enable Automatic RTS/DTR flow control.

**EFR[7]: Auto CTS Flow Control Enable**

Automatic CTS or DSR Flow Control.

- Logic 0 = Automatic CTS/DSR flow control is disabled (default).
- Logic 1 = Enable Automatic CTS/DSR flow control. Transmission stops when CTS/DSR# pin de-asserts (HIGH). Transmission resumes when CTS/DSR# pin is asserted (LOW). The selection for CTS# or DSR# is through MCR bit-2.

### *4.14 TXCNT[7:0]: Transmit FIFO Level Counter - Read Only*

Transmit FIFO level byte count from 0x00 (zero) to 0x40 (64). This 8-bit register gives an indication of the number of characters in the transmit FIFO. The FIFO level Byte count register is read only. The user can take advantage of the FIFO level byte counter for faster data loading to the transmit FIFO., which reduces CPU bandwidth requirements.

### *4.15 TXTRG [7:0]: Transmit FIFO Trigger Level - Write Only*

An 8-bit value written to this register sets the TX FIFO trigger level from 0x00 (zero) to 0x40 (64). The TX FIFO trigger level generates an interrupt whenever the data level in the transmit FIFO falls below this preset trigger level.

### *4.16 RXCNT[7:0]: Receive FIFO Level Counter - Read Only*

Receive FIFO level byte count from 0x00 (zero) to 0x40 (64). It gives an indication of the number of characters in the receive FIFO. The FIFO level byte count register is read only. The user can take advantage of the FIFO level byte counter for faster data unloading from the receiver FIFO, which reduces CPU bandwidth requirements.

### *4.17 RXTRG[7:0]: Receive FIFO Trigger Level - Write Only*

An 8-bit value written to this register, sets the RX FIFO trigger level from 0x00 (zero) to 0x40 (64). The RX FIFO trigger level generates an interrupt whenever the receive FIFO level rises to this preset trigger level.

**TABLE 19: UART RESET CONDITIONS**

| REGISTERS | RESET STATE |
|---|---|
| DLL | Bits 7-0 = 0xXX |
| DLM | Bits 7-0 = 0xXX |
| RHR | Bits 7-0 = 0xXX |
| THR | Bits 7-0 = 0xXX |
| IER | Bits 7-0 = 0x00 |
| FCR | Bits 7-0 = 0x00 |
| ISR | Bits 7-0 = 0x01 |
| LCR | Bits 7-0 = 0x00 |
| MCR | Bits 7-0 = 0x00 |
| LSR | Bits 7-0 = 0x60 |
| MSR | Bits 3-0 = logic 0<br>Bits 7-4 = logic levels of the inputs |
| SPR | Bits 7-0 = 0xFF |
| FCTR | Bits 7-0 = 0x00 |
| EFR | Bits 7-0 = 0x00 |
| TXCNT | Bits 7-0 = 0x00 |
| TXTRG | Bits 7-0 = 0x00 |
| RXCNT | Bits 7-0 = 0x00 |
| RXTRG | Bits 7-0 = 0x00 |
| XCHAR | Bits 7-0 = 0x00 |
| XON1 | Bits 7-0 = 0x00 |
| XON2 | Bits 7-0 = 0x00 |
| XOFF1 | Bits 7-0 = 0x00 |
| XOFF2 | Bits 7-0 = 0x00 |
| | |
| **I/O SIGNALS** | **RESET STATE** |
| TX[ch-3:0] | HIGH |
| IRTX[ch-3:0] | LOW |
| RTS#[ch-3:0] | HIGH |
| DTR#[ch-3:0] | HIGH |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Range | 7 Volts |
| Voltage at Any Pin | -0.5 to 7V |
| Operating Temperature | -40$^{o}$ to +85$^{o}$ C |
| Storage Temperature | -65$^{o}$ to +150$^{o}$ C |
| Package Dissipation | 500 mW |
| Thermal Resistance (10x10x1.4mm 64-LQFP) | $\theta$-ja =70, $\theta$-jc =14 $^{o}$C/W |

## ELECTRICAL CHARACTERIISTICS

### *DC ELECTRICAL CHARACTERISTICS*

TA=0$^{o}$ to 70$^{o}$C (-40$^{o}$ to +85$^{o}$C for industrial grade package), Vcc-3.3V and 5V +/-10% unless specified

| SYMBOL | PARAMETER | 3.3V MIN | 3.3 MAX | 5V MIN | 5V MAX | UNITS | CONDITION |
|---|---|---|---|---|---|---|---|
| VILCK | Clock Input Low Voltage | -0.3 | 0.6 | -0.5 | 0.6 | V | |
| VIHCK | Clock Input High Voltage | 2.4 | VCC | 3.0 | VCC | V | |
| VIL | Input Low Voltage | -0.3 | 0.7 | -0.5 | 0.8 | V | |
| VIH | Input High Voltage | 2.0 | 6.0 | 2.0 | 6.0 | V | |
| VOLCK | Clock Output (XTAL2) Low Voltage | | 0.4 | | 0.4 | V | Iout=4 mA at 3.3V<br>Iout=6 mA at 5V |
| VOHCK | Clock Output (XTAL2) High Voltage | 2.0 | | 2.4 | | V | Iout=-1 mA at 3.3V<br>Iout=-2 at 5V |
| VOL | Output Low Voltage | See **Figure 16** | | | | | |
| VOH | Output High Voltage | See **Figure 17** | | | | | |
| IIL | Input Low Leakage Current | | -10 | | -10 | uA | |
| IIH | Input High Leakage Current | | 10 | | 10 | uA | |
| CIN | Input Pin Capacitance | | 5 | | 5 | pF | |
| ICC | Power Supply Current | | 5 | | 5 | mA | External clock at 2MHz. A7-A0 at GND, all inputs at VCC or GND and outputs unloaded |
| ISLEEP | Sleep Current | | 0.6 | | 1.5 | mA | Four UARTs asleep. A7-A0 at GND, all inputs at VCC or GND and outputs unloaded. |

FIGURE 16. XR16L784 VOL SINK CURRENT CHART

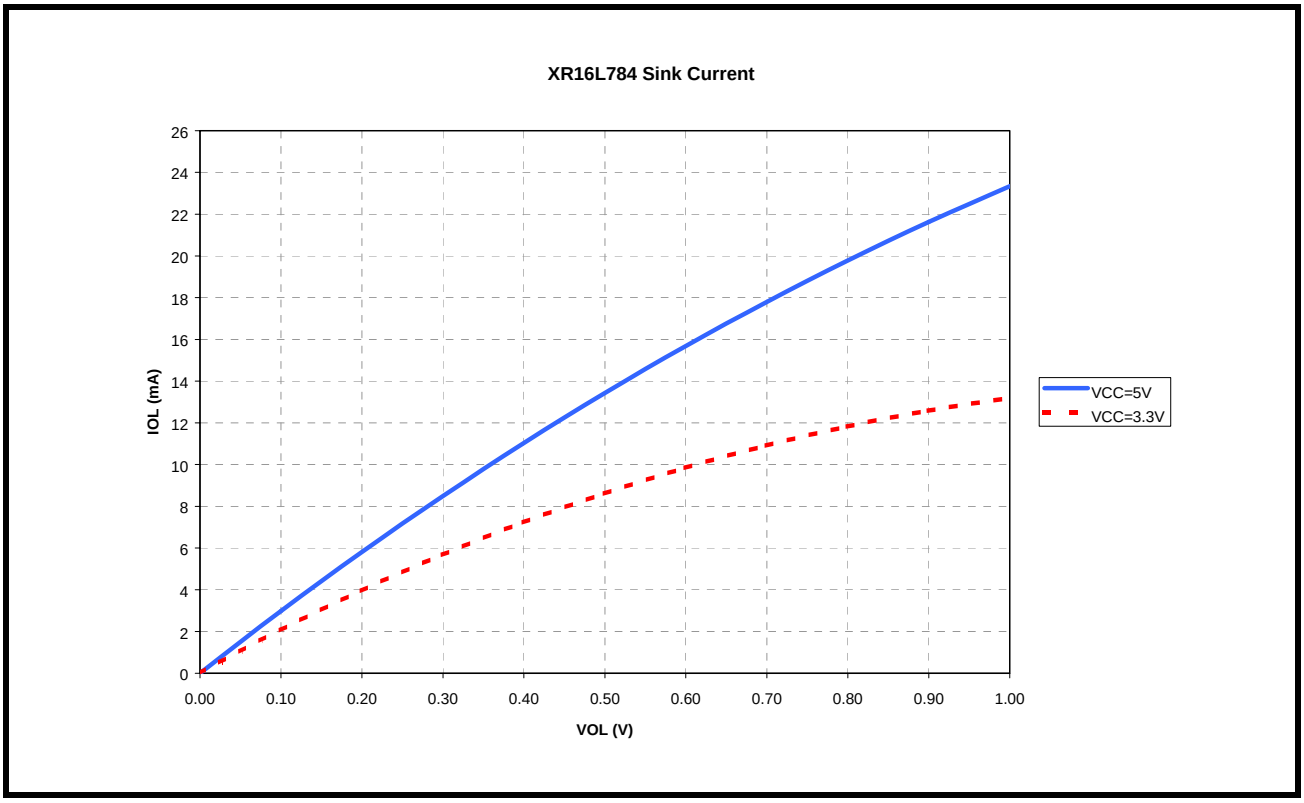
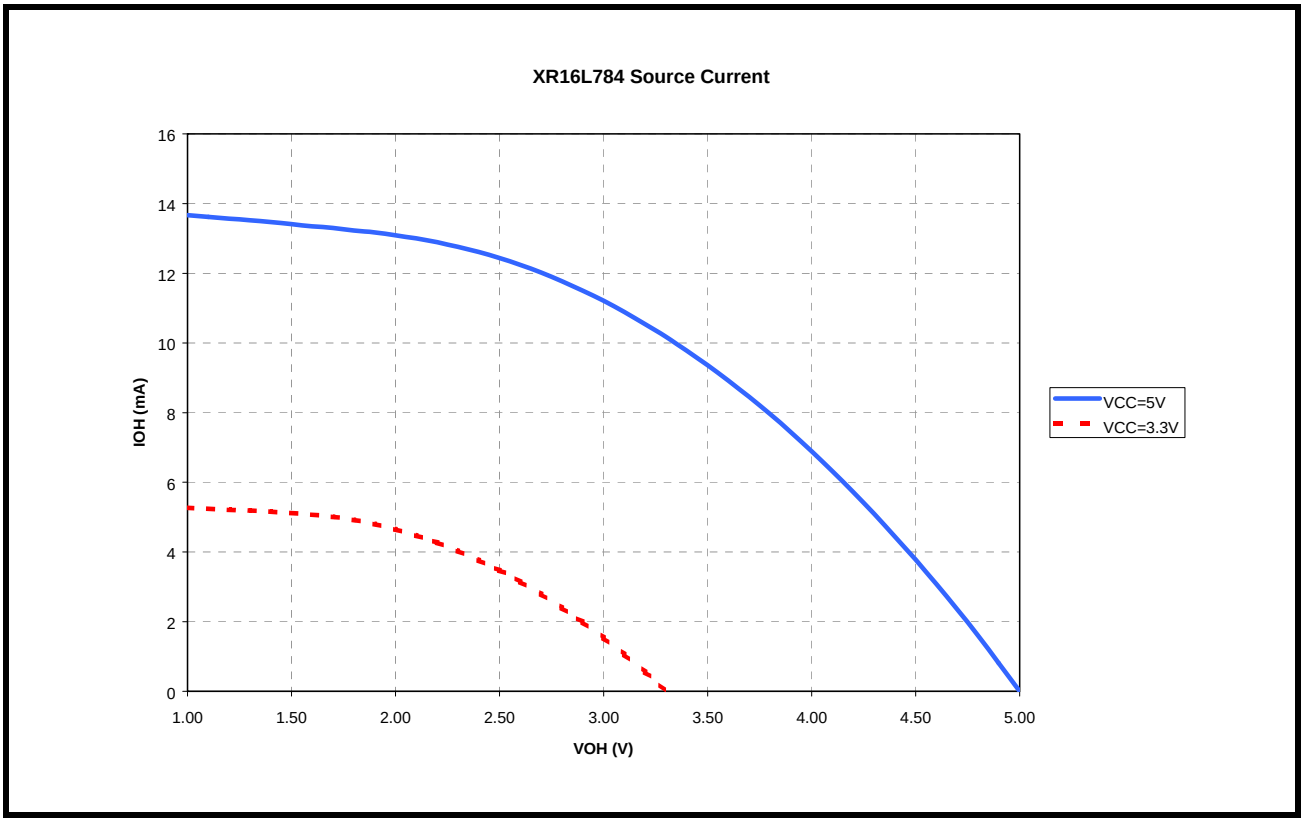



FIGURE 17. XR16L784 VOH SOURCE CURRENT CHART

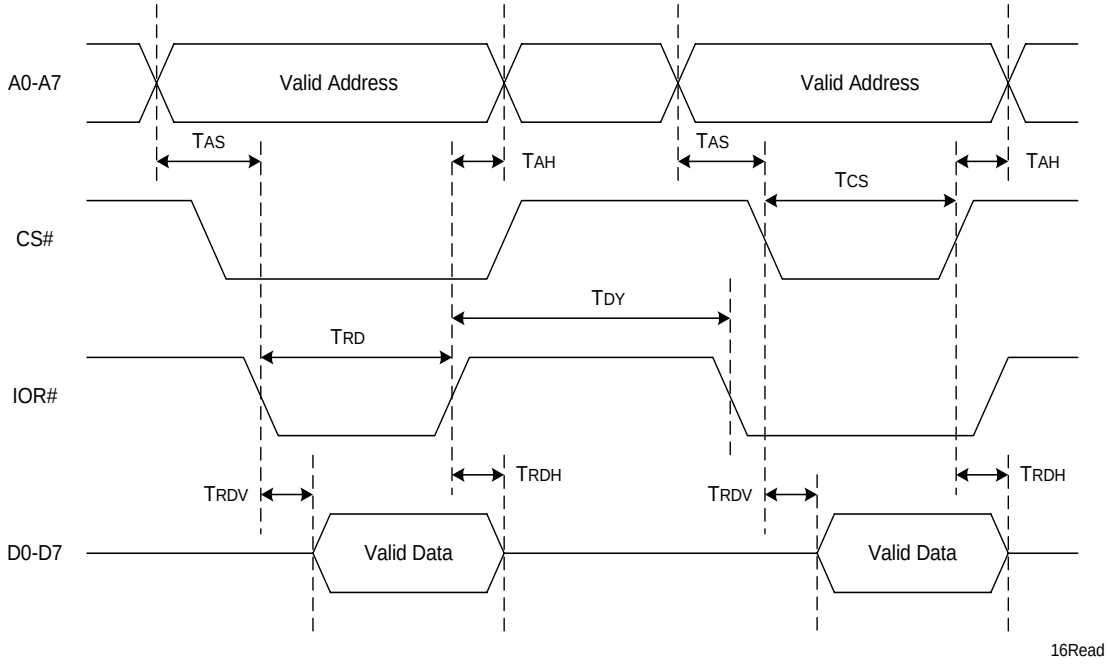


## AC ELECTRICAL CHARACTERISTICS

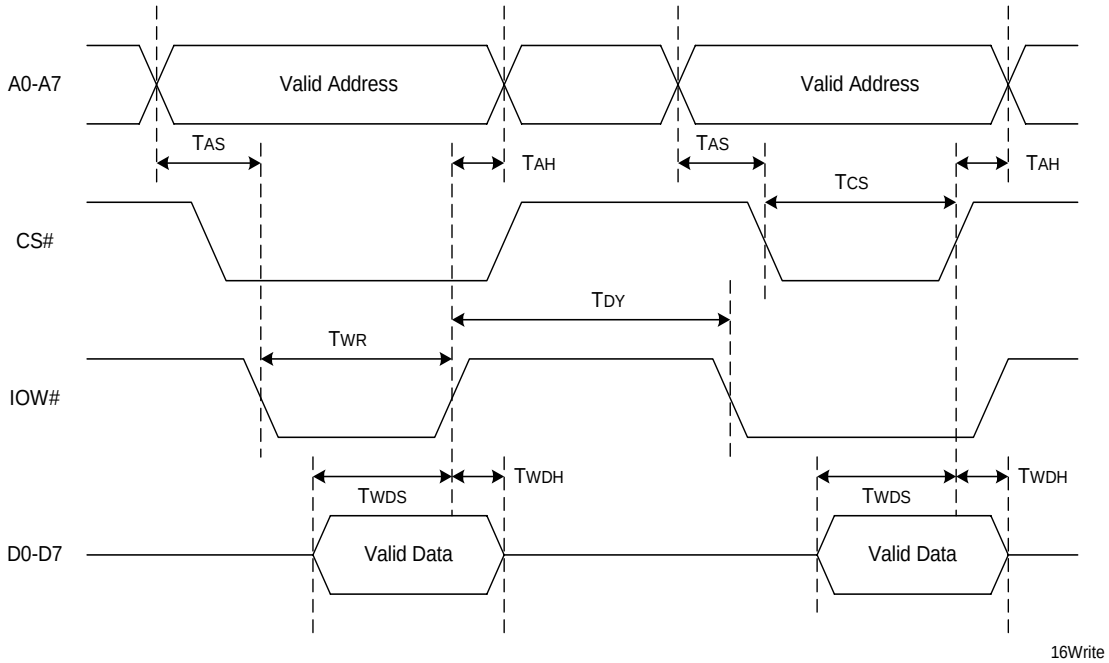
### TA=0$^{O}$ TO 70$^{O}$C (-40$^{O}$ TO +85$^{O}$C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.97V TO 5.5V, 70 PF LOAD WHERE APPLICABLE

| SYMBOL | PARAMETER | 3,3V MIN | 3.3V MAX | 5V MIN | 5V MAX | UNITS |
|---|---|---|---|---|---|---|
| TC1,TC2 | Clock Pulse Period | 10 | | 8 | | ns |
| TOSC | Oscillator Frequency | | 16 | | 24 | MHz |
| TECK | External Clock Frequency | | 33 | | 50 | MHz |
| TAS | Address Setup (16 Mode) | 5 | | 5 | | ns |
| TAH | Address Hold (16 Mode) | 10 | | 10 | | ns |
| TCS | Chip Select Width (16 Mode) | 50 | | 50 | | ns |
| TDY | Delay between CS# Active Cycles (16 Mode) | 50 | | 50 | | ns |
| TRD | Read Strobe Width (16 Mode) | 50 | | 50 | | ns |
| TWR | Write Strobe Width (16 Mode) | 40 | | 30 | | ns |
| TRDV | Read Data Valid (16 Mode) | 35 | | 25 | | ns |
| TWDS | Write Data Setup (16 Mode) | 15 | | 10 | | ns |
| TRDH | Read Data Hold (16 Mode) | | 15 | | 10 | ns |
| TWDH | Write Data Hold (16 Mode) | 15 | | 10 | | ns |
| TADS | Address Setup (68 Mode) | 10 | | 5 | | ns |
| TADH | Address Hold (68 Mode) | 10 | | 10 | | ns |
| TRWS | R/W# Setup to CS# (68 Mode) | 10 | | 10 | | ns |
| TRDA | Read Data Access (68 mode) | 35 | | 25 | | ns |
| TRDH | Read Data Hold (68 mode) | | 15 | | 10 | ns |
| TWDS | Write Data Setup (68 mode) | 10 | | 10 | | ns |
| TWDH | Write Data Hold (68 Mode) | 10 | | 10 | | ns |
| TRWH | CS# De-asserted to R/W# De-asserted (68 Mode) | 10 | | 10 | | ns |
| TCSL | CS# Width (68 Mode) | 50 | | 40 | | ns |
| TCSD | CS# Cycle Delay (68 Mode) | 50 | | 40 | | ns |
| TWDO | Delay from IOW# to Modem Output | | 50 | | 50 | ns |
| TMOD | Delay to set Interrupt from Modem Input | | 50 | | 35 | ns |
| TRSI | Delay To Reset Interrupt From IOR# | | 50 | | 35 | ns |
| TSSI | Delay From Stop To Set Interrupt | | 1 | | 1 | Bclk |
| TRRI | Delay From IOR# To Reset Interrupt | | 45 | | 40 | ns |
| TSI | Delay From Stop To Interrupt | | 45 | | 40 | ns |
| TWRI | Delay From IOW# To Reset Interrupt | | 45 | | 40 | ns |
| TRST | Reset Pulse | 40 | | 40 | | ns |
| Bclk | Baud Clock | 16X or 8X of data rate | | | | Hz |

**FIGURE 18. 16 MODE (INTEL) DATA BUS READ AND WRITE TIMING**

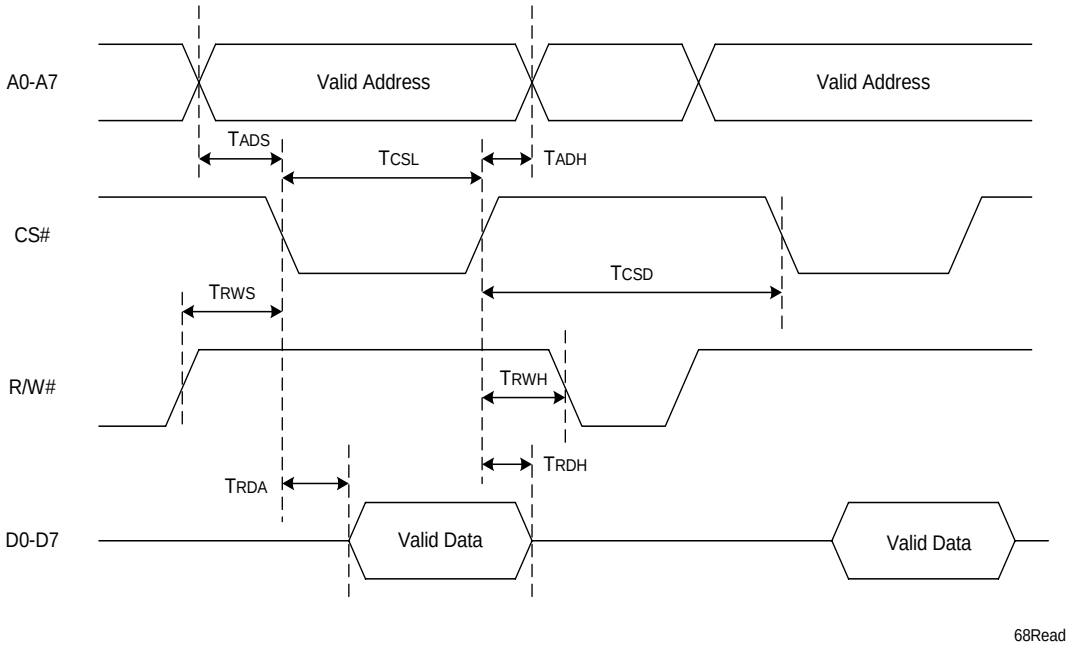



16 Mode (Intel) Data Bus Read Timing

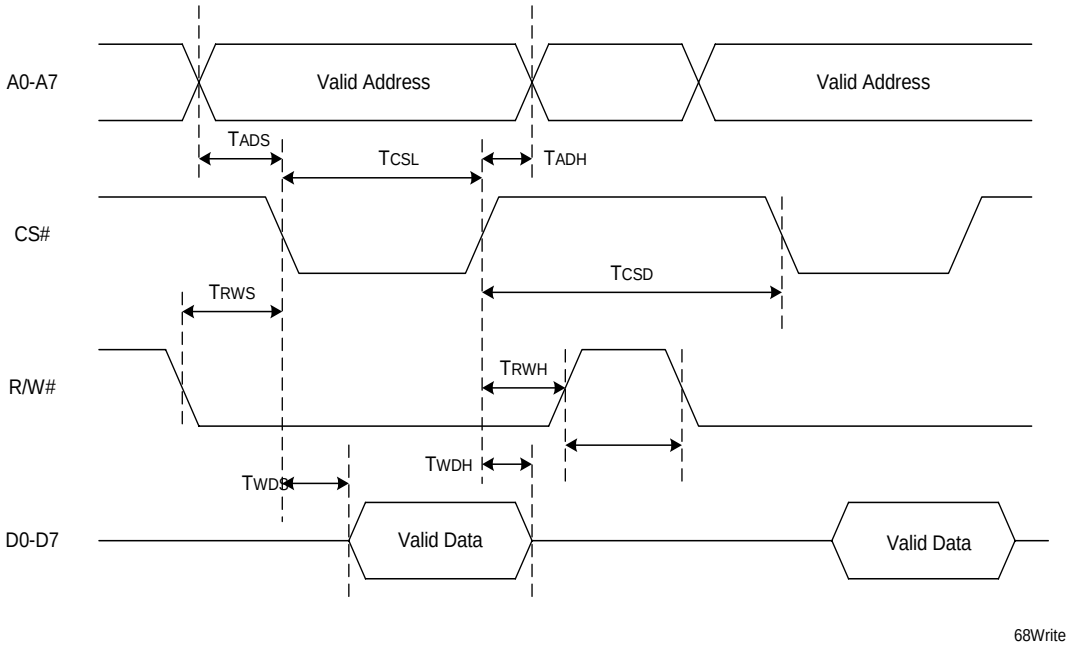



16 Mode (Intel) Data Bus Write Timing

**FIGURE 19. 68 MODE (MOTOROLA) DATA BUS READ AND WRITE TIMING**




68 Mode (Motorola) Data Bus Read Timing




68 Mode (Motorola) Data Bus Write Timing

**FIGURE 20. MODEM INPUT/OUTPUT PORT DELAY**

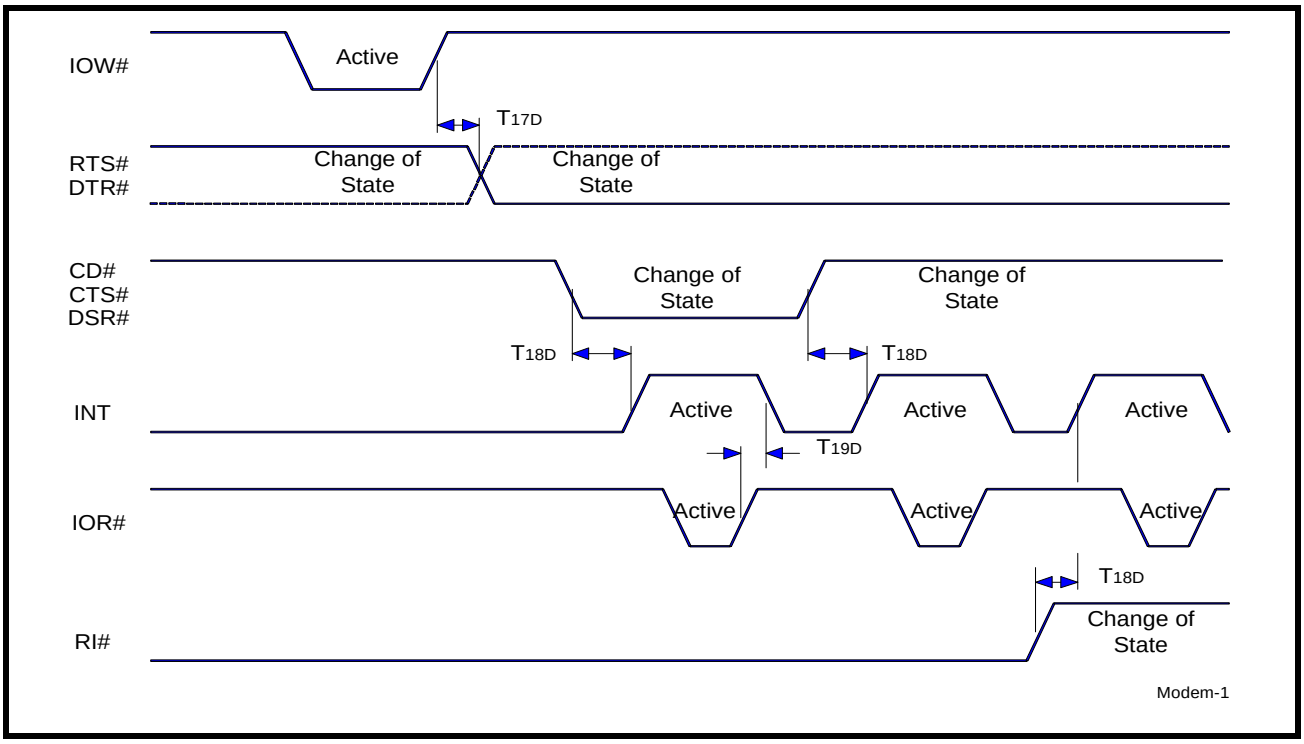



**FIGURE 21. RECEIVE INTERRUPT TIMING [NON-FIFO MODE]**

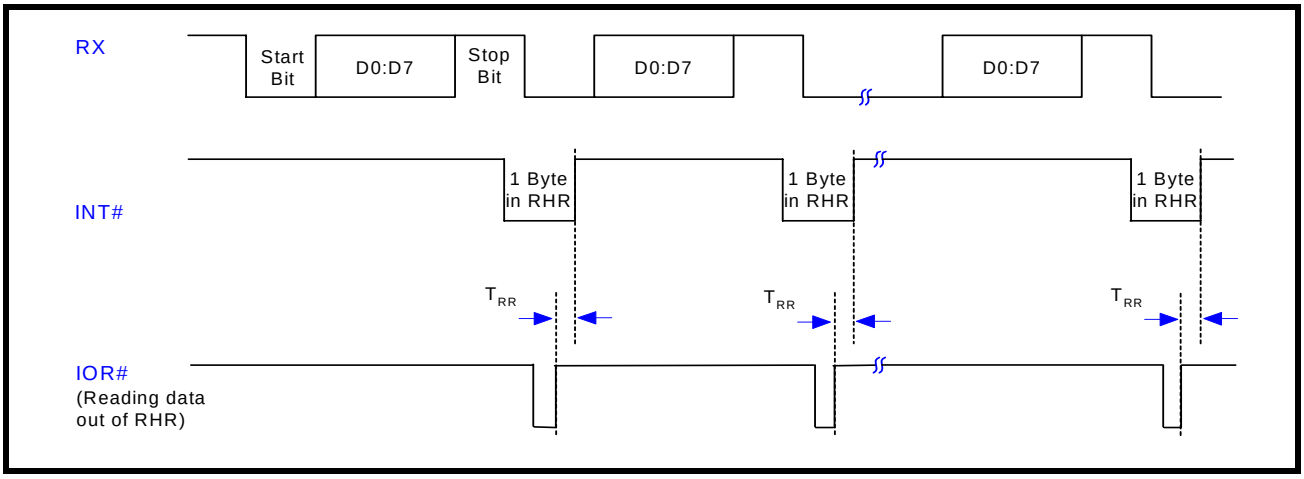


**FIGURE 22. TRANSMIT INTERRUPT TIMING [NON-FIFO MODE]**

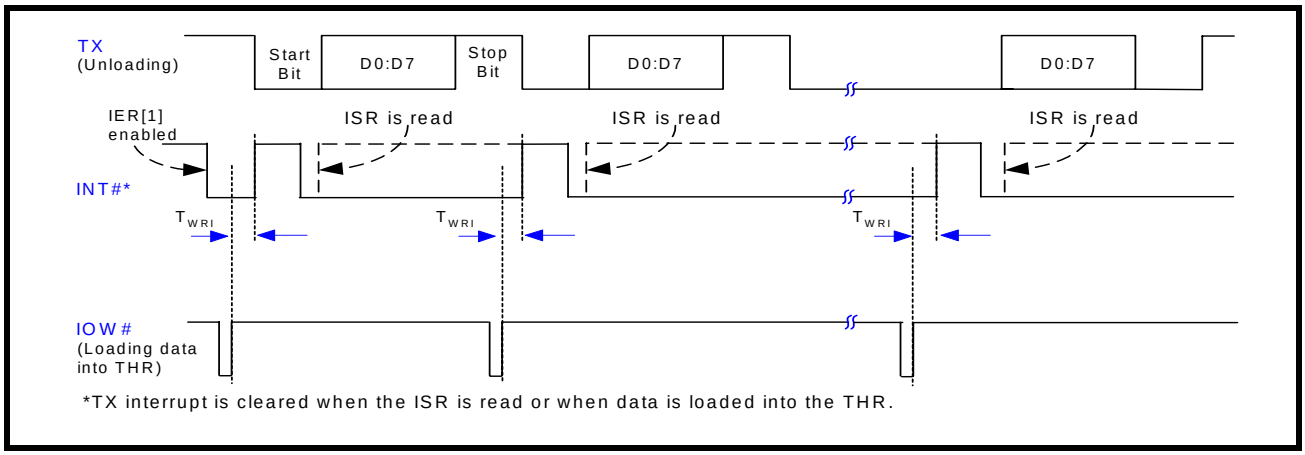



**FIGURE 23. RECEIVE INTERRUPT TIMING [FIFO MODE]**

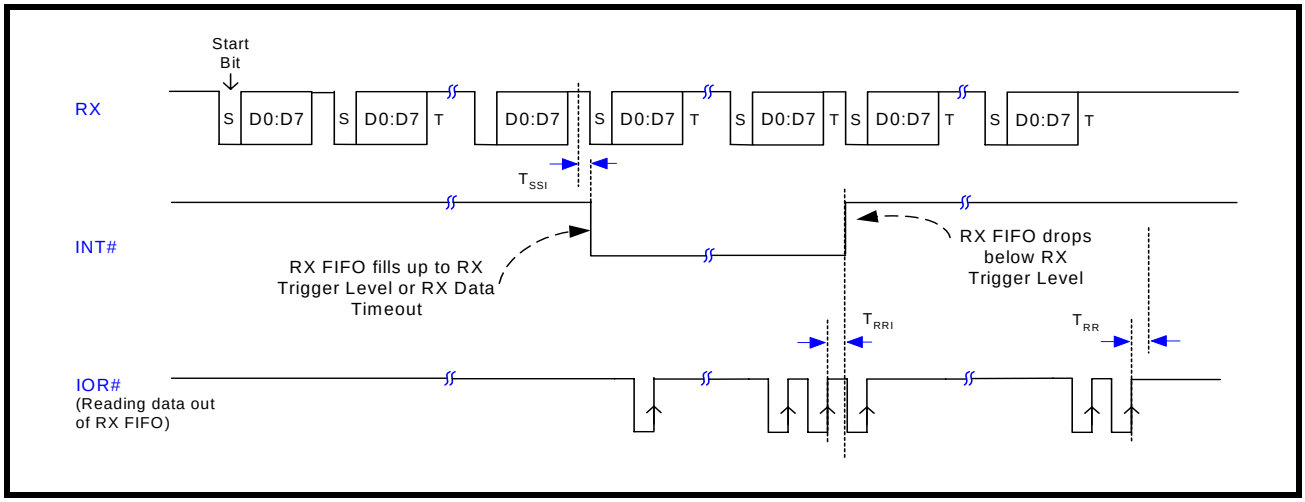
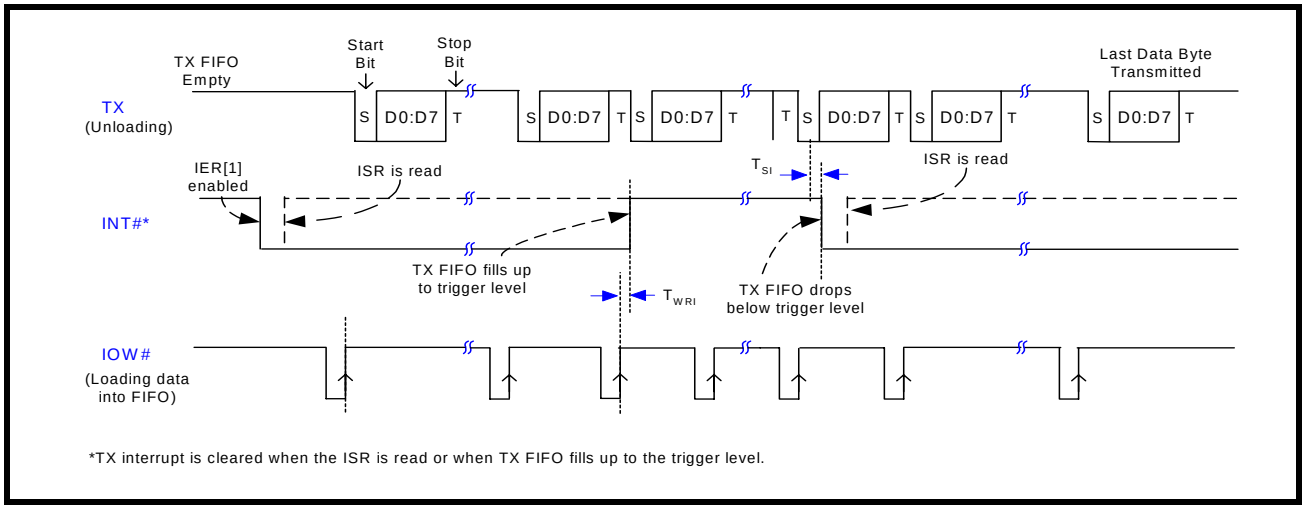
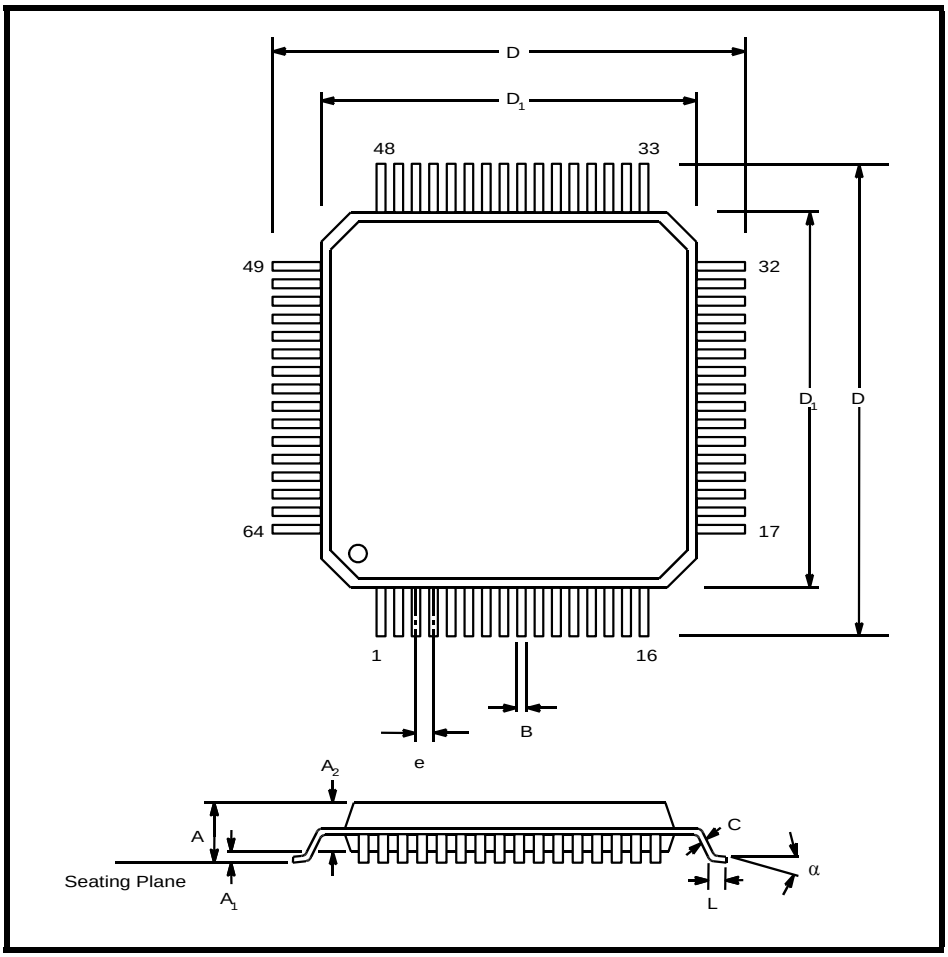



**FIGURE 24. TRANSMIT INTERRUPT TIMING [FIFO MODE]**



## PACKAGE DIMENSIONS, 64-LQFP




*Note: The control dimension is the millimeter column*

| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.055 | 0.063 | 1.40 | 1.60 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.053 | 0.057 | 1.35 | 1.45 |
| B | 0.007 | 0.011 | 0.17 | 0.27 |
| C | 0.004 | 0.008 | 0.09 | 0.20 |
| D | 0.465 | 0.480 | 11.80 | 12.20 |
| D1 | 0.390 | 0.398 | 9.90 | 10.10 |
| e | 0.020 BSC | | 0.50 BSC | |
| L | 0.018 | 0.030 | 0.45 | 0.75 |
| a | 0× | 7× | 0× | 7× |

## REVISION HISTORY

| REVISION | DESCRIPTION |
|---|---|
| P1.0.0 | Preliminary |
| 1.0.1 | Further clarification on A0-A7, RTS#, CTS#, DTR#, DSR# and ENIR pin description and throughout the datasheet, change $V_{IH}$ from 2.2V to 2.4V at 5V, change $V_{OH}$ from 2.4V to 2.0 at 3.3V and from 4V to 2.4V at 5V, change $I_{CC}$ from 10 to 5mA and its test condition to 2MHz. clock, and $I_{SLEEP}$ to 0.6 and 1.5mA for 3.3V and 5V respectively. Revised the AC timing table. |
| 1.0.2 | Updated values of AC Electrical Characteristics ($T_{AS}$, $T_{AH}$, $T_{CS}$, $T_{RD}$, $T_{ADS}$, $T_{ADH}$, $T_{WDS}$, $T_{WDH}$). Added Exar's UART Technical Support E-mail address to first and last page. |
| 1.1.0 | (June 2003) Added Device Status to Ordering Information. |
| 1.2.0 | (June 2004) Clarified pin descriptions- changed from using logic 1 and logic 0 to HIGH (VCC) and LOW (GND) for input and output pin descriptions. Added VOH vs. IOH and VOL vs. IOL curves (**Figure 16** and **Figure 17**). Clarified Transmit and Receive interrupt timing diagrams (**Figure 21**-**Figure 24**). DREV register was updated to 0x04 for devices with top mark date code of "D2 YYWW". |
| 1.2.1 | (February 2005) Corrected Trigger Table selection and programmable trigger level selection in **Table 14**. |
| 1.2.2 | (October 2005) Updated the 1.4mm-thick Quad Flat Pack package description from "TQFP" to "LQFP" to be consistent with the JEDEC and Industry norms. Clarified wake-up interrupt in Sleep Mode description. |
| 1.2.3 | (July 2008) Corrected description of Xon/Xoff/Special character interrupt. |

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