CS48500 Data Sheet

FEATURES

- Cost-effective, High-performance 32-bit DSP
  - 300,000,000 MAC/S (multiply accumulates per second)
  - Dual MAC cycles per clock
  - 72-bit accumulators are the most accurate in the industry
  - 24k x 32 SRAM, 2k blocks - assignable to data or program
  - Internal ROM contains a variety of configurable sound enhancement feature sets
  - 8-channel internal DMA
  - Internal watch-dog DSP lock-up prevention
- DSP Tool Set w/ Private Keys for Protecting Customer IP
- Configurable Serial Audio Inputs/Outputs
  - Configurable for all input/output types
  - Maximum 32-bit @ 192 kHz
  - Supports 32-bit audio sample I/O between DSP chips
  - TDM input modes (multiple channels on same line)
  - 192 kHz SPDIF transmitter
  - Multi-channel DSD direct stream digital SACD input
- Supports Two Different Input Fs Sample Rates
  - Output can be master or slave
  - Dual processing path capability
  - Input supports dual domain slave clocking
  - Hardware assist time sampling for sample rate conversion
- Integrated Clock Manager/PLL
  - Can operate from external crystal, external oscillator
- Input Fs Auto Detection
- Host & Boot via Serial Interface
- Configurable GPIOs and External Interrupt Input
- 1.8V Core / 3.3V I/O that are +5V Tolerant
- Low-power Mode
  - "Energy-Star Ready" via low-power mode, 350uW in standby

Differentiating from the legacy Cirrus multi-standard, multi-channel decoders, this new CS48500 family is still based on the same high-performance 32-bit fixed point DSP Digital Signal Processor core but instead is equipped with much less memory, tailoring it for more cost-effective applications associated with multi-channel and virtual-channel sound enhancements. Target applications are:

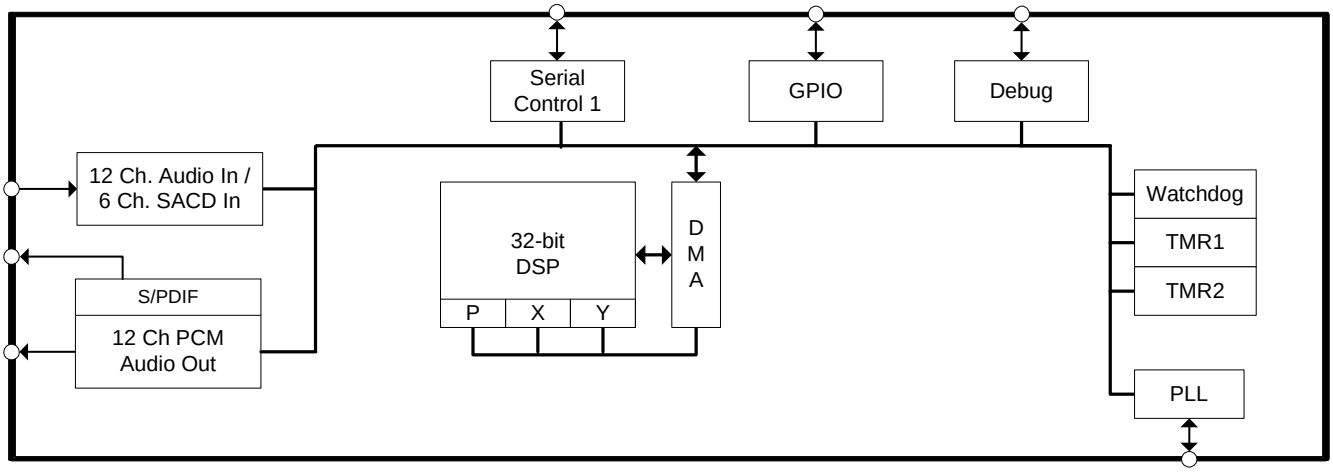
- Digital Televisions
- Multimedia Peripherals
- iPod® Docking Stations
- Automotive Head Units
- Automotive Outboard Amplifiers
- HD-DVD & Blu-ray Disc DVD Receivers
- PC Speakers

In these applications there are a wide variety of licensable DSP IP codes available today from:

Cirrus also has developed, or is developing their own royalty-free versions of popular features sets like Cirrus Bass Manager, Cirrus Dynamic Volume Leveler, Cirrus Original Multichannel Surround, Cirrus Virtual Speaker & Cirrus 3D-Audio.

The CS48500 is programmed using the Cirrus proprietary DSP Composer™ GUI development tool. Processing chains may be designed using a drag-and-drop interface to place/utilize functional macro audio DSP primitives. The end result is a software image that is down-loaded to the DSP via serial host or serial boot modes.

Ordering Information:
See page 23 for ordering information



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1. Documentation Strategy

The *CS48500 Data Sheet* describes the CS48500 family of multichannel audio processors. This document should be used in conjunction with the following documents when evaluating or designing a system around the CS48500 family of processors.

Document Name	Description
CS48500 Data Sheet	This document
CS48500 Hardware User's Manual	Includes detailed system design information including Typical Connection Diagrams, Boot-Procedures, Pin Descriptions, Etc.
AN298 - CS48500 Firmware User's Manual	Includes detailed firmware design information including signal processing flow diagrams and control API information
DSP Composer User's Manual	Includes detailed configuration and usage information for the GUI development tool.

Table 1. CS48500 Related Documentation

The scope of the *CS48500 Data Sheet* is primarily the hardware specifications of the CS48500 family of devices. This includes hardware functionality, characteristic data, pinout, and packaging information.

The intended audience for the *CS48500 Data Sheet* is the system PCB designer, mcu programmer, and the quality control engineer.

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2. Overview

The CS48500 DSP Family is designed to provide high-performance post-processing and mixing of ditial audio. The dual clock domain provided on the PCM inputs allows for the mixing of audio streams with different sampling frequencies. The low-power standby preserves battery life for applications which are always on, but not necessarily processing audio, such as automotive audio systems.

There are three devices comprising the CS48500 family. The CS48520, CS48540 and CS48560 are differentiated by the number of inputs and outputs available. All DSPs support dual input clock domains and dual audio processing paths. All DSPs are available in a 48-pin QFP package. Please refer to Table 2 on page 8 for the input, output, firmware features of each device.

2.1 Licensing

Licenses are required for all of the 3rd party audio processing algorithms listed in Section 3. Please contact your local Cirrus Logic Sales representative for more information.

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3. Code Overlays

The suite of software available for the CS48500 family consists of an operating system (OS) and a library of overlays. The overlays have been divided into three main groups called Matrix-processors, Virtualizer-processors, and Post-processors. All software components are defined below:

1. **OS/Kernel** - Encompasses all non-audio processing tasks, including loading data from external memory, processing host messages, calling audio-processing subroutines, error concealment, etc.

2. **Matrix-processor**- Any Module that performs a matrix decode on PCM data to produce more output channels than input channels (2⇨n channels). Examples are Dolby ProLogic IIx and DTS Neo:6. Generally speaking, these modules increase the number of valid channels in the audio I/O buffer.

3. **Virtualizer-processor** - Any module that encodes PCM data into fewer output channels than input channels (n⇨2 channels) with the effect of providing “phantom” speakers to represent the physical audio channels that were eliminated. Examples are Dolby Headphone® and Dolby Virtual Speaker®. Generally speaking, these modules reduce the number of valid channels in the audio I/O buffer.

4. **Post-processors** - Any module that processes audio I/O buffer PCM data in-place after the matrix- or virtualizer-processors. Examples are bass management, audio manager, tone control, EQ, delay, customer-specific effects, etc.

The bulk of each overlay is stored in ROM within the CS48500, but a small image is required to configure the overlays and boot the DSP. This small image can either be stored in an external serial FLASH/EEPROM, or downloaded via a host controller through the SPI™/I^2C® serial port.

The overlay structure reduces the time required to reconfigure the DSP when a processing change is requested. Each overlay can be reloaded independently without disturbing the other overlays. For example, when a new matrix-processor is selected, the OS, virtualizer-, and post-processors do not need to be reloaded — only the new matrix-processor (the same is true for the other overlays).

Table 2 below lists the firmware available based on device selection. Please refer AN298, *CS48500 Firmware User’s Manual* for the latest listing of application codes and Cirrus Framework™ modules available.

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Table 2. Device and Firmware Selection Guide

Device	Suggested Application	Chanenel Count Input/Output	Package
CS48520-CQZ	Digital TV Portable Audio Docking Station Portable DVD DVD Mini / Receiver Multimedia PC Speakers	Up to 4 channel in / 4 channel out	48-pin QFP
CS48540-CQZ **CS48540-DQZ**	CS48520 features Plus 8 Channel Car Audio DVD Receiver	Up to 8 channel in / 8 channel out	48-pin QFP
CS48560-CQZ **CS48560-DQZ**	CS48540 features Plus 12 channel Car Audio High-end Digital TV Dual Source/Dual Zone SACD	Up to 12 channel in /12 channel out	48-pin QFP

Note: Refer to AN298 for more information on Software features

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4. Hardware Functional Description

4.1 DSP Core

The CS48500 is a single-core DSP with separate X and Y data and P code memory spaces. The DSP core is a high-performance, 32-bit, user-programmable, fixed-point DSP that is capable of performing two multiply-and-accumulate (MAC) operations per clock cycle. The DSP core has eight 72-bit accumulators, four X- and four Y-data registers, and 12 index registers.

The DSP core is coupled to a flexible DMA engine. The DMA engine can move data between peripherals such as the serial control port (SCP), digital audio input (DAI) and digital audio output (DAO), or any DSP core memory, all without the intervention of the DSP. The DMA engine off loads data move instructions from the DSP core, leaving more MIPS available for signal processing instructions.

CS48500 functionality is controlled by application codes that are stored in on-board ROM or downloaded to the CS48500 from a host controller or external serial FLASH/EEPROM.

Users can develop their applications using DSP Composer to create the processing chain and then compile the image into a series of commands that are sent to the CS48500 through the SCP. The processing application can either load modules (matrix-processors, virtualizers, post-processors) from the DSPs on-board ROM, or custom firmware can be downloaded through the SCP.

The CS48500 is suitable for a variety of audio post-processing applications such as automotive head-ends, automotive amplifiers, and boom boxes.

4.1.1 DSP Memory

The DSP core has its own on-chip data and program RAM and ROM and does not require external memory for post-processing applications.

The Y-RAM and P-RAM share a single block of memory that can be configured to make Y and P equal in size, or more memory can be allocated for Y-RAM in 2kword blocks.

4.1.2 DMA Controller

The powerful 8-channel DMA controller can move data between 8 on-chip resources. Each resource has its own arbiter: X, Y, and P RAMs/ROMs and the peripheral bus. Modulo and linear addressing modes are supported, with flexible start address and increment controls. The service intervals for each DMA channel, as well as up to 6 interrupt events, are programmable.

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4.2 On-chip DSP Peripherals

4.2.1 Digital Audio Input Port (DAI)

Each version of the CS48500 support a different number of input channels. Refer toTable 2 on page 8 for more details.

The DAI port supports a wide variety of data input formats at sample rates (Fs) as high as 192 kHz. The port is capable of accepting PCM or DSD formats. Up to 32-bit word lengths are supported. DSD is supported and internally converted to PCM before processing. The DAI also supports a time division multiplexed (TDM) one-line data mode, that packs PCM audio on a single data line (the total number possible depends on the ratio of SCLK to LRCLK and the version of chip. For example on the CS48520 only 4 ch of PCM are supported in one line mode and on the CS48560 up to 8 channels are supported.).

The port has two independent slave-only clock domains. Each data input can be independently assigned to a clock domain. The sample rate of the input clock domains can be determined automatically by the DSP, off-loading the task of monitoring the SPDIF receiver from the host. A time-stamping feature allows the input data to be sample-rate converted via software.

4.2.2 Digital Audio Output Port (DAO)

Each version of the CS48500 support a different number of output channels. Refer toTable 2 on page 8 for more details.

DAO port supports PCM resolutions of up to 32-bits. The port supports sample rates (Fs) as high as 192 kHz. The port can be configured as an independent clock domain mastered by the DSP, or as a clock slave if an external MCLK or SCLK/LRCLK source is available. One of the serial audio pins can be re-configured as a SPDIF transmitter that drives a bi-phase encoded S/PDIF signal (data with embedded clock on a single line).

4.2.3 Serial Control Port ($I^2C^®$ or SPI™)

The on-chip serial control port is capable of operating as master or slave in either SPI™ or $I^2C^®$ modes. Master/Slave operation is chosen by mode select pins when the CS48500 comes out of reset. The serial clock pin can support frequencies as high as 25 MHz in SPI mode (SPI clock speed must always be ≤ (F_{dclk}/2)). The CS48500 serial control port also includes a pin for flow control of the communications interface (#SCP_BSY) and a pin to indicate when the DSP has a message for the host (#SCP_IRQ).

4.2.4 GPIO

Many of the CS48500 peripheral pins are multiplexed with GPIO. Each GPIO can be configured as an output, an input, or an input with interrupt. Each input-pin interrupt can be configured as rising edge, falling edge, active-low, or active-high.

4.2.5 PLL-based Clock Generator

The low-jitter PLL generates integer or fractional multiples of a reference frequency which are used to clock the DSP core and peripherals. Through a second PLL divider chain, a dependent clock domain can be output on the DAO port for driving audio converters. The CS48500 defaults to running from the external reference frequency and is switched to use the PLL output after overlays have been loaded and configured, either through master boot from an external FLASH or through host control. A built-in crystal oscillator circuit with a buffered output is provided. The buffered output frequency ratio is selectable between 1:1 (default) or 2:1.

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4.2.6 Hardware Watchdog Timer

The CS48500 has an integrated watchdog timer that acts as a “health” monitor for the DSP. The watchdog timer must be reset by the DSP before the counter expires, or the entire chip is reset. This peripheral ensures that the CS48500 will reset itself in the event of a temporary system failure. In stand-alone mode (i.e. no host mcu), the DSP will reboot from external FLASH. In slave mode (i.e. host mcu present) a GPIO will be used to signal the host that the watchdog has expired and the DSP should be rebooted and re-configured.

4.3 DSP I/O Description

4.3.1 Multiplexed Pins

Many of the CS48500 pins are multi-functional. For details on pin functionality please refer to the *CS48500 Hardware User’s Manual*.

4.3.2 Termination Requirements

Open-drain pins on the CS48500 must be pulled high for proper operation. Please refer to the *CS48500 Hardware User’s Manual* to identify which pins are open-drain and what value of pull-up resistor is required for proper operation.

Mode select pins on the CS48500 are used to select the boot mode upon the rising edge from reset. A detailed explanation of termination requirements for each communication mode select pin can be found in the *CS48500 Hardware User’s Manual*.

4.3.3 Pads

The CS48500 I/Os operate from the 3.3 V supply and are 5 V tolerant.

4.4 Application Code Security

The external program code may be encrypted by the programmer to protect any intellectual property it may contain. A secret, customer-specific key is used to encrypt the program code that is to be stored external to the device. Please contact your local Cirrus representative for details.

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5. Characteristics and Specifications

Note: All data sheet minimum and maximum timing parameters are guaranteed over the rated voltage and temperature. All data sheet typical parameters are measured under the following conditions: T = 25 °C, C_L = 20 pF, VDD = VDDA = 1.8 V, VDDIO = 3.3 V, GNDD = GNDIO = GNDA = 0 V.

5.1 Absolute Maximum Ratings

(GNDD = GNDIO = GNDA = 0 V; all voltages with respect to 0 V)

Parameter		Symbol	Min	Max	Unit
DC power supplies:	Core supply	VDD	–0.3	2.0	V
	PLL supply	VDDA	–0.3	3.6	V
	I/O supply	VDDIO	–0.3	3.6	V
	|VDDA – VDDIO|		-	0.3	V
Input pin current, any pin except supplies		I_{in}	-	+/- 10	mA
Input voltage on PLL_REF_RES		V_{filt}	-0.3	3.6	V
Input voltage on I/O pins		V_{inio}	-0.3	5.0	V
Storage temperature		T_{stg}	–65	150	°C

Caution: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

5.2 Recommended Operating Conditions

(GNDD = GNDIO = GNDA = 0 V; all voltages with respect to 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
DC power supplies:	Core supply	VDD	1.71	1.8	1.89	V
	PLL supply	VDDA	3.13	3.3	3.46	V
	I/O supply	VDDIO	3.13	3.3	3.46	V
	|VDDA – VDDIO|			0		V
Ambient operating temperature		T_A		-		°C
	- CQZ		0		+ 70	
	- DQZ		- 40		+ 85	

Note: It is recommended that the 3.3 V IO supply come up ahead of or simultaneously with the 1.8 V core supply.

5.3 Digital DC Characteristics

(Measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	2.0	-	-	V
Low-level input voltage, except XTI	V_{IL}	-	-	0.8	V
Low-level input voltage, XTI	V_{ILXTI}	-	-	0.6	V
Input Hysteresis	V_{hys}		0.4		V
High-level output voltage (I_O = -2mA), except XTI	V_{OH}	VDDIO * 0.9	-	-	V
Low-level output voltage (I_O = 2mA), except XTI	V_{OL}	-	-	VDDIO * 0.1	V
Input leakage current (all digital pins with internal pull-up resistors disabled)	I_{IN}	-	-	5	µA
Input leakage current (all digital pins with internal pull-up resistors enabled, and XTI)	I_{IN-PU}	-	-	56	µA

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5.4 Power Supply Characteristics

(measurements performed under operating conditions)

Parameter	Min	Typ	Max	Unit
Operational Power Supply Current:				
VDD: Core and I/O operating[1]	-	203	-	mA
VDDA: PLL operating	-	8	-	mA
VDDIO: With most ports operating	-	27	-	mA
Total Operational Power Dissipation:		469		mW
Standby Power Supply Current:				
VDD: Core and I/O not clocked	-	100	-	µA
VDDA: PLL halted	-	1	-	µA
VDDIO: All connected I/O pins 3-stated by other ICs in system	-	15	-	µA
Total Standby Power Dissipation:	-	350	-	µW

1.Dependent on application firmware and DSP clock speed.

5.5 Thermal Data (48 LQFP)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)					
Two-layer Board[1]	θ_{ja}	-	63.5	-	°C / Watt
Four-layer Board[2]		-	54	-	
Thermal Resistance (Junction to Top of Package)					
Two-layer Board[1]	ψ_{jt}	-	0.70	-	°C / Watt
Four-layer Board[2]		-	0.64	-	

Notes: 1. Two-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20 % of the top & bottom layers.

2. Four-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20 % of the top & bottom layers and 0.5-oz. copper covering 90 % of the internal power plane & ground plane layers.

3. To calculate the die temperature for a given power dissipation

   T_j = Ambient Temperature + [(Power Dissipation in Watts) * θ_{ja}]

4. To calculate the case temperature for a given power dissipation

   $T_c = T_j$ - [(Power Dissipation in Watts) * ψ_{jt}]

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5.6 Switching Characteristics— RESET

Parameter	Symbol	Min	Max	Unit
RESET# minimum pulse width low	T_{rstl}	1	-	µs
All bidirectional pins high-Z after RESET# low	T_{rst2z}	-	100	ns
Configuration pins setup before RESET# high	T_{rstsu}	50	-	ns
Configuration pins hold after RESET# high	T_{rsthld}	20	-	ns

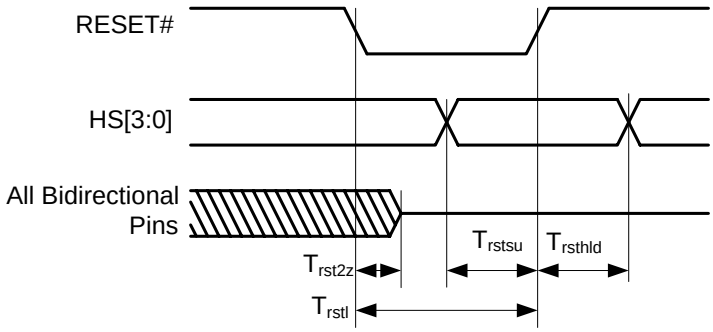


Figure 1. RESET Timing

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5.7 Switching Characteristics — XTI

Parameter	Symbol	Min	Max	Unit
External Crystal operating frequency	F_{xtal}	10	30	MHz
XTI period	T_{clki}	33.3	100	ns
XTI high time	T_{clkih}	13.3	-	ns
XTI low time	T_{clkil}	13.3	-	ns
External Crystal Load Capacitance (parallel resonant)[1]	C_L	10	18	pF
External Crystal Equivalent Series Resistance	ESR		50	Ω

1. C_L refers to the total load capacitance as specified by the crystal manufacturer. Crystals which require a C_L outside this range should be avoided. The crystal oscillator circuit design should follow the crystal manufacturer's recommendation for load capacitor selection.

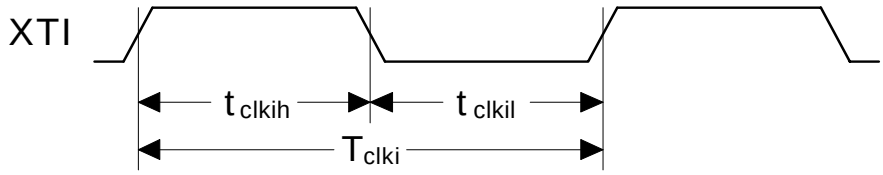


Figure 2. XTI Timing

5.8 Switching Characteristics — Internal Clock

Parameter	Symbol	Min	Max	Unit
Internal DCLK frequency[1]	F_{dclk}	-		MHz
CS4852x-CQZ		F_{xtal}	150	
CS4854x-CQZ		F_{xtal}	150	
CS4856x-CQZ		F_{xtal}	150	
CS4852x-DQZ		F_{xtal}	150	
CS4854x-DQZ		F_{xtal}	150	
CS4856x-DQZ				
Internal DCLK period[1]	DCLKP	-		ns
CS4852x-CQZ		6.7	$1/F_{xtal}$	
CS4854x-CQZ		6.7	$1/F_{xtal}$	
CS4856x-CQZ		6.7	$1/F_{xtal}$	
CS4852x-DQZ		6.7	$1/F_{xtal}$	
CS4854x-DQZ		6.7	$1/F_{xtal}$	
CS4856x-DQZ		6.7	$1/F_{xtal}$	

1. After initial power-on reset, $F_{dclk} = F_{xtal}$. After initial kickstart commands, the PLL is locked to max F_{dclk} and remains locked until the next power-on reset.

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5.9 Switching Characteristics — Serial Control Port - SPI Slave Mode

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Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{spisck}	-		25	MHz
SCP_CS# falling to SCP_CLK rising	t_{spicss}	24		-	ns
SCP_CLK low time	t_{spickl}	20		-	ns
SCP_CLK high time	t_{spickh}	20		-	ns
Setup time SCP_MOSI input	t_{spidsu}	5		-	ns
Hold time SCP_MOSI input	t_{spidh}	5		-	ns
SCP_CLK low to SCP_MISO output valid	t_{spidov}	-		8	ns
SCP_CLK falling to SCP_IRQ# rising	$t_{spiirqh}$	-		20	ns
SCP_CS# rising to SCP_IRQ# falling	$t_{spiirql}$	0			ns
SCP_CLK low to SCP_CS# rising	t_{spicsh}	24		-	ns
SCP_CS# rising to SCP_MISO output high-Z	$t_{spicsdz}$	-	20		ns
SCP_CLK rising to SCP_BSY# falling	$t_{spicbsyl}$	-	3*DCLKP+20		ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the SCP_BSY# pin should be implemented to prevent overflow of the input data buffer.

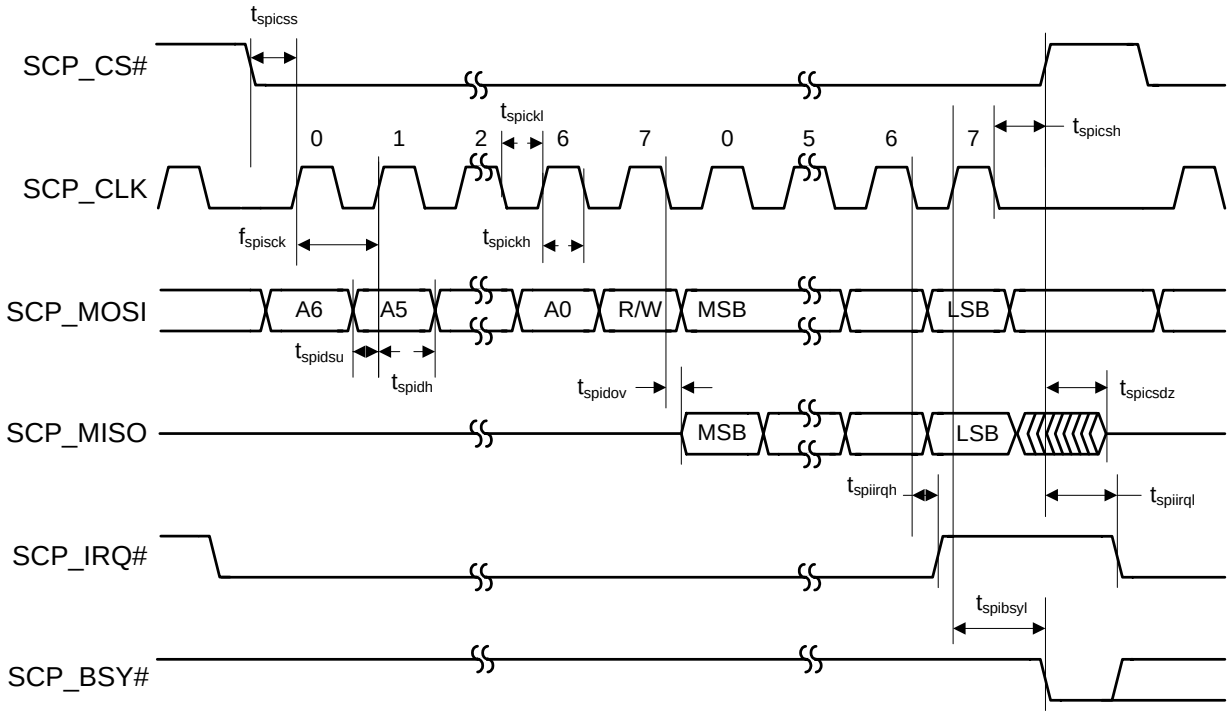


Figure 3. Serial Control Port - SPI Slave Mode Timing

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5.10 Switching Characteristics — Serial Control Port - SPI Master Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{spisck}	-		25	MHz
SCP_CS# falling to SCP_CLK rising [2]	t_{spicss}	-	11*DCLKP + (SCP_CLK PERIOD)/2	-	ns
SCP_CLK low time	t_{spickl}	20		-	ns
SCP_CLK high time	t_{spickh}	20		-	ns
Setup time SCP_MISO input	t_{spidsu}	9		-	ns
Hold time SCP_MISO input	t_{spidh}	5		-	ns
SCP_CLK low to SCP_MOSI output valid	t_{spidov}	-		8	ns
SCP_CLK low to SCP_CS# falling	t_{spicsl}	7		-	ns
SCP_CLK low to SCP_CS# rising	t_{spicsh}	-	11*DCLKP + (SCP_CLK PERIOD)/2	-	ns
Bus free time between active SCP_CS#	t_{spicsx}		3*DCLKP	-	ns
SCP_CLK falling to SCP_MOSI output high-Z	t_{spidz}	-		20	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.
2. SCP_CLK PERIOD refers to the period of SCP_CLK as being used in a given application. It does not refer to a tested parameter

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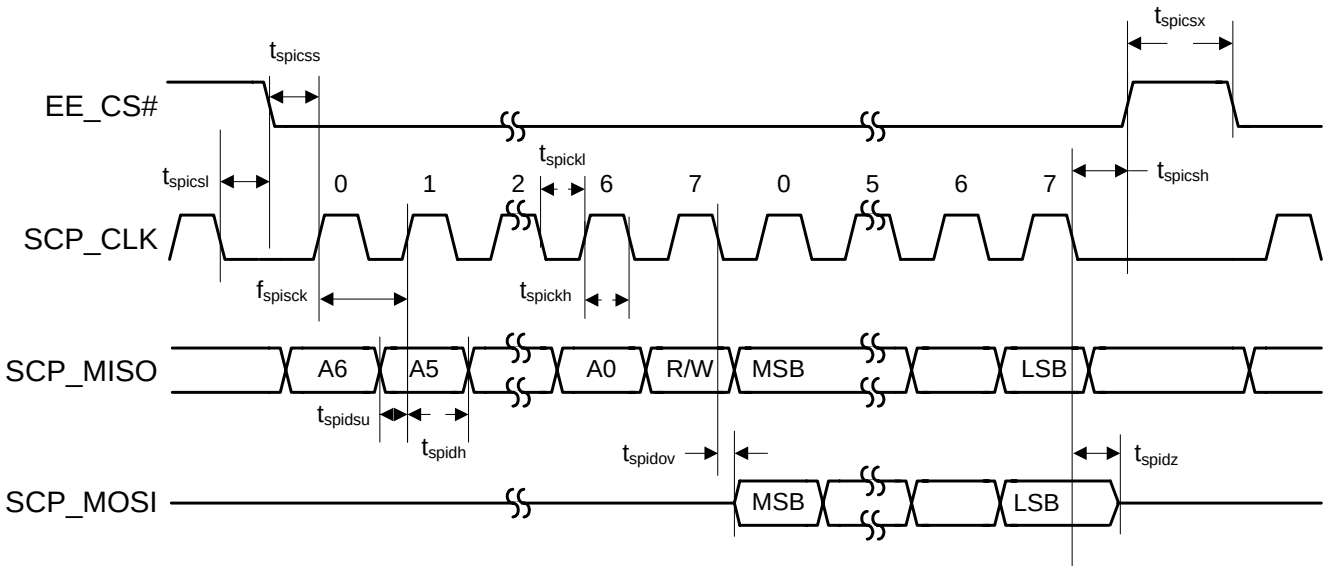


Figure 4. Serial Control Port - SPI Master Mode Timing

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5.11 Switching Characteristics — Serial Control Port - I²C Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{iicck}	-		400	kHz
SCP_CLK low time	t_{iicckl}	1.25		-	µs
SCP_CLK high time	t_{iicckh}	1.25		-	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25			µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25		-	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5		-	µs
Bus free time between STOP and START conditions	t_{iicbft}	3		-	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100			ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	20		-	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	-		18	ns
SCP_CLK falling to SCP_IRQ# rising	$t_{iicirqh}$	-		3*DCLKP + 40	ns
NAK condition to SCP_IRQ# low	$t_{iicirql}$		3*DCLKP + 20		ns
SCP_CLK rising to SCB_BSY# low	$t_{iicbsyl}$	-	3*DCLKP + 20		ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the SCP_BSY# pin should be implemented to prevent overflow of the input data buffer.

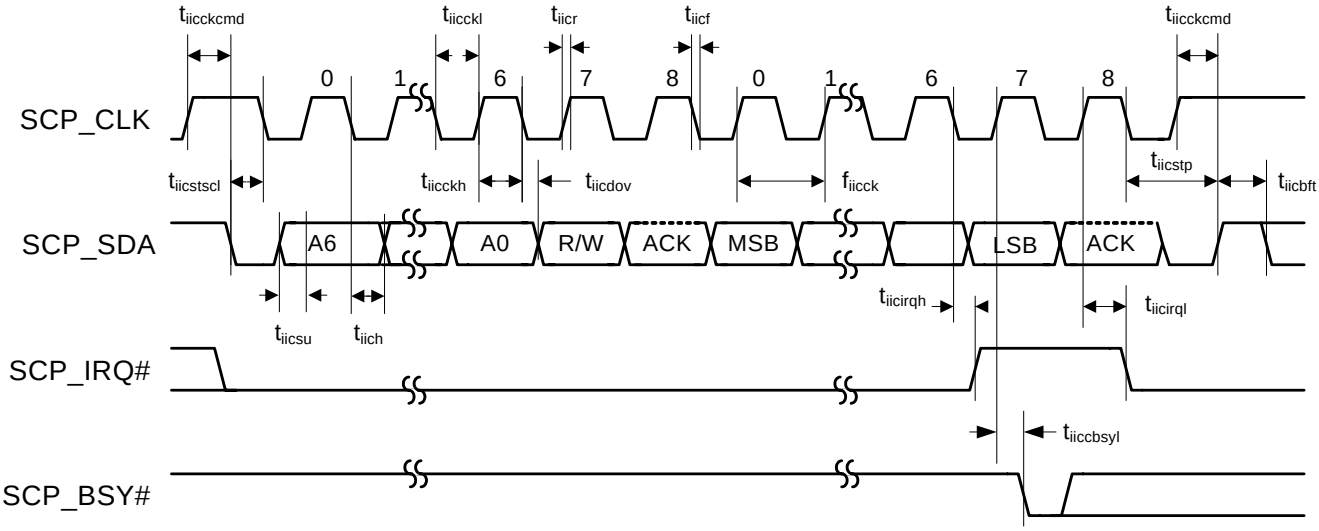


Figure 5. Serial Control Port - I²C Slave Mode Timing

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5.12 Switching Characteristics — Serial Control Port - I²C Master Mode

Parameter	Symbol	Min	Max	Units
SCP_CLK frequency[1]	f_{iicck}	-	400	kHz
SCP_CLK low time	t_{iicckl}	1.25	-	µs
SCP_CLK high time	t_{iicckh}	1.25	-	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25		µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	-	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	-	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	-	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100		ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	20	-	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	-	18	ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.

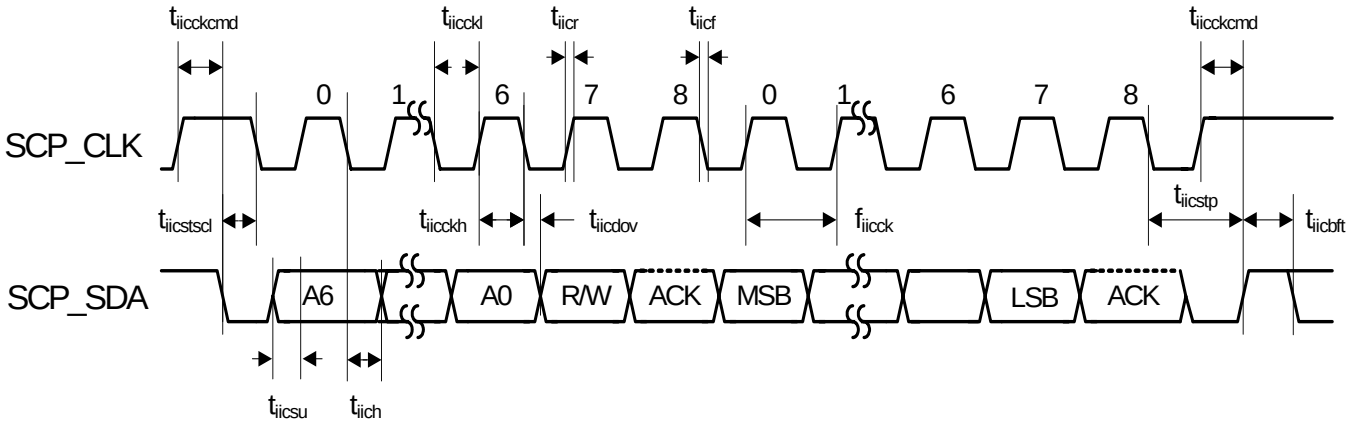


Figure 6. Serial Control Port - I²C Master Mode Timing

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5.13 Switching Characteristics — Digital Audio Slave Input Port

Parameter	Symbol	Min	Max	Unit
DAI_SCLK period	$T_{daiclkp}$	40	-	ns
DAI_SCLK duty cycle	-	45	55	%
Setup time DAI_DATAn	t_{daidsu}	10	-	ns
Hold time DAI_DATAn	t_{daidh}	5	-	ns

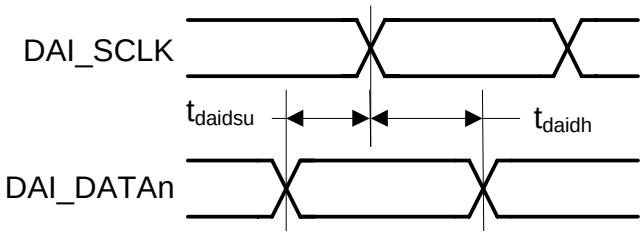


Figure 7. Digital Audio Input (DAI) Port Timing Diagram

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5.14 Switching Characteristics — DSD Slave Input Port

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Duty Cycle	-	40	-	60	%
DSD_SCLK Pulse Width Low	t_{sclkl}	78	-	-	ns
DSD_SCLK Pulse Width High	t_{sclkh}	78	-	-	ns
DSD_SCLK Frequency (64x Oversampled)	-	1.024	-	3.2	MHz
(128x Oversampled)	-	2.048	-	6.4	MHz
DSD_A / _B valid to DSD_SCLK rising setup time	t_{sdlrs}	20	-	-	ns
DSD_SCLK rising to DSD_A or DSD_B hold time	t_{sdh}	20	-	-	ns
DSD clock to data transition (Phase Modulation mode)	t_{dpm}	-20	-	20	ns

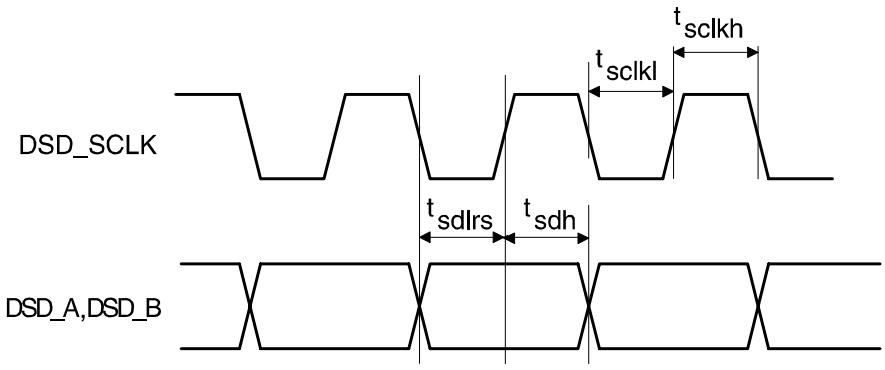


Figure 8. Direct Stream Digital - Serial Audio Input Timing

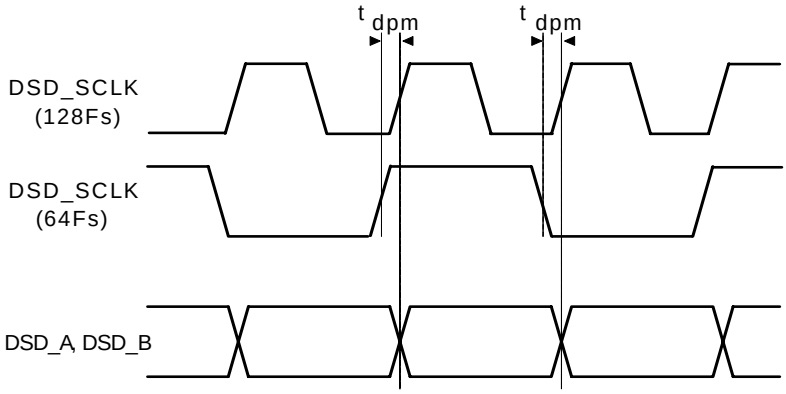


Figure 9. Direct Stream Digital - Serial Audio Input Timing for Phase Modulation Mode

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5.15 Switching Characteristics — Digital Audio Output Port

Parameter	Symbol	Min	Max	Unit
DAO_MCLK period	$T_{daomclk}$	40	-	ns
DAO_MCLK duty cycle	-	40	60	%
DAO_SCLK period for Master or Slave mode[1]	$T_{daosclk}$	40	-	ns
DAO_SCLK duty cycle for Master or Slave mode[1]	-	40	60	%
Master Mode (Output A1 Mode)[1,2]				
DAO_SCLK delay from DAO_MCLK rising edge, DAO_MCLK as an input	$t_{daomsck}$	-	19	ns
DAO_LRCLK delay from DAO_SCLK transition, respectively[3]	$t_{daomstlr}$	-	8	ns
DAO1_DATA[3..0], DAO2_DATA[1..0] delay from DAO_SCLK transition[3]	t_{daomdv}	-	10	ns
Slave Mode (Output A0 Mode)[4]				
DAO1_DATA[3..0], DAO2_DATA[1..0] delay from DAO_SCLK transition[3]	t_{daosdv}		15	ns

1.Master mode timing specifications are characterized, not production tested.

2.Master mode is defined as the CS48500 driving both DAO_SCLK, DAO_LRCLK. When MCLK is an input, it is divided to produce DAO_SCLK, DAO_LRCLK.

3.This timing parameter is defined from the non-active edge of DAO_SCLK. The active edge of DAO_SCLK is the point at which the data is valid.

4.Slave mode is defined as DAO_SCLK, DAO_LRCLK driven by an external source.

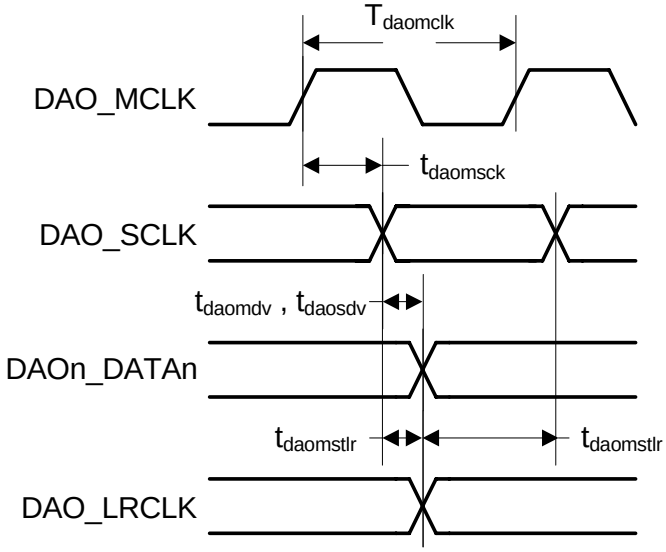


Figure 11. Digital Audio Port Timing, MCLK Master Mode

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6. Ordering Information

The CS48500 family part number is described as follows:

CS485NI-XYZ

where

N - Product Number Variant

I - ROM ID Number

X - Product Grade

Y - Package Type

Z - Lead (Pb) Free

Table 3. Ordering Information

Part No.	Grade	Temp. Range	Package
CS48520-CQZ	Commercial	0 to +70 °C	48-pin LQFP
CS48540-CQZ	Commercial	0 to +70 °C	
CS48540-DQZ	Automotive	-40 to +85 °C	
CS48560-CQZ	Commercial	0 to +70 °C	
CS48560-DQZ	Automotive	-40 to +85 °C	

NOTE: Please contact the factory for availability of the -D (automotive grade) package.

7. Environmental, Manufacturing, & Handling Information

Table 4. Environmental, Manufacturing, & Handling Information

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS48520-CQZ	260 °C	3	7 Days
CS48540-CQZ			
CS48540-DQZ			
CS48560-CQZ			
CS48560-DQZ			

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

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8. Device Pinout Diagrams

8.1 CS48520, 48-pin LQFP Pinout Diagram

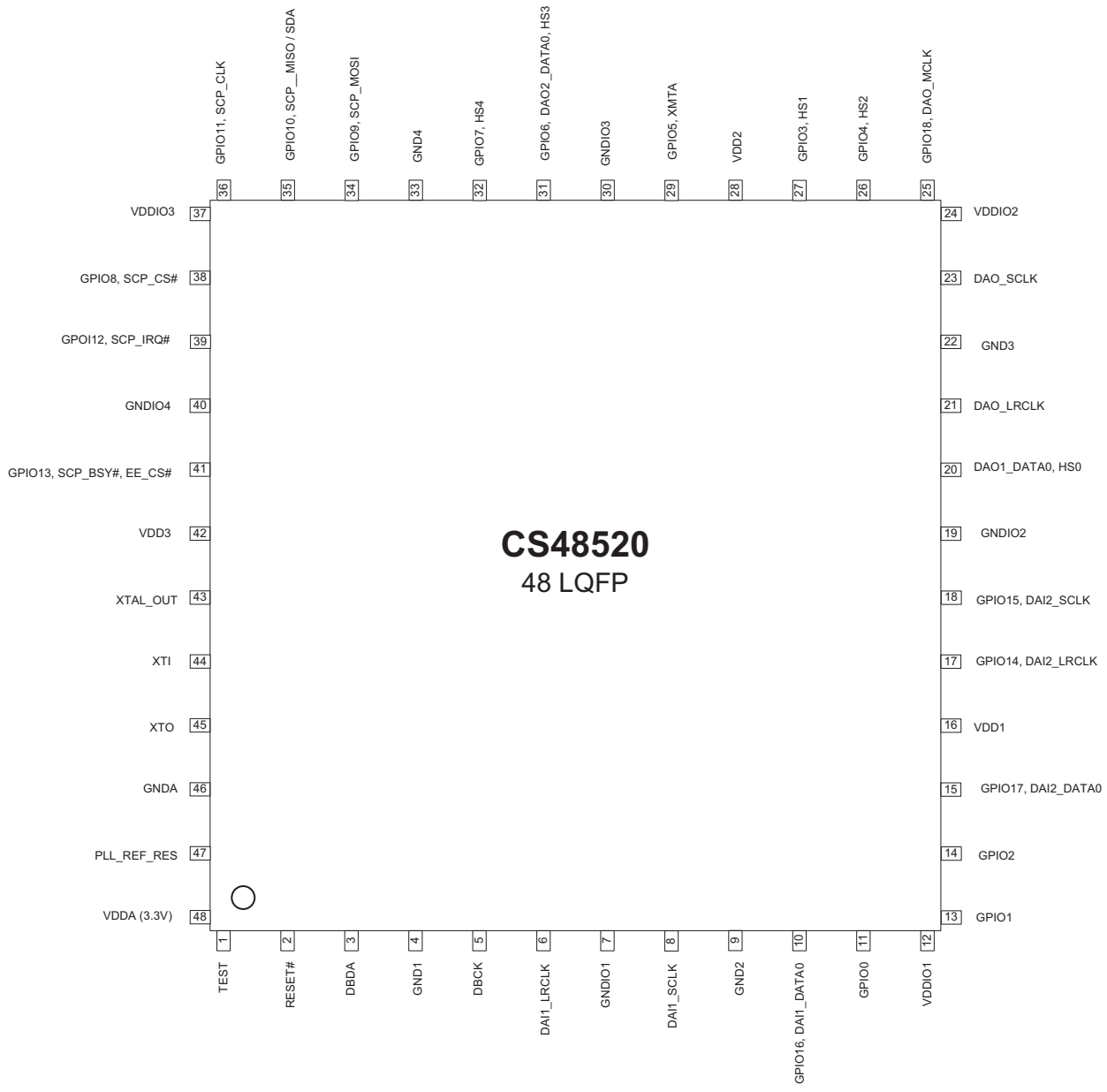


Figure 12. CS48520, 48-Pin LQFP Pinout

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8.2 CS48540, 48-pin LQFP Pinout Diagram

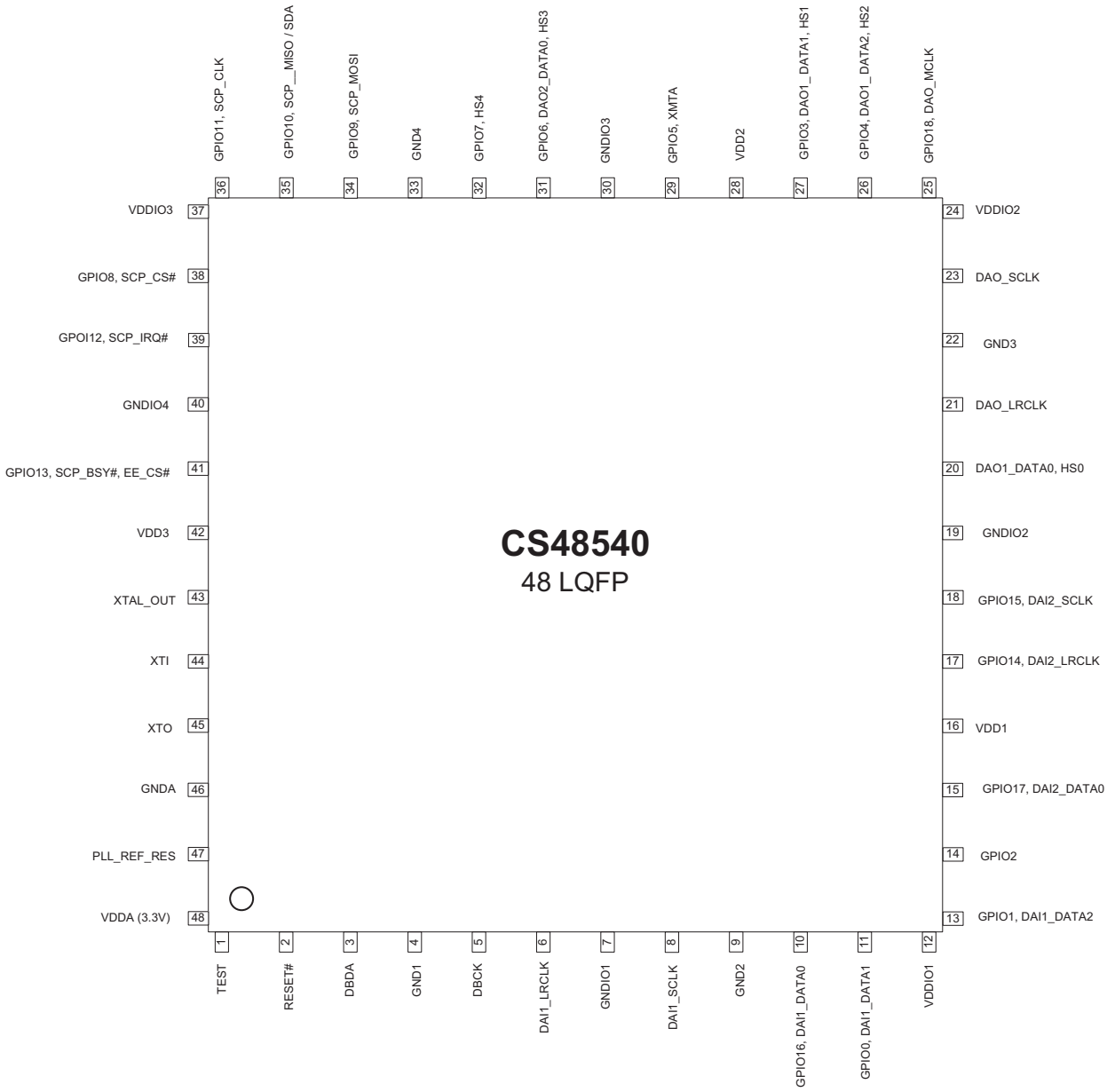


Figure 13. CS48540, 48-Pin LQFP Pinout

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8.3 CS48560,48-pin LQFP Pinout Diagram

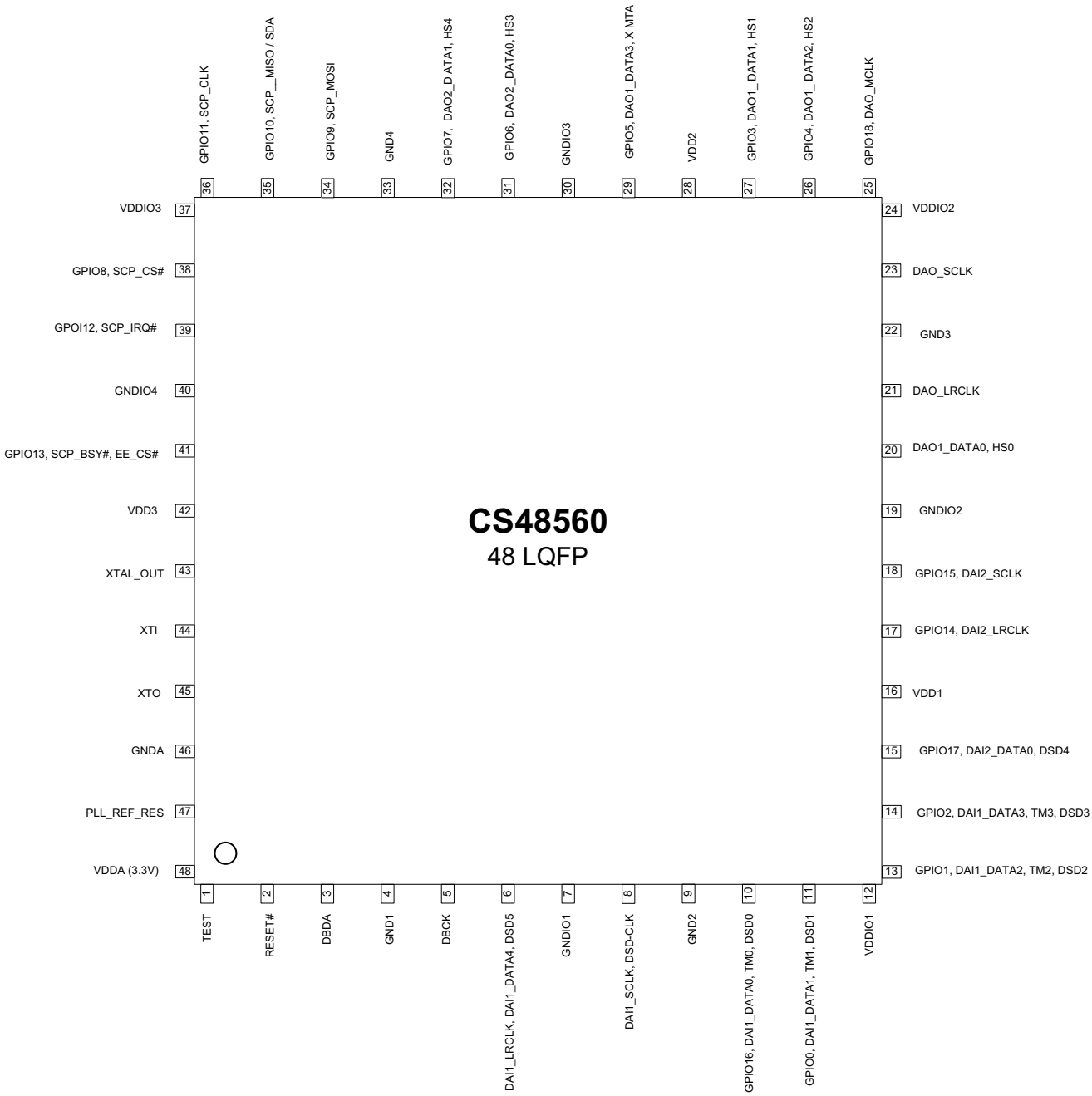
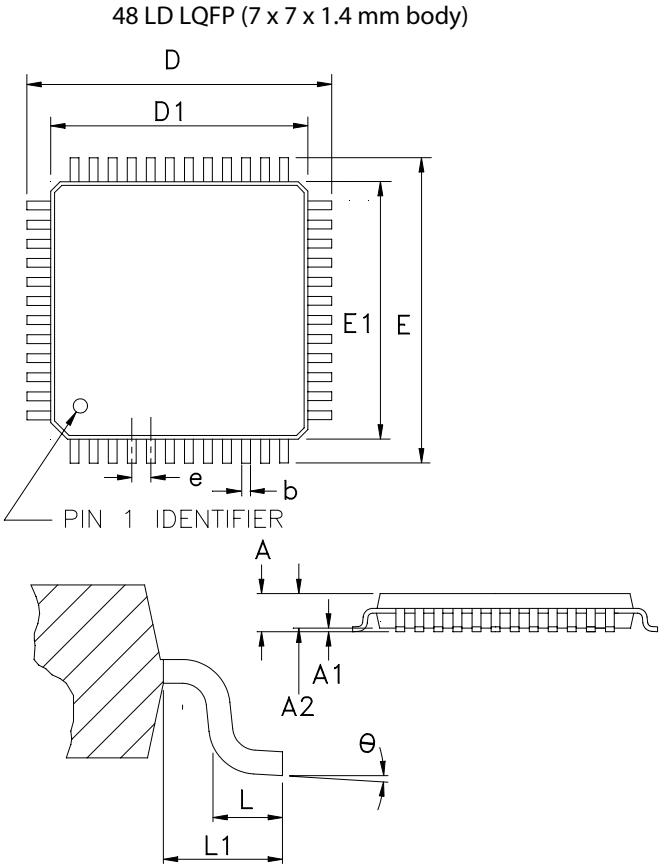


Figure 14. CS48560, 48-Pin LQFP Pinout

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9. Package Mechanical Drawings

9.1 48-pin LQFP Package Drawing



	Number of Leads		
	48		
	MIN	NOM	MAX
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
theta	0		7
L	0.45	0.60	0.75
L1	1.00 REF		

NOTES:
1) Reference document: JEDEC MS-026
2) All dimensions are in millimeters and controlling dimension is in millimeters.
3) D1 and E1 do not include mold flash which is 0.25 mm max. per side.A1
4) Dimension b does not include a total allowable dambar protrusion of 0.08 mm max.

Figure 15. 48-Pin LQFP Package Drawing

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10. Revision History

Revision	Date	Changes
A1	JUL 2006	Advance release.
A2	JUL 2006	Updated pinout definition for pins 26 and 27. Updated typical power numbers.
A3	DEC 5 2006	Updated sections 2.0, 4.2.1, 5.8, Table 3, Table 4, to show new device numbering scheme. Updated sections 8.1, 8.2, 8.3.

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