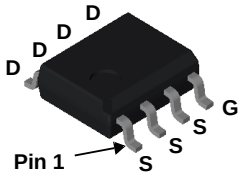
MOSFET, N-Channel, POWERTRENCH®

40 V, 18.6 A, 4.5 mΩ

FDS8840NZ

ON Semiconductor®

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SOIC8
CASE 751EB

General Description

The FDS8840NZ has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance.

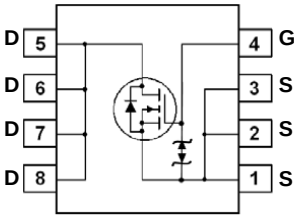
Features

- Max $r_{DS(on)}$ = 4.5 mΩ at V_{GS} = 10 V, I_D = 18.6 A
- Max $r_{DS(on)}$ = 6.0 mΩ at V_{GS} = 4.5 V, I_D = 14.9 A
- HBM ESD Protection Level of 6 kV Typical (Note 3)
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$ and Fast Switching
- High Power and Current Handling Capability
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

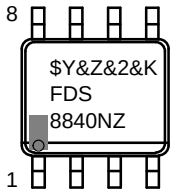
Applications

- Synchronous Buck for Vcore and Server
- Notebook Battery Pack
- Load Switch

PIN ASSIGNMENT



MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&2	= Numeric Date Code
&K	= Lot Code
FDS8840NZ	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ORDERING INFORMATION

Part Number	Device Marking	Package	Shipping†
FDS8840NZ	FDS8840NZ	SOIC8 (Pb-Free / Halogen Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous	18.6	A
	Drain Current Pulsed	63	
E_{AS}	Single Pulse Avalanche Energy (Note 4)	600	mJ
P_D	Power Dissipation, T_A = 25°C (Note 1a)	2.5	W
	Power Dissipation, T_A = 25°C (Note 1b)	1.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		31		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		−6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 18.6 A		3.9	4.5	mΩ
		V_{GS} = 4.5 V, I_D = 14.9 A		4.6	6.0	
		V_{GS} = 10 V, I_D = 18.6 A, T_J = 125°C		5.9	7.0	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 18.6 A		83		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		5665	7535	pF
C_{oss}	Output Capacitance			650	865	pF
C_{rss}	Reverse Transfer Capacitance			445	670	pF
R_g	Gate Resistance			1.2		Ω

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Switching Characteristics							
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 20 V, I_D = 18.6 A, V_{GS} = 10 V, R_{GEN} = 6 Ω			18	32	ns
t_r	Rise Time				13	23	ns
$t_{d(off)}$	Turn−Off Delay Time				57	103	ns
t_f	Fall Time				11	20	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V	V_{DD} = 20 V, I_D = 18.6 A		103	144	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 5 V			54	76	nC
Q_{gs}	Gate to Source Charge				16		nC
Q_{gd}	Gate to Drain “Miller” Charge				19		nC
Drain−Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 18.6 A			0.8	1.2	V
		V_{GS} = 0 V, I_S = 2.1 A			0.7	1.2	
t_{rr}	Reverse Recovery Time	I_F = 18.6 A, di/dt = 100 A/μs			33	53	ns
Q_{rr}	Reverse Recovery Charge				21	34	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a.) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper



b.) 125°C/W when mounted on a minimum pad

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source servers only as protection against ESD. No gate overvoltage rating is implied.
4. Starting T_J = 25°C, L = 3 mH, I_{AS} = 20 A, V_{DD} = 40 V, V_{GS} = 10 V.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

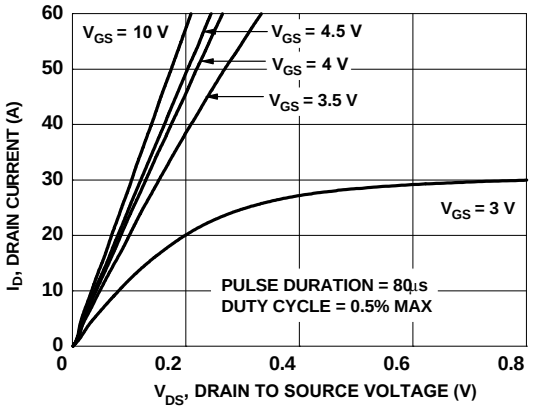


Figure 1. On−Region Characteristics

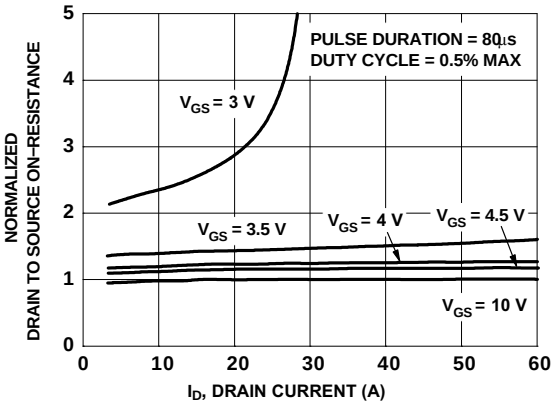


Figure 2. Normalized On−Resistance vs Drain Current and Gate Voltage

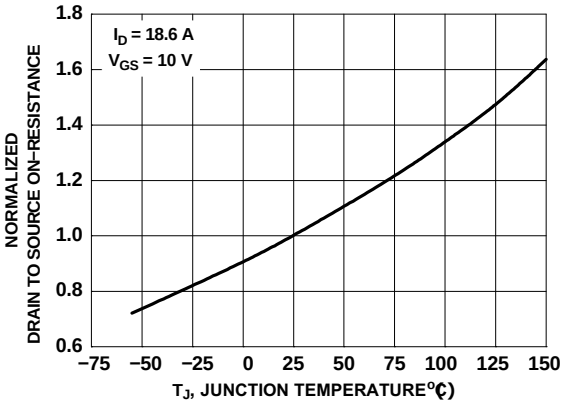


Figure 3. Normalized On−Resistance vs Junction Temperature

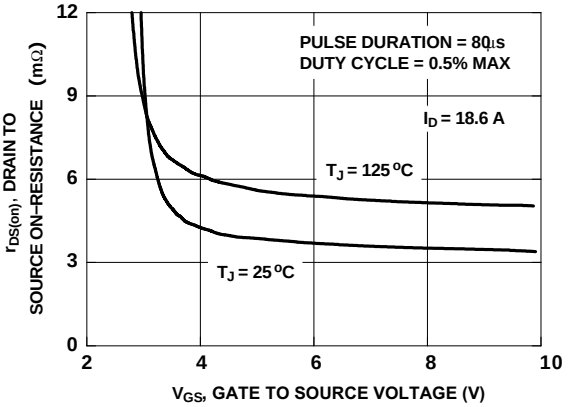


Figure 4. On−Resistance vs Gate to Source Voltage

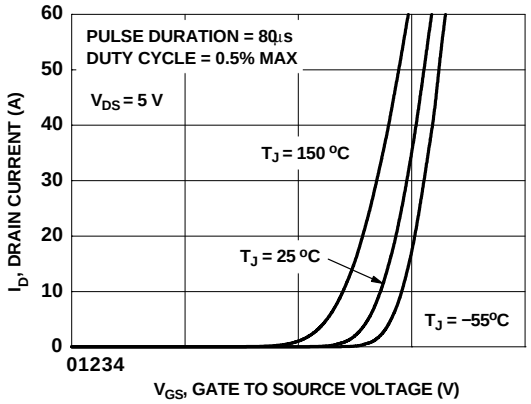


Figure 5. Transfer Characteristics

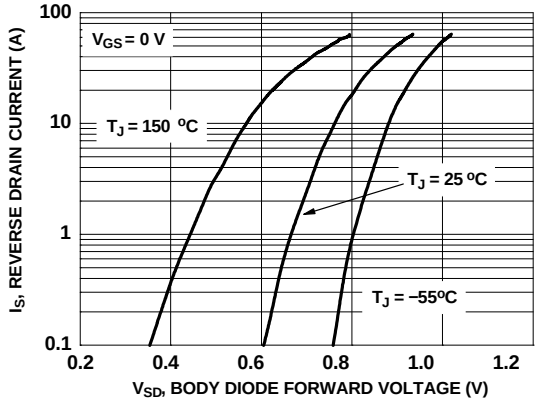


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

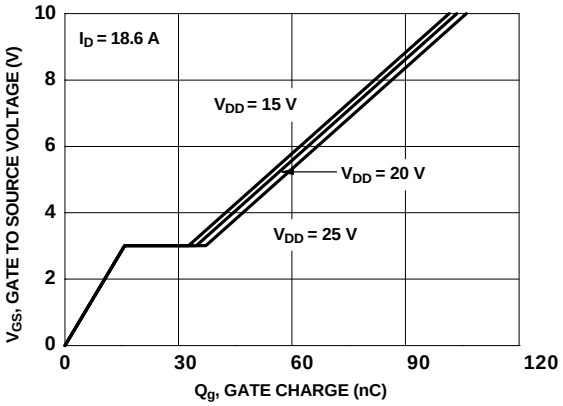


Figure 7. Gate Charge Characteristics

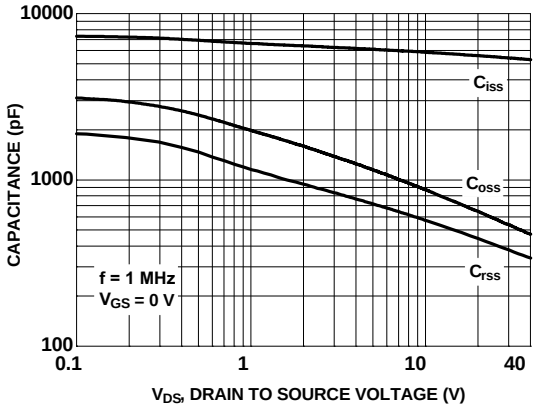


Figure 8. Capacitance vs Drain to Source Voltage

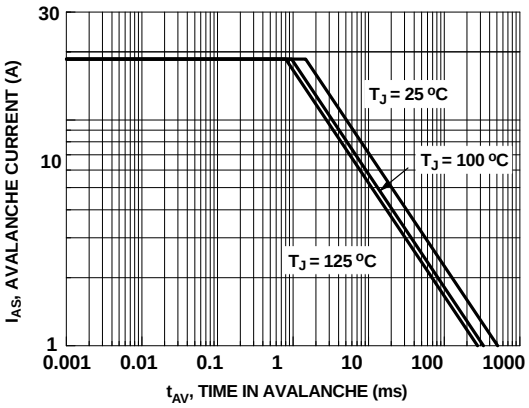


Figure 9. Unclamped Inductive Switching Capability

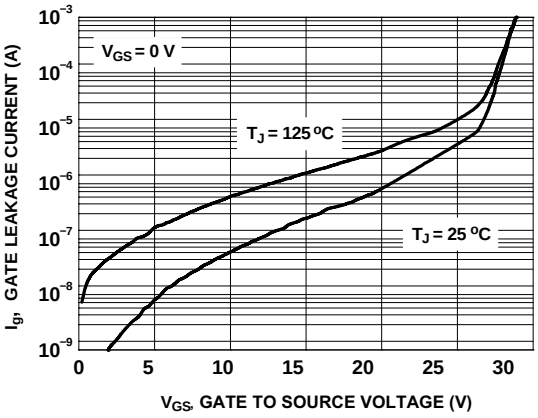


Figure 10. I_{GSS} vs V_{GS}

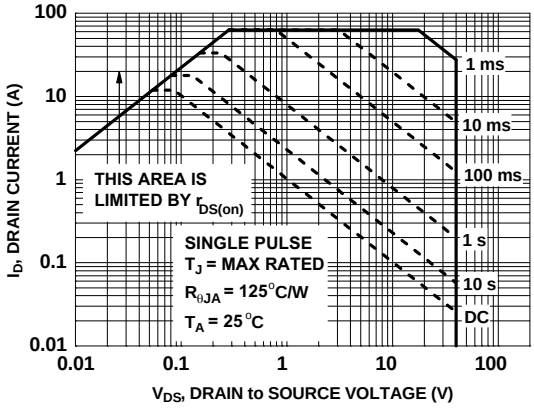


Figure 11. Forward Bias Safe Operating Area

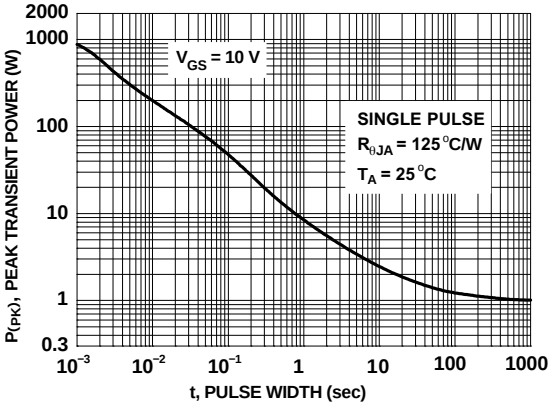


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

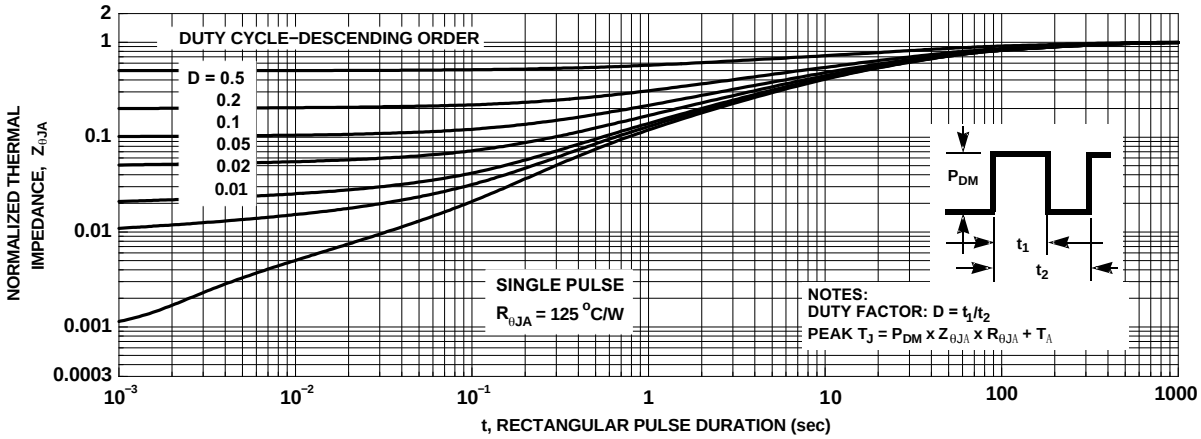
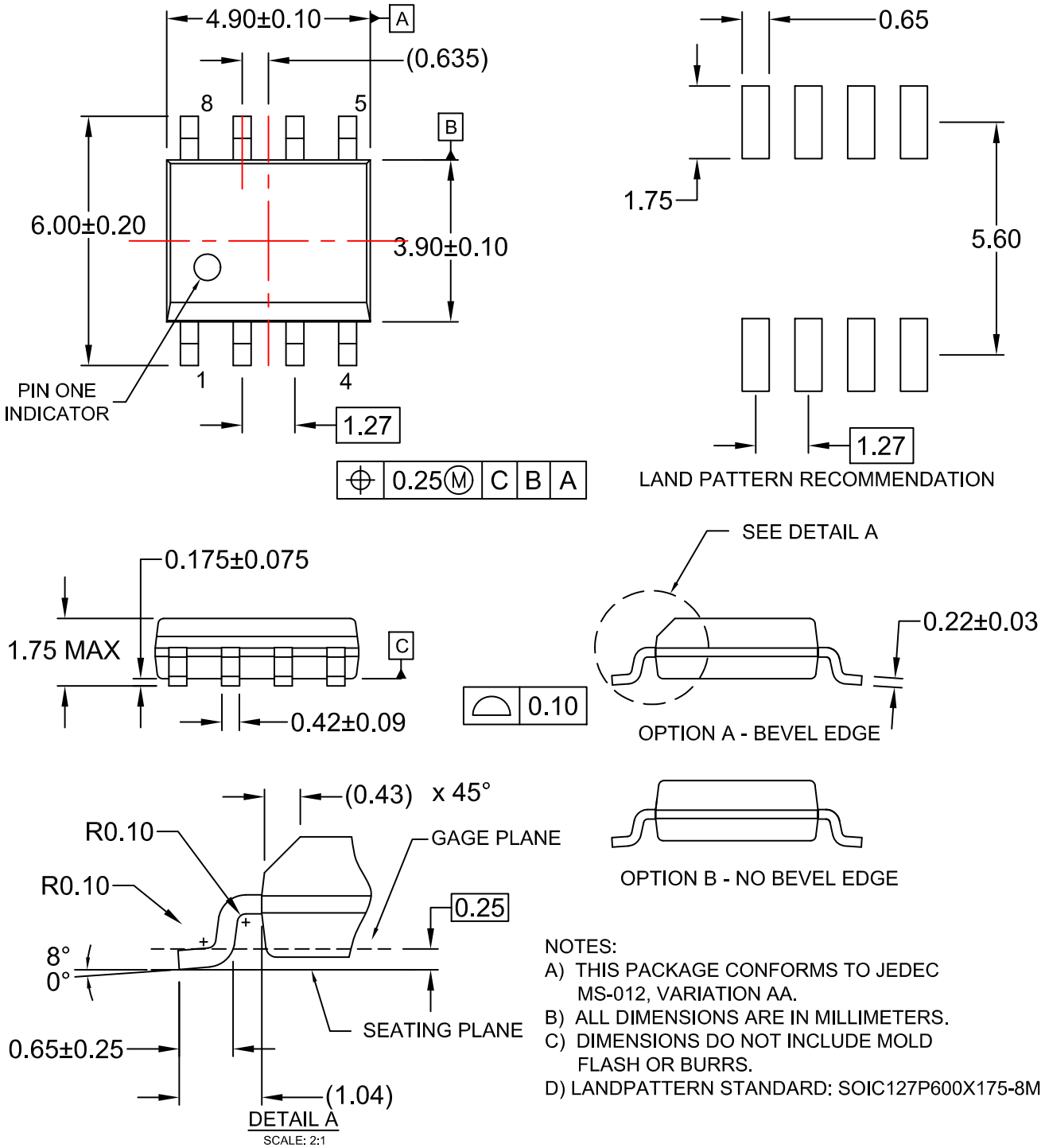


Figure 13. Transient Thermal Response Curve

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DATE 24 AUG 2017



NOTES:
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C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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