Power Multiplexer for USB High Side Switch

General Description

The uP7536 is a current limited power multiplexer acting as a high side switch for USB applications where heavy capacitive loads and short-circuits are likely to be encountered. It switches output voltage to 5VSB at S3/S4/S5 states with 400mΩ switch and 200mA capacity; to 5VCC at S0/S1/S2 states with 80mΩ switch and 1.5A capacity.

This device features an active-high enable control input. Soft start function limits the inrush current from supply input when enabled. Disabling the device reduces its standby current down to less than 1uA.

Optimal switch logic according to S3# and 5VCC status ensures seamless output voltage transition.

When the output load exceeds the current-limit threshold or a short is present, the uP7536 asserts over current protection and limits the output current to a safe level by driving the power switches into saturation mode.

Other features include soft-start to limit inrush current during plug-in, thermal shutdown to prevent catastrophic switch failure from high-current loads, under-voltage lockout (UVLO) to ensure that the device remains off unless there is a valid input voltage present. The uP7536 is available in SOT23-8L, (P)SOP-8L, MSOP-8L packages.

Applications

- **Notebook and Desktop PCs**
- **USB Power Management**
- **ACPI Power Distribution**
- **Hot-Plug Power Supplies**

Features

- **Compliant to USB Specifications**
- **Operating Range: 4.5 V to 5.5 V**
- **Output Voltage Switch to 5VSB at S3/S4/S5**
  - **200mA Continuous Load Current**
  - **400mΩ High Side Switch**
- **Output Voltage Switch to 5VCC at S0/S1/S2**
  - **1.5A Continuous Load Current**
  - **80mΩ High Side Switch**
- **Low Quiescent Current: 50uA Typical**
- **Low Standby Current: Less Than 1uA**
- **Slow Turn On and Fast Turn Off**
- **Enable Active-High**
- **UL Approved : E316940**
- **TuV EN60950-1 Certification**
- **CB IEC60950-1 Certificatioon**
- **RoHS Compliant and Halogen Free**

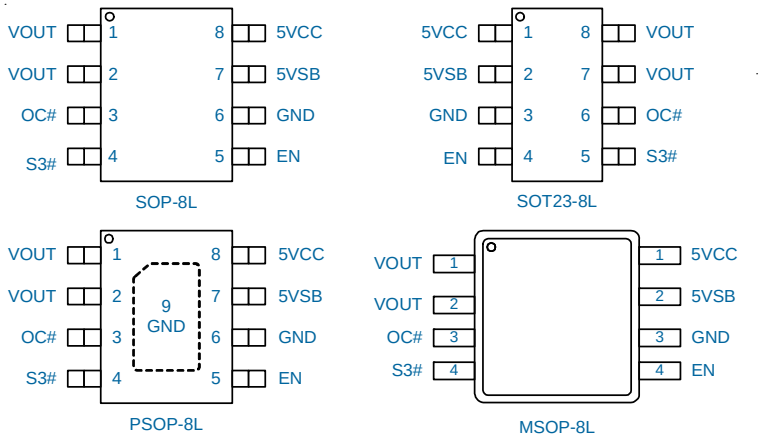
Ordering Information

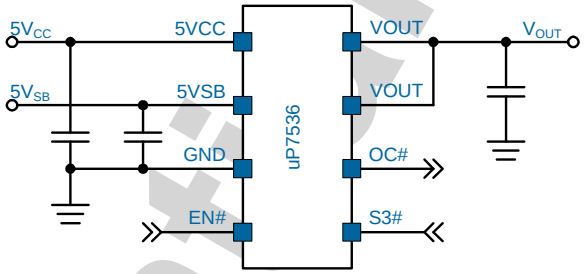
Order Number	Package	Top Marking
uP7536AMA8	SOT23-8L	S32
uP7536ASW8	PSOP-8L	uP7536A
uP7536ARA8	MSOP-8L	uP7536A
uP7536BMA8	SOT23-8L	S58
uP7536BSW8	PSOP-8L	uP7536B
uP7536BRA8	MSOP-8L	uP7536B

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

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Pin Configuration & Typical Application Circuit



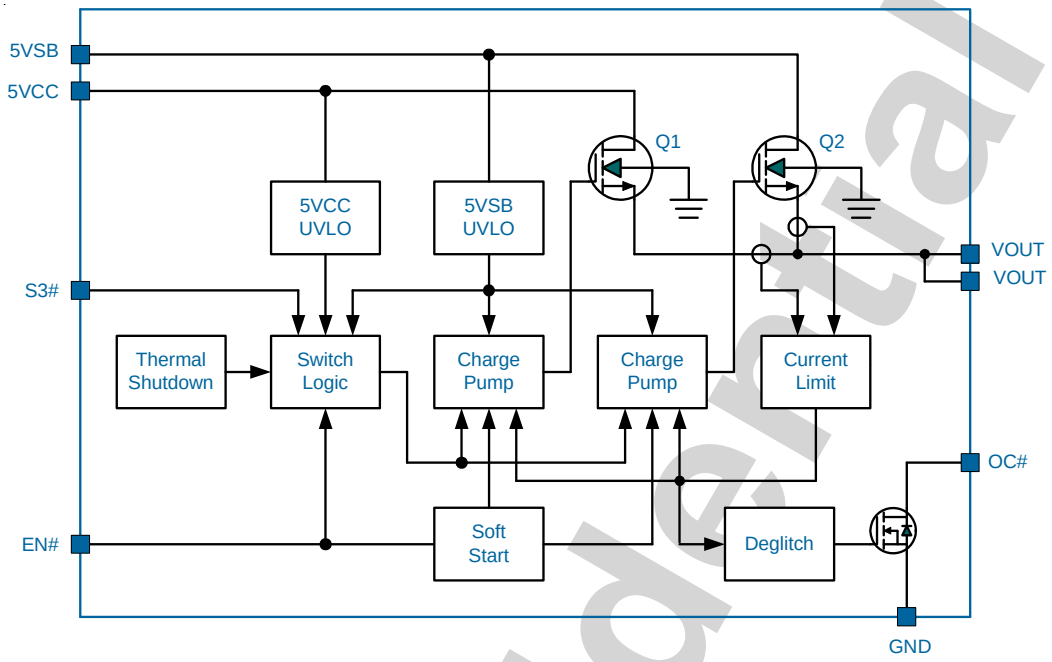


Functional Pin Description

Pin Name	Pin Function
5VCC	**Supply Input from 5VCC.** This pin is the N-Channel MOSFET Drain that supplies output current at S0/S1/S2 states and should be connected to 5VCC. Bypss this pin with a minimum 1uF capacitor to ground.
5VSB	**Supply Input.** This pin is the N-Channel MOSFET Drain that supplies output current at S3/S4/S5 states and should be connected to 5VSB. This pin also supplies operating current for the device. Bypass this pin with a minimum 1uF capacitor to ground.
GND	**Ground.**
EN	**Enable Input.** This is the enable input to turn on/off the power switch. Pulling low this pin shuts down the device.
S3#	**Sleep State Control Pin.** This pin along with the 5VCC status controls the switching configuration.
OC#	**Fault Flag.** This is an active-low, open-drain fault flag output for the power switch. The uP7536 asserts this pin low when fault occurs with typical 8ms deglitch delay.
VOUT	**Output Voltage.** These pins are output from N-Channel MOSFET Sources. Bypass these pins with a minimum 10uF capacitor to ground.

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Functional Block Diagram



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Functional Description

Power Switches

The uP7536 is a current limited power multiplexer acting as a high side switch for USB applications where heavy capacitive loads and short-circuits are likely to be encountered. It contains two N-Channel MOSFETs Q1 and Q2 as power switches that supply output current to VOUT pins. The sources of Q1 and Q2 are connected together to the VOUT pins, the drain of Q1 is connected to 5VCC pin and the drain of Q2 is connected to 5VSB pin. The MOSFETs are without body diode and prevent current flows when turned off.

Q2 is a 400mΩ MOSFET with 200mA capacity and Q1 is a 80mΩ MOSFET with 1.5A capacity. The power switches are driven by internal charge pumps and controlled by S3# and enable status. The uP7536 switches the output voltage to 5VSB through Q2 at S3/S4/S5 states, to 5VCC through Q1 at S0/S1/S2 states.

Charge Pumps and Drivers

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

Chip Enable

The EN pin receives a TTL or CMOS compatible input to enable/disable the uP7536. Logic low disables the power switch, charge pump, gate driver and other circuitry and reduces the supply current down to less than 1uA. Logic high restores bias to the drive and control circuits and turns the switch on.

Soft Start

The uP7536 features soft start function to eliminate the inrush current into downstream and voltage droop of upstream when hot-plug-in with capacitive loads. The soft start interval is 1.3ms typically. The input current to charge up the load capacitor is proportional to its capacitance. The uP7536 current limit function may be active during the plug-in of extreme large capacitive load.

Over Current Limit

The uP7536 continuous monitors the output current for over current protection to protect the system power, the power switch, and the load from damage during output short circuit or soft start interval. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load. The current limit level is typical 2.3A when the power switch operates in linear region and is typical 1.5A in saturation region.

The uP7536 asserts fault condition and pulls low OC# when over current, over temperature, input under voltage lockout condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 8ms deglitch circuit prevents the OC# signal from oscillation

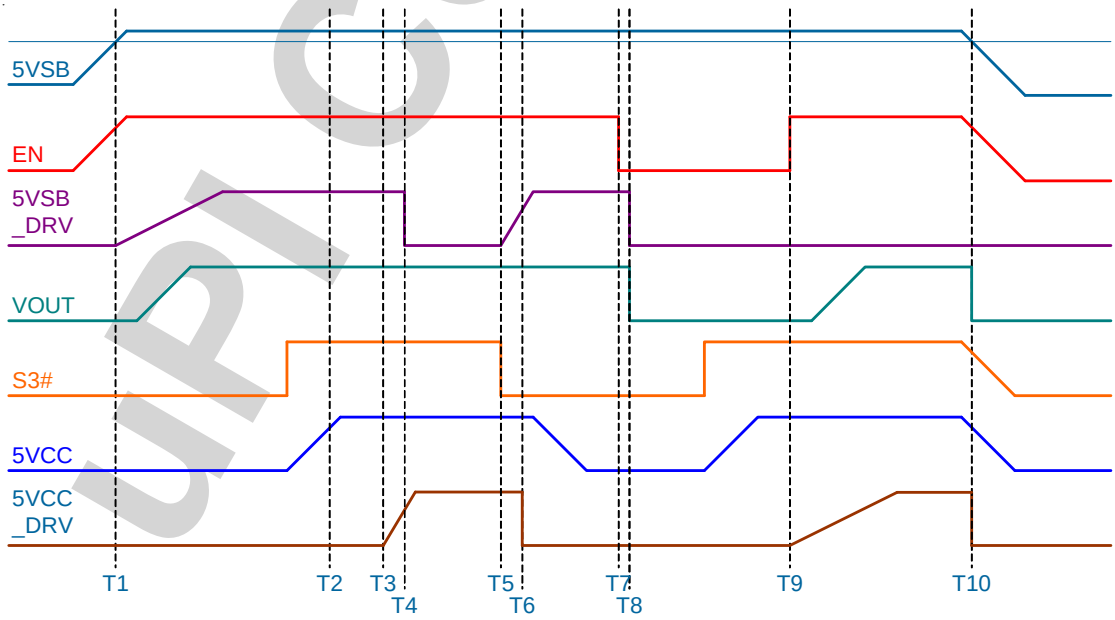


Figure 1. Typical Timing Diagram

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or false triggering. If an over temperature shutdown occurs, the OC# is asserted instantaneously.

Under Voltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 4.2V, a control signal turns off the power switch.

Over Temperature Protection

The uP7536 continuously monitors the operating temperature of the power switch for over temperature protection. The uP7536 asserts over temperature and turns off the power switch to prevent the device from damage if the junction temperature rises to approximately 135°C due over current or short-circuit conditions. Hysteresis is built into the thermal sense, the switch will not turn back on until the device has cooled approximately 20 degrees. The open-drain false reporting output (OC#) is asserted (active low) when an overtemperature shutdown or over current occurs. If the fault condition is not removed, the switch will pulse on and off as the temperature cycles between these limits.

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Absolute Maximum Rating

(Note 1)

Supply Input Voltage, 5VSB ---------- -0.3V to +5.7V
Other Pins ---------- -0.3V to +5.7V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
SOT23-8L θ_{JA} ---------- 250°C/W
SOT23-8L θ_{JC} ---------- 140°C/W
SOP-8L θ_{JA} ---------- 160°C/W
SOP-8L θ_{JC} ---------- 40°C/W
PSOP-8L θ_{JA} ---------- 50°C/W
PSOP-8L θ_{JC} ---------- 5°C/W
MSOP-8L θ_{JA} ---------- 160°C/W
MSOP-8L θ_{JC} ---------- 40°C/W
Power Dissipation, P_D @ T_A = 25°C
SOT23-8L ---------- 0.4W
SOP-8L ---------- 0.625W
PSOP-8L ---------- 2.0W
MSOP-8L ---------- 0.625W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{IN} ---------- +4.5V to +5.5V

Electrical Characteristics

($5V_{SB}$ = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input 5VSB						
Suppy Input Voltage Range			4.5	--	5.5	V
Under Voltage Lockout	V_{UVLO}	5VSB rising	--	4.3	4.5	V
UVLO Hysteresis			--	80	--	mV
Shutdown Current	I_{SD}	No load on VOUT, Disabled	--	0.01	1	uA
Quiescent Current	I_Q	No load on VOUT, Enabled, S3# = 0, 5VCC = 0V	--	50	70	uA
Supply Input 5VCC						
Supply Input Voltage Range			4.5	--	5.5	V
Under Voltage Lockout	V_{UVLO}	5VCC rising	--	4.3	4.5	V
UVLO Hysteresis			--	80	--	mV

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Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Enable Control						
High Level Threshold			1.2	--	--	V
Low Level Threshold			--	--	0.4	V
Enable Pin Input Current			-1	--	1	uA
Enable Delay	T_{D_EN}	Enable threshold to VOUT starting to ramp up	--	0.15	1	ms
Power Switch for 5VSB (Q2)						
N-MOSFET ON Restiance	$R_{DS(ON)}$	I_{OUT} = 100mA	--	400	500	mΩ
Leakage Current		VOUT connected to GND, Disabled	--	--	1	uA
Reverse Leakge Current		V_{OUT} = 5.5V, 5VSB = 0V	--	--	1	uA
Power Switch for 5VCC (Q1)						
N-MOSFET ON Restiance	$R_{DS(ON)}$	I_{OUT} = 1A @ 25°C	--	80	100	mΩ
Leakage Current		5VCC = 5.5V, VOUT = 0V, Disabled	--	--	1	uA
Reverse Leakge Current		V_{OUT} = 5.5V, 5VCC = 0V, Disabled	--	--	1	uA
Current Limit						
Current Limit Threshold for Q2		for uP7536A	300	750	1500	mA
		for uP7536B	500	1000	1500	
Current Limit Threshold for Q1			1.7	2.3	4.6	A
OC# Ouptut Low Voltage		$I_{OC\#}$ = 5mA	--	--	0.4	V
Off State Current		V_{OC}# = 5.5V	--	--	1	uA
OC# Deglitch		OC# assertion	4	8	15	ms
		OC# de-assertion	150	250	500	us
Softstart						
Output Voltage Ramp Up Time		S3# = 0V, C_{OUT} = 10uF, No Load	--	1.3	--	ms
		S3# = 5V_{CC} = 5V, C_{OUT} = 10uF, No Load	--	1.3	--	ms
Over Temperature Protection						
Thermal Shutdown Threshold Level		By Design	--	135	--	°C
Thermal Shutdown Hysteresis		By Design	--	30	--	°C

Note 1. Stresses beyond those listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operation Condition* section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

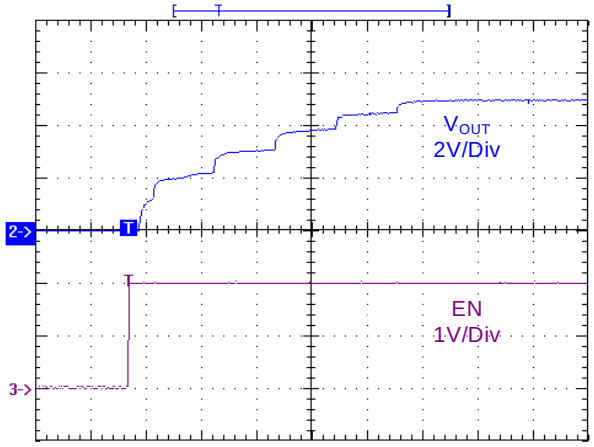
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. These items are not tested in production, specified by design.

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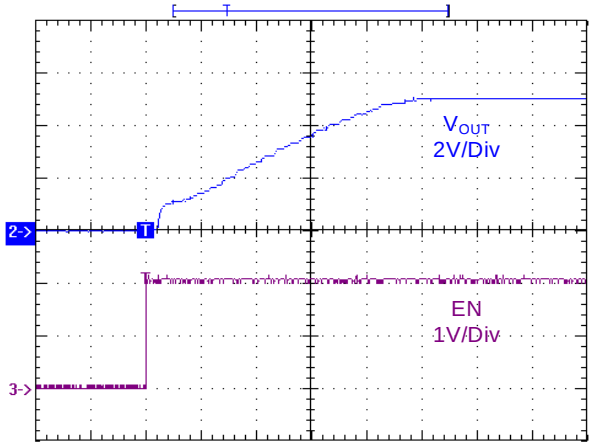
Typical Operation Characteristics

Trun On into 5VSB



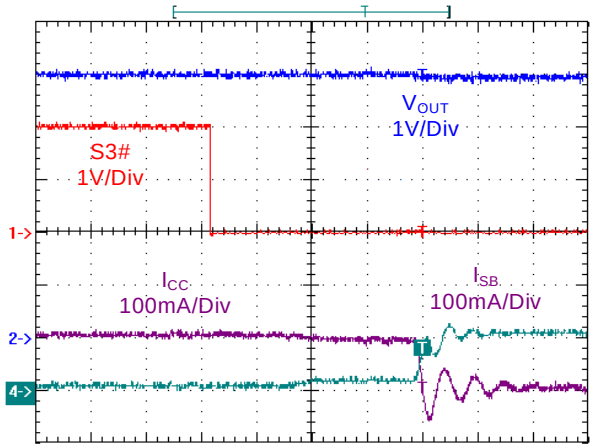
Time (250us/Div)
C_{OUT} = 1uF, S3# = 0V

Trun On into 5VCC



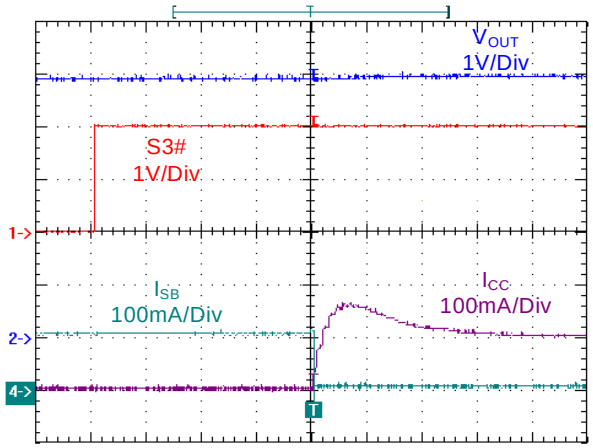
Time (250us/Div)
C_{OUT} = 1uF, S3# = 5V

S3# form High to Low



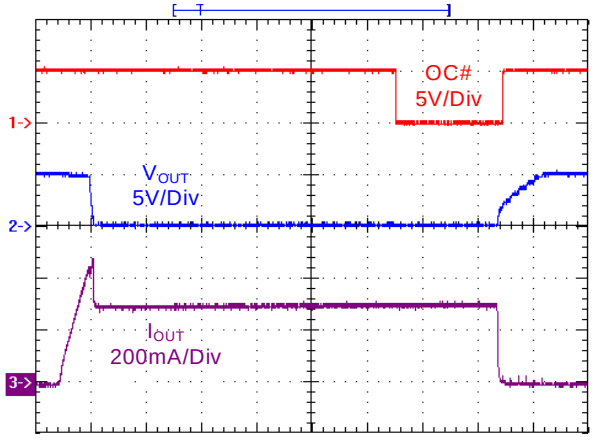
Time (10us/Div)
C_{OUT} = 1uF, I_{OUT} = 100mA

S3# from Low to High



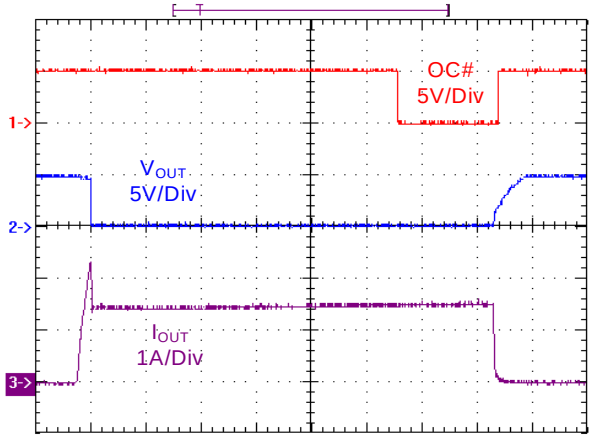
Time (500us/Div)
C_{OUT} = 1uF, I_{OUT} = 100mA

OCP for 5VSB



Time (2ms/Div)
C_{OUT} = 10uF, S3# = Low

OCP for 5VCC

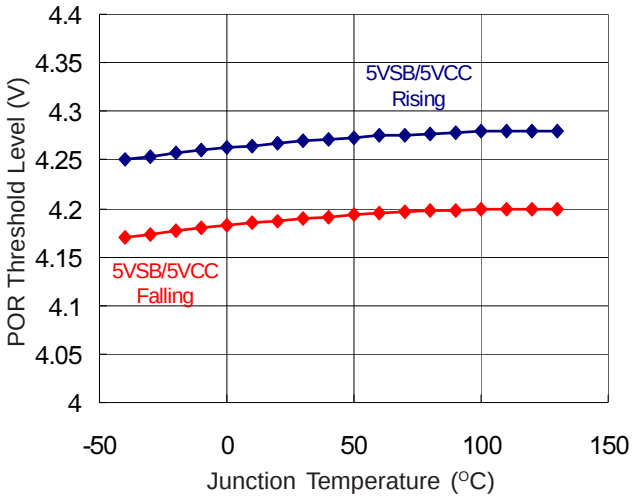


Time (2ms/Div)
C_{OUT} = 10uF, S3# = High

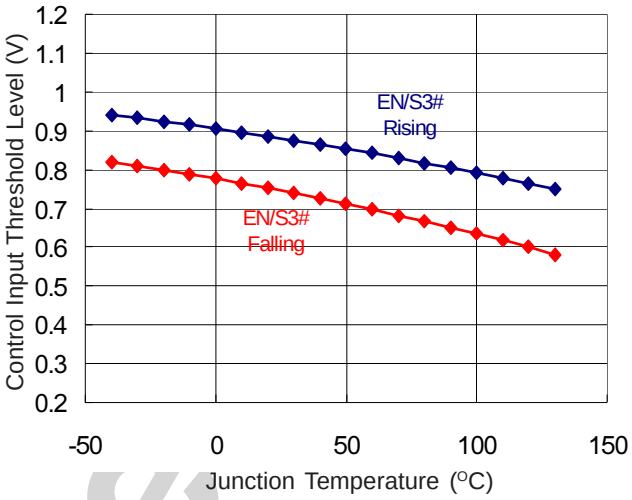
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Typical Operation Characteristics

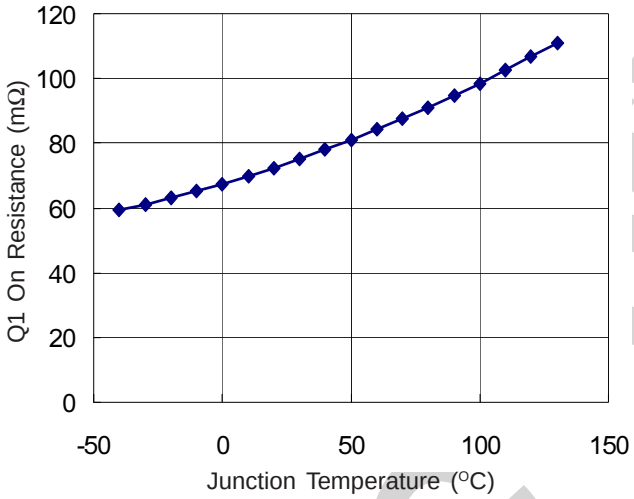
POR Threshold Level vs. Temperature



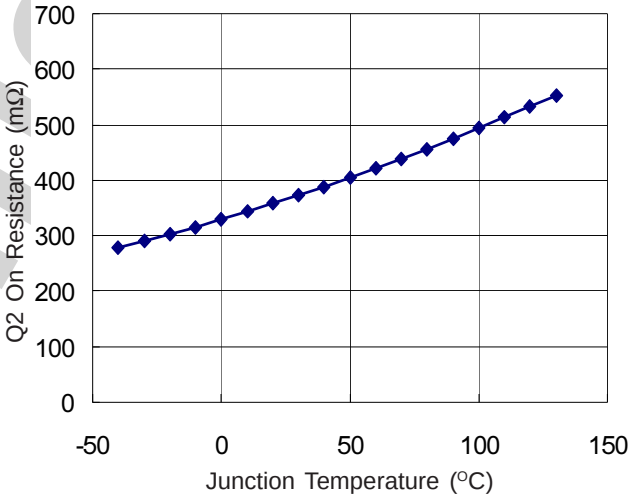
Control Input Level vs. Temperature



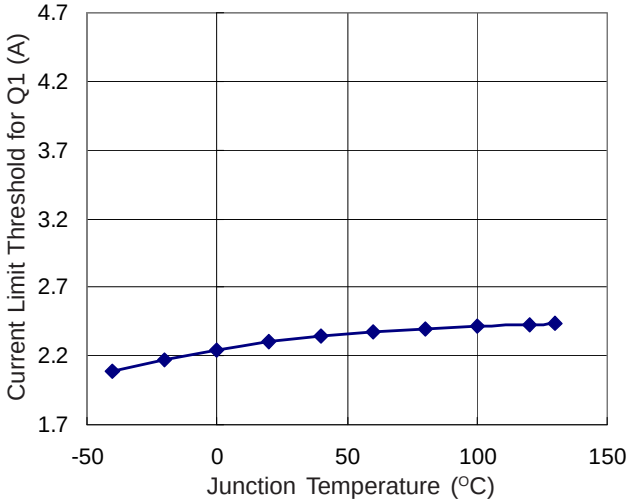
Q1 On Resistance vs. Temperature



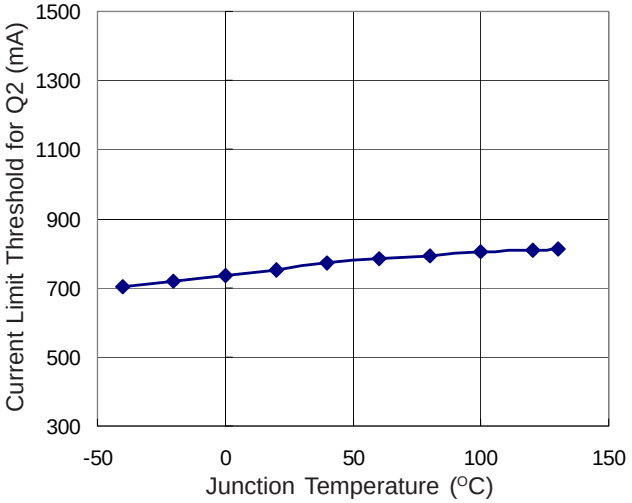
Q2 On Resistance vs. Temperature



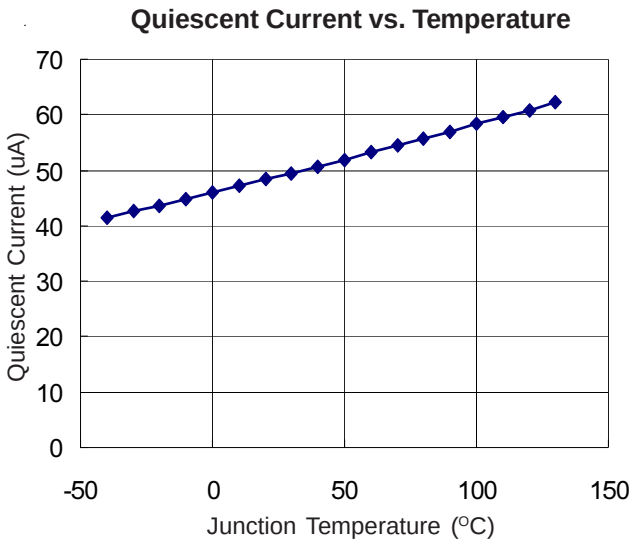
5VCC Q1 Current Limit vs. Temperature



5VSB Q2 Current Limit vs. Temperature



Typical Operation Characteristics



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Application Information

The uP7536 is a current limited power multiplexer acting as a high side switch for USB applications where heavy capacitive loads and short-circuits are likely to be countered. It switches output voltage to 5VSB at S3/S4/S5 states with 450mΩ switch and 200mA capability; to 5VCC at S0/S1/S2 states with 90mΩ switch and 1.5A capability.

This device features an active-high enable control input. Soft start function limits the inrush current from supply input when enabled. Disabling the device reduces its standby current down to less than 1uA. Optimal switch logic according to S3# and 5VCC status ensures seamless output voltage transition. When the output load exceeds the current-limit threshold or a short is present, the uP7536 asserts overcurrent protection and limits the output current to a safe level by driving the power switches into saturation mode.

Other features include soft-start to limit inrush current during plug-in, thermal shutdown to prevent catastrophic switch failure from high-current loads, under-voltage lockout (UVLO) to ensure that the device remains off unless there is a valid input voltage present. The uP7536 is available in SOT23-8, (P)SOP-8, and MSOP-8 package.

Input and output capacitors

Bypass the supply input pins with a single 4.7uF capacitor as close as possible to the uP7536. A 4.7uF output capacitor at the output pin is recommended even much larger output capacitors are already available at the output of the uP7536, especially if the output capacitors are more than 2 inches away on the PCB. The inrush current to charge the output capacitors is calculated as:

$$I_{IN} = C_{OUT} \times \frac{V_{OUT}}{T_{SS}} \text{ (A)}$$

Special care should be paid to large output capacitor applications. Take C_{OUT} = 1000uF as example, the inrush current is I_{IN} = 1000uF x 5V / 1.3ms = 3.8A. This is higher than the current limit threshold of Q1 and Q2. In this case, the output voltage ramp up time is controlled by the current limit function of Q1 and Q2. Fault indication function may be false triggered and pull low the OC# as shown in Figure 1. The OC# is pulled low after 8ms delay and released when V_{OUT} > 2V.

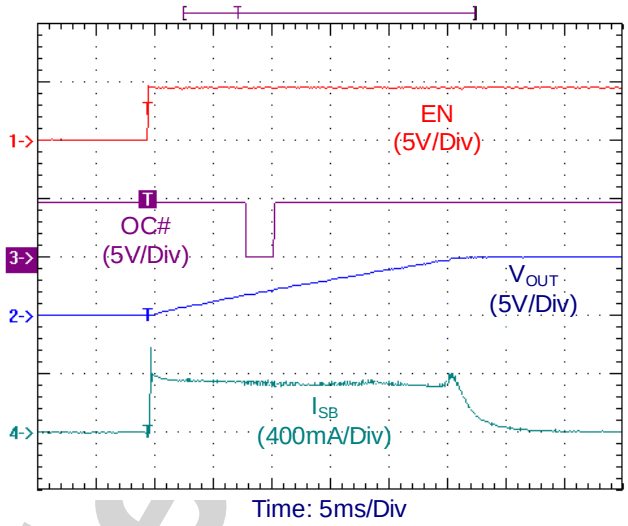


Figure 1. Turn on into 5VSB with 2000uF output capacitor.

Hot Plug Application

The output voltage undergoes an abrupt drop when a device with large input capacitors is hot plugged into the output of uP7536 as shown in Figure 2, where a device with 1500uF is hot plugged into uP7536 output with 470uF output capacitor. The output voltage ramp up time is controlled by the current limit level. The OC# is not pulled low since the output voltage is kept higher than 2.0V before the delay time.

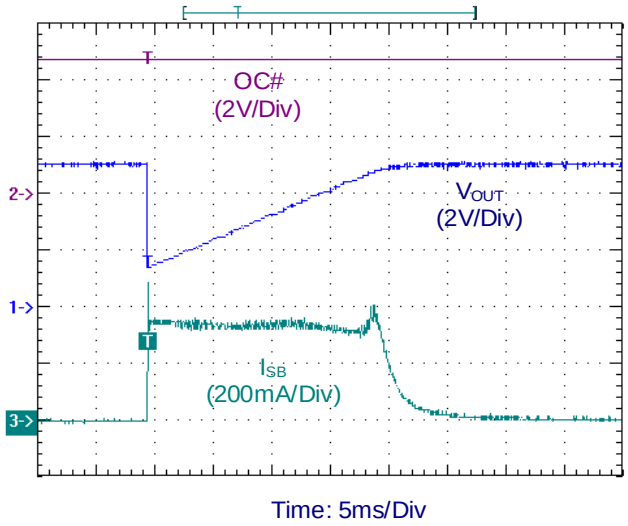


Figure 2. Hot plug application with S3# = 0V.

Thermal Consideration

Temperature effect should be well considered when dealing with voltage drop and power dissipation. The maximum $R_{DS(ON)}$ of the power switch is 90mΩ of Q1 under 25°C junction temperature. If the device is expected to operate

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at 125°C junction temperature, the $R_{DS(ON)}$ of Q1 will become

90mΩ * (1 + (125°C - 25°C) * 0.5%/°C) = 135mΩ

where 0.5%/°C is the approximated temperature coefficient of the $R_{DS(ON)}$.

If the maximum load current is expected to be 1.2A, the maximum voltage will become

1.2A * 100mΩ = 120mV

This in turn will cause power dissipation as

1.2A * 120mV = 144mW

The temperature raise is calculated as

144mW * 250°C/W = 36°C

The junction temperature is calculated as T_A + 36°C, where T_A is the expected maximum ambient temperature. A few iterations are required until get final solutions.

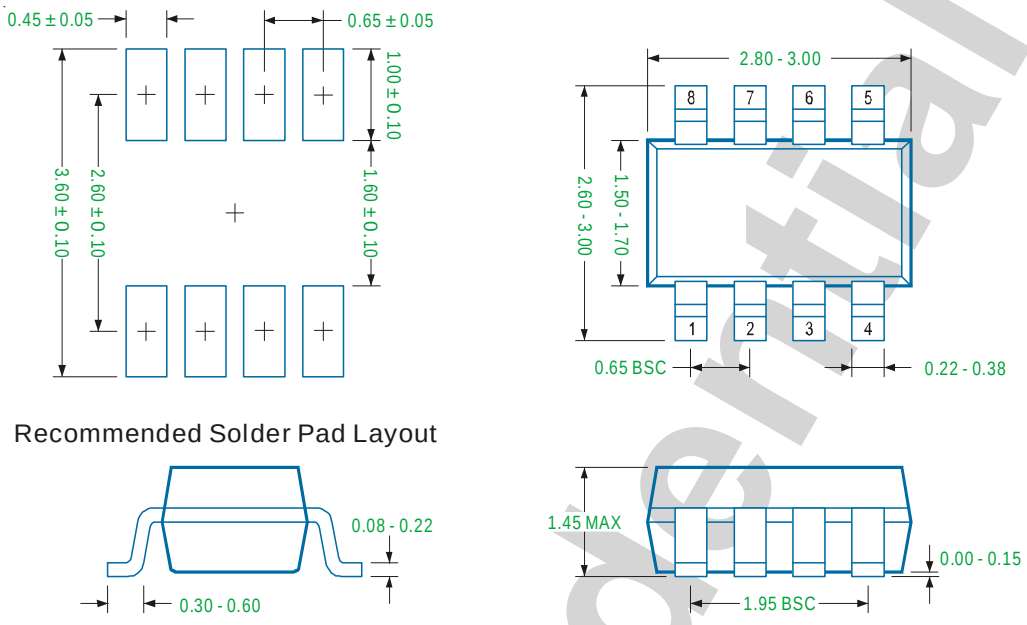
PCB Layout Consideration

- Place the uP7536 as close to the USB connector as possible to minimize the parasitic elements.
- Keep the power trace short and wide to minimize the parasitic resistance along the trace.
- Place the bypassing capacitor as close to the device as possible.

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Package Information

SOT23-8L



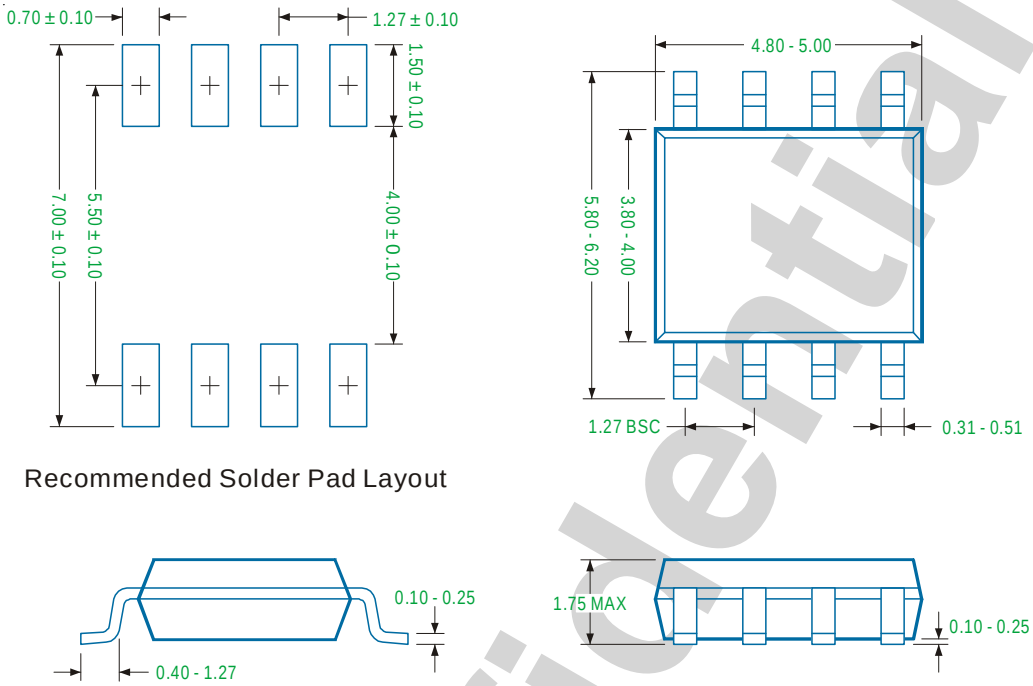
Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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Package Information

SOP- 8L



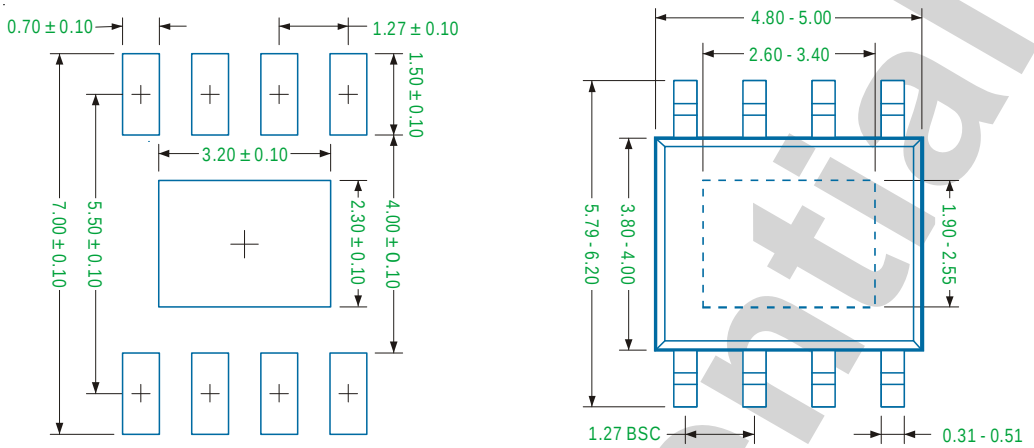
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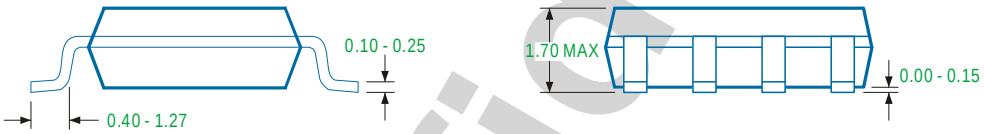
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Package Information

PSOP- 8L



Recommended Solder Pad Layout



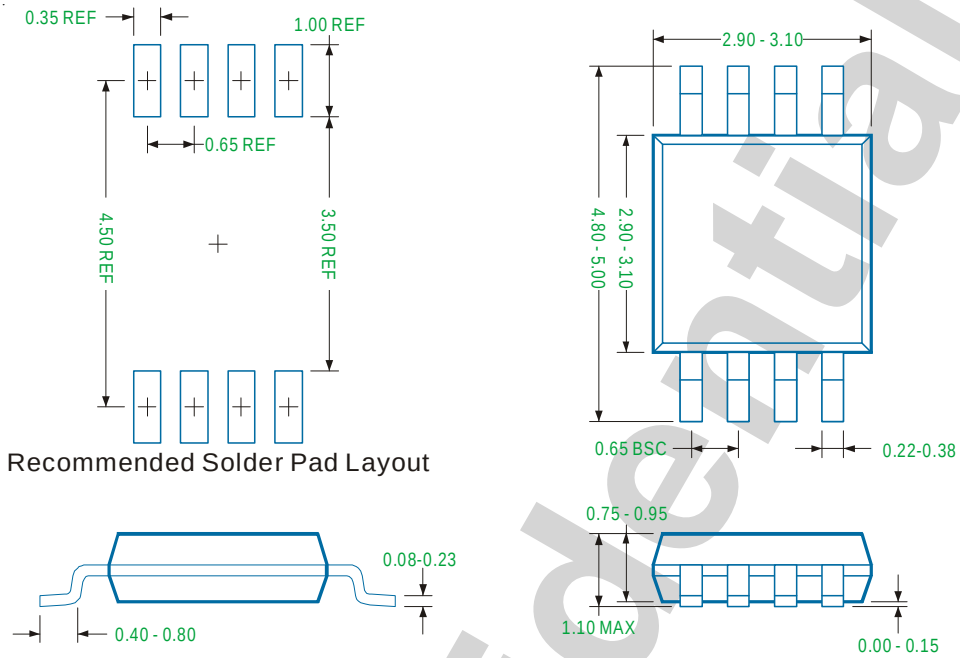
Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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Package Information

MSOP- 8L



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